

INVERTER NON-LINEARITIES IN PROGNOSIS OF DRIVE SYSTEMS  
FINAL RESEARCH REPORT

Andrew Babel  
The Marshall Plan Scholarship Recipient  
PhD Student  
Michigan State University  
East Lansing, Michigan 48824, USA

Supervised and Approved by:  
Univ.-Prof. Dr.-Ing. Annette Mütze

Graz University of Technology  
Electric Drives and Machines Institute  
Inffeldgasse 18/1 A8010 Graz, Austria

Submitted to:  
The Austrian Marshall Plan Foundation  
in fulfillment of the requirements of  
Austrian Marshall Plan Scholarship 2013

2013

## ACKNOWLEDGMENTS

Without the scholarship provided by the Austrian Marshall Plan Foundation, this opportunity would not have been possible. The scholarship would have been unknown and unavailable to me, were it not for the collaboration between Professor Annette Mütze and Professor Elias Strangas, who introduced this scholarship to me. I am incredibly appreciative of Professor Mütze for the great effort that she has spent with me in my professional development during my time with her institute and her effort to make my stay in Graz pleasant. Professor Strangas also, as always, provided me with invaluable guidance during this experience.

I would like to thank Kathrin Manninger in the International Relations and Mobility Programmes Office for helping me greatly with the application process, my arrival, and all of the associated paperwork.

Additional financial support for my travel was provided by the Michigan State University Graduate School Research Enhancement Grant. With this, my research stay was more comfortable and productive; I greatly appreciate that financial contribution.

I would not have had such an enriching experience without the students and staff of the Electric Machines and Drive Institute at the Graz University of Technology. I would like to give thanks to everyone I worked with; most notably Dr. Krischan, Dr. Seebacher, and Mr. Seelmeister. In addition, the administrative assistance from Ms. Liebmann was invaluable, I thank you for this. Overall, the friendships and warm welcome given to me by all of the students and staff will carry with me: Hendrik, Alex, Dr. Krischan, Madeleine, Werner, Klaus Sobe, Stephan, Dr. Bacher, Mr. Gläsel, Mr. Schloffer, and Klaus Lang; I thank you.

Further, I would like to thank my colleagues at the Electrical Machines and Drives Lab at Michigan State University for their support during my time overseas.

I would like to give special thanks to my wife, Sandy, for putting her career on hold for six months in order to follow me to another continent for an adventure I know we will both remember fondly.

## PREFACE

**Organization** This report is the compilation of all of the reports and manuscripts assembled from work done while I was a visiting researcher at the Technical University of Graz in Graz, Austria. The research results became two papers. One paper was accepted to the prestigious Applied Power Electronics Conference for 2014; the second will be submitted to another eminent conference: the 2014 Energy Conversion Congress and Exposition. Due to the high quality of the papers, they will then be submitted to reputable journals. The papers will be either submitted to the *IEEE Transactions on Industrial Applications*, *IEEE Transactions on Power Electronics*, or *IEEE Transactions on Industrial Electronics*.

**Chapter 1: Initial Literature Review** This chapter introduces the possible inverter nonlinearities and concludes that the main ones of interest are the current-voltage relationship of the IGBT collector-to-emitter and the diode anode-to-cathode. Further, it discusses the two main motivations for the study of inverter nonlinearities: compensation for the voltage drop and diagnosis and prognosis. The method then discusses the possible nonlinear voltage drops which might exist over the collector-emitter and anode-cathode, respectively. These include the deadtime, forward voltage drop, effects of propagation delay, and pwm resolution. The chosen method identifies the forward voltage drop and was at the time of this report a method which uses applied direct currents with knowledge of the duty cycle to identify all of the devices. This was the preliminary literature review; the manuscripts have updated information which was used to refine the method chosen - as well as new - previously undiscussed, methods.

**Chapter 2: Initial Characterization Results Report** This chapter reviews the chosen method and introduces another which uses a slightly different approach: the spectral composition of the PWM signal. All methods use a voltage sensor placed from the inverter phases to the negative DC link. The duty cycle with direct current method is first discussed, and attempts to characterize the inverter using the mean of the PWM waveform with the duty cycle. This is derived analytically, but performs poorly because of noise. A similar method using the mean

and RMS calculations are performed, and these have a similar noise problem. To address the noise problem, a method based upon the frequency content of the measured PWM signal is performed, and this is able to determine the device characteristics, and is more noise-resistant. This is shown analytically, in simulation, and in experimentation. This report also looks into characterizing the inverter with applied alternating currents. This is successful, but at the time of this report, the spectral method was not applied to the inverter. The last portion of this report proves that no combination of applied direct currents will result in a set of equations which can be used to solve for the individual device voltages given that the sensors are not placed with respect to the negative DC link.

**Chapter 3: Inverter Characterization Manuscript Submitted to APEC 2014** This manuscript builds upon the work done in the characterization results report. This manuscript repeats the basic literature review of the previous reports, and demonstrates the issue of nonlinearities with more evidence. The voltage disturbance for a direct current representation is shown analytically for use in proving the characterization methods. The analytical expression of AC PWM voltage is derived analytically, but this expression proves too complex for use in analysis. Two methods are investigated which use direct currents: the mean and the spectral methods already previously discussed. Two methods are discussed for an alternating current: the “algorithm” method previously discussed and the method which assumes local “DC-like” behavior and characterizes with the short-time Fourier transform.

**Chapter 4: Inverter Condition Monitoring Manuscript to be Submitted to ECCE 2014** The unsubmitted manuscript investigates inverter nonlinearities from the condition monitoring perspective. Specifically, the ways in which inverter nonlinearities affect the condition monitoring algorithms are discussed. The state of the art of all condition monitoring disciplines is given for inverters. The inverter fault of interest is the bond wire lift-off. This is modeled and the appropriate background literature reviewed. In addition, the experimental imposition of the fault is shown, because that the actual inverter could not be damaged in the test system. Under this fault, possible diagnostic methods are given, first using the characterization proce-

dure. Linear discriminant classification (LDC) is then used to diagnose faults of different severities, and the selection of observations with knowledge of device nonlinearities is discussed as a way to improve the success of the LDC diagnosis. Prognosis is discussed by first introducing the prognostic model for bond wire lift-off, which is primarily a thermal- and thermal-mechanical model. The study of nonlinearities and characterization are vital, as the estimate of remaining useful life is greatly improved.

# CONTENTS

<b>Chapter 1 Literature Review</b>	<b>1</b>
1.1 Introduction	1
1.2 Discussion of Nonlinearities	2
1.2.1 Deadtime	2
1.2.2 Forward Voltage Drop	5
1.2.3 Propagation Delay and PWM Resolution	6
1.3 Characterization Methods	6
1.4 Chosen Characterization Method	7
1.4.1 Details of Method of Choice	9
1.5 Conclusion and Future Work	10
<b>Chapter 2 Characterization Investigation Results</b>	<b>11</b>
2.1 Introduction	11
2.2 Characterization of an Inverter with Applied Direct Current	13
2.2.1 Characterization with $V_\phi \rightarrow V_{DC-}$	13
2.2.1.1 Method 1: Dual Duty Cycle Mean Calculation Method	15
2.2.1.1.1 Derivation	16
2.2.1.1.2 Simulation	17
2.2.1.1.3 Experimental	18
2.2.1.2 Method 2: Mean and RMS Calculation Method	18
2.2.1.2.1 Derivation	19
2.2.1.3 Method 3: DFT Spectral Method	20
2.2.1.3.1 Derivation	20
2.2.1.3.2 Simulation	21
2.2.1.3.3 Experimental	22
2.2.2 Characterization with $V_\phi \rightarrow V_\phi$	22
2.3 Characterization of an Inverter with Applied Alternating Current	27
2.4 Conclusion	29
2.5 Appendix: Derivation of Phase Voltage Sensor Method	30
2.5.1 Equivalent Circuits for Current Vector Along [100]	31
2.5.2 Equivalent Circuits for Current Vector Along [011]	34
2.5.3 Equivalent Circuits for Current Vector Along [010]	36
2.5.4 Equivalent Circuits for Current Vector Along [101]	38
2.5.5 Equivalent Circuits for Current Vector Along [001]	40
2.5.6 Equivalent Circuits for Current Vector Along [110]	42
<b>Chapter 3 APEC 2014 Conference Submission: “Inverter Device Nonlinearity Characterization Technique for Use in a Motor Drive System”</b>	<b>54</b>
3.1 Introduction	54

3.1.1	Motivation . . . . .	54
3.1.2	Outline . . . . .	55
3.2	Study of Nonlinearities . . . . .	56
3.2.1	Nonlinearity Classification . . . . .	56
3.2.2	Requirements on the Procedure . . . . .	57
3.2.3	General Approach . . . . .	57
3.2.4	Experimental Setup . . . . .	58
3.3	Representing the Voltage Disturbance . . . . .	58
3.3.1	Representing the Voltage Disturbance with Direct Current . . . . .	59
3.3.1.1	Analytic Expression of the DC Waveform . . . . .	59
3.3.2	Extension of the DC Representation to AC . . . . .	61
3.4	Methods Utilizing Direct Current . . . . .	62
3.4.1	Method Utilizing the Waveform Mean . . . . .	63
3.4.2	Method Utilizing the Waveform Spectrum . . . . .	64
3.5	Methods Utilizing Alternating Current . . . . .	66
3.5.1	Method Using Developed Algorithm . . . . .	68
3.5.2	Method Using DC Approximation with STFT . . . . .	71
3.6	Conclusions . . . . .	72

<b>Chapter 4</b>	<b>Manuscript for ECCE 2014: “Effects of Detailed Nonlinearity Characterization upon Condition Monitoring” . . . . .</b>	<b>73</b>
4.1	Introduction . . . . .	73
4.1.1	Motivation and Background . . . . .	73
4.1.2	State of the Art . . . . .	74
4.1.2.1	Diagnosis . . . . .	74
4.1.2.2	Prognosis . . . . .	75
4.1.2.3	Fault Tolerant Design . . . . .	75
4.1.2.4	Fault Mitigation . . . . .	75
4.1.3	Aim of This Work . . . . .	76
4.1.4	Outline . . . . .	76
4.2	Inverter Modeling . . . . .	77
4.2.1	Relationship Between Fault and Measured Quantities . . . . .	77
4.2.2	Chosen Example: Bond Wire Lift-Off . . . . .	78
4.2.3	Imposition of Artificial Faults for Simulations and Experiments . . . . .	79
4.3	Diagnosis . . . . .	80
4.3.1	Characterization Diagnosis . . . . .	81
4.3.2	Linear Discriminant Classifier . . . . .	82
4.4	Prognosis . . . . .	87
4.4.1	Thermomechanical Model . . . . .	87
4.4.2	Thermal Model of Inverter . . . . .	88
4.5	Conclusions . . . . .	90

# Chapter 1

## Literature Review

### 1.1 Introduction

The nature of semiconductor devices is such that they have a nonlinear voltage and current characteristic. Coupled with the use of pulsewidth modulation (PWM) to control the current in three phase inverters and the complications associated with this, the result is the distortion of the output voltage of a three phase voltage source inverter (VSI). These phenomena resulting in the distortion of the output voltage of an inverter are termed “inverter nonlinearities.”

Typically because the distortion caused by such nonlinearities is small it is ignored, or maybe only one nonlinearity is mitigated. The case where all are studied or accounted for is rare. There are, however, situations where it is important to understand these inverter nonlinearities. The nonlinearities themselves may contain information about the health of the drive. Diagnosis and prognosis (D&P) studies attempt to take advantage of the information the nonlinearities hold in order to evaluate the condition of the inverter and predict the future health. The use of inverter nonlinearities for D&P has been discussed at various lengths in [1–3].

Inverter nonlinearities, if not mitigated, may have a negative effect upon the operation of sensorless drive schemes. Sensorless schemes, typically using flux and position observers, suffer observer performance degradation in the presence of inverter nonlinearities. The observers must not only take into account the machine model, which is typical, but also that of the inverter nonlinearities. Further, other studies seek to remove the effect of inverter nonlinearities in order to achieve a smoother output voltage. Removing these effects is especially important at low speeds and currents, where the voltage distortion can be significant with respect to the fundamental. Removing effects from voltage applied to the machine can improve the current and



torque controller stability and performance. Discussion of the nonlinear effects, and methods to mitigate inverter nonlinearities have been studied in [4–12]. The problem with not accounting for inverter nonlinearities is clearly seen in situations where the voltage command is used to estimate machine voltage. For instance, in [13] accounting for inverter nonlinearities is used to simplify the characterization procedure by avoiding the use of voltage sensors. This document is concerned with the characterization of these inverter nonlinearities to the end of developing an improved prognostic algorithm.

## 1.2 Discussion of Nonlinearities

The four main inverter nonlinearities discussed in the literature are: deadtime, forward voltage drop, propagation delay (including rise/fall times and gate drive delay), and distortion due to PWM resolution. The two dominant effects are deadtime and forward voltage drop.

### 1.2.1 Deadtime

Inverter deadtime is required because of the limitations of semiconductor devices. When the gating signal is either applied or removed from the IGBT, the IGBT does not immediately close and stop conduction. If another switch were to open in the same phase leg, the result would be a shorted phase leg, called “shoot-through.” The gating signals are therefore delayed to prevent this phenomenon. In Fig. 1.1(a), the ideal gate signals are given, and in Fig. 1.1(b) the gate signals with deadtime are shown. The voltage in 1.1(c) shows the resulting actual voltage waveform in the presence of deadtime, and Fig. 1.1(d) the equivalent phase to neutral voltage. Note that the voltage takes time to turn off, to the right of the second dashed line in Fig. 1.1(d). Without deadtime, if the bottom switch were to be turned on, there would be a short.

When discussing voltage-source inverters, the effect of deadtime upon the voltage output is highly nonlinear, and thus any representative function is highly nonlinear. This is true for any inverter, but this case focuses on three phase voltage source inverters. This nonlinearity in the output voltage is because of the dependence on which device is conducting, and the fact that the effect is nonlinear with respect to each device. The different conducting devices are repre-

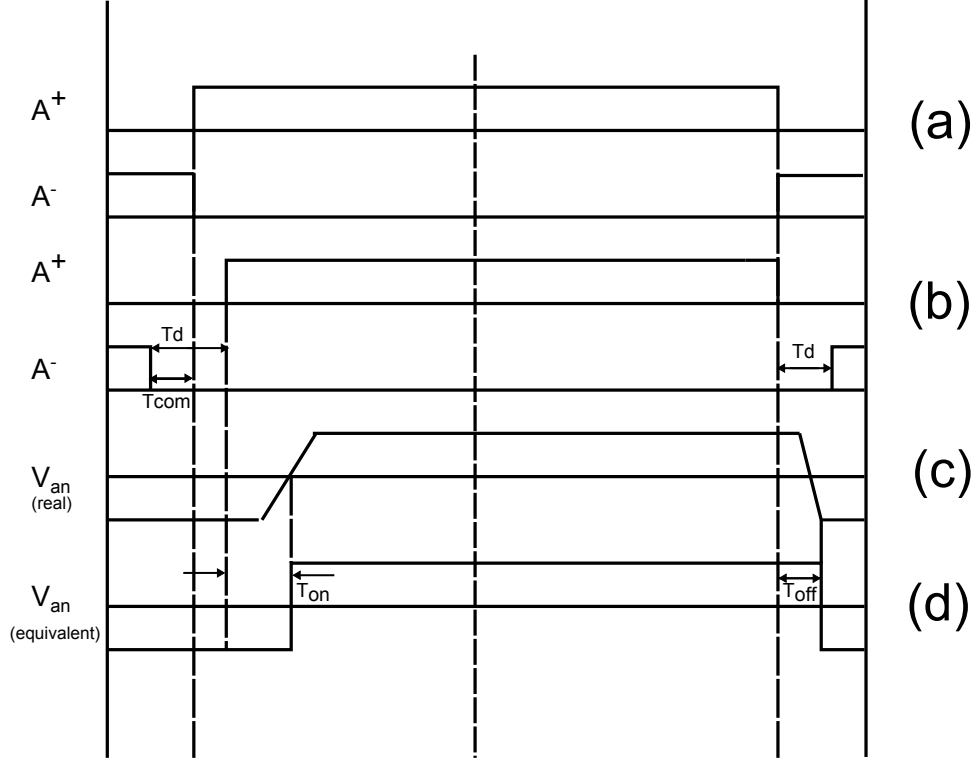


Figure 1.1: Plots showing the implementation of deadtime. (From [10])

sented by the different phasors in the space vector plane. The voltage drops can be thought of as a decrease in each of these three vectors. Essentially, The phase A IGBTs/diodes will only cause voltage attenuation along the positive or negative of this phase A axis. The vector representing the voltage drop due to the deadtime is well-defined and is related to the conducting devices, switching frequency, DC link voltage, and applied deadtime, as shown in equation (1.1). The conducting device dependence is represented by the sign function. The switching frequency is given by  $f_s$ , the the DC link voltage by  $V_{DC}$  and the applied deadtime  $t_d$ .

$$\begin{aligned} \bar{v}_{dt} &= \frac{4}{3} t_d f_s V_{dc} \text{sign}\{\bar{i}\} \\ \text{sign}\{\bar{i}\} &= \frac{1}{2} \left[ \text{sign}\{\bar{i}_a\} + \text{sign}\{\bar{i}_b\} e^{j\frac{2\pi}{3}} + \text{sign}\{\bar{i}_c\} e^{j\frac{4\pi}{3}} \right] \end{aligned} \quad (1.1)$$

To reiterate the understanding of the three phase effect of discrete voltage drop, the  $\text{sign}\{\bar{i}\}$  can be plotted with one rotation of the vector  $\bar{i}$ . This is shown in Fig. 1.2.

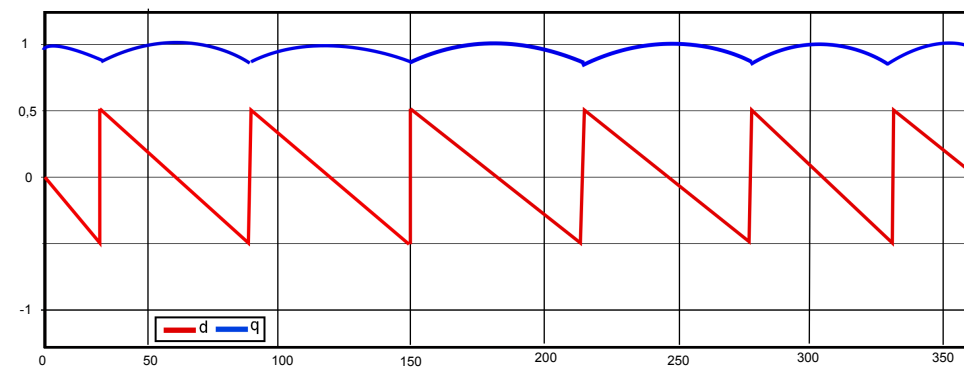
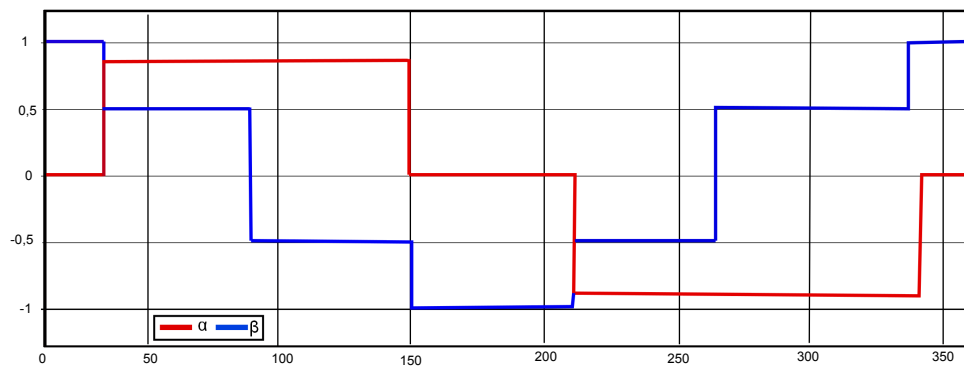
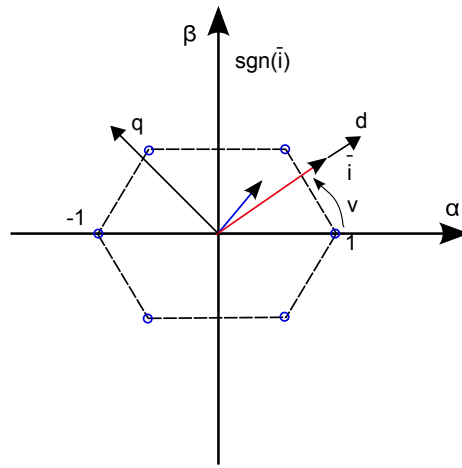


Figure 1.2: Three-phase representation of the sign function in the space vector plane. (From [14])

## 1.2.2 Forward Voltage Drop

The forward voltage drop has two components. The first is the discrete forward junction voltage drop, which is manifested much like the deadtime. In fact, the directionality of the discrete forward voltage drop is the same as the deadtime, so the sign function used to represent the deadtime is also used here. Note that the discrete value of the voltage drop differs between the IGBT and the diode. The second forward voltage drop is the ohmic voltage drop over the device. This behaves as a resistor, and as such, the voltage drop increases as the current increases. The two of these effects are summarized into one voltage error equation, in equation (1.2). A large assumption is that of the voltage drop. Note that in equations (1.3), the forward voltage drop over the diode and IGBT are averaged to one value, the same is applied to the resistance. This allows for the simplification of the characterization procedure but obfuscates which device the voltage drop is truly coming from. This becomes problematic for diagnosis and prognosis because the health of each individual device should be isolated.. Also, this average is only reasonable if the duty cycle is approximately  $D = 50\%$ , or the voltage command is low, and each device (the IGBT and diode of one half-leg) conducts half of the time. The final voltage error, not machine voltage, is given in equation (1.4).

$$\bar{v}_{on} = \frac{4}{3} V_{th} \text{sign}\{\bar{i}\} + R_d \bar{i} \quad (1.2)$$

$$\begin{aligned} V_{th} &= \frac{V_{th,sw} + V_{th,fw}}{2} \\ R_d &= \frac{R_{sw} + R_{fw}}{2} \end{aligned} \quad (1.3)$$

$$\bar{v}_{err} = \frac{4}{3} V'_{th} \text{sign}(\bar{i}) + R_d \bar{i} \quad (1.4)$$

$$V'_{th} = V_{th} + t_d f_s V_{dc}$$

### 1.2.3 Propagation Delay and PWM Resolution

As mentioned prior, in the study of inverter nonlinearities, the effects of deadtime and forward voltage drop dominate. The propagation delay and distortion due to PWM resolution can be problematic, but have a much smaller effect. The propagation delay, seen in Fig. 1.1(c) as the sloping edge of the voltage waveform, mandates the use of deadtime, but even with deadtime can cause a slight change in magnitude if the turn-on and turn-off times differ, or a small change in phase due to the delay between the commanded and output signals. The delay can be more significant if the driving circuit has delay inherent within it. PWM resolution is the ability of the PWM scheme to create the voltage waveform desired. A sufficient switching frequency is required in order to generate a given sinusoidal frequency. The extreme of this would be if the switching frequency were the same as the fundamental frequency, so that only a square wave of varying duty cycle could be applied to the machine. This would result in a great number of harmonics, and distortion of the output voltage signal. In many cases, where the switching frequency is much greater than the fundamental, this is not a problem. In this study only the effects of deadtime and forward voltage drop are discussed, because the delay and PWM resolution issues are not dominating for the reasons given here.

## 1.3 Characterization Methods

The main methods of characterization found were those of [4–6, 14]. [6] discusses an online method to estimate the deadtime inverter nonlinearity, whereas [4, 5, 14] discusses offline or non-loaded methods at standstill. [6] estimates only the effect of deadtime with an adaline observer when the machine is operating with no applied direct axis current. Having an online method would be ideal, but the fact that the method constrains the controller to no direct current ( $i_d = 0$ ), and that the paper with the online method only estimates deadtime, a well defined quantity, makes this method undesirable. In addition, its computation complexity raises concerns about stability in situ. The offline method of [4] uses the voltage command of the current controller and flux observer to estimate the resistance and effect of deadtime. The threshold voltage is found simply with the voltage command from applying a low frequency and low

magnitude sinusoidal current to the machine at standstill (to minimize inductive and resistive drops). The resistance is found from the orthogonal relationship between applied flux and the voltage induced. [5] introduced a method to find a detailed machine model using a standstill DC test. A model of the inverter is built which roughly accounts for the linear and nonlinear effects, or the resistance and voltage drop (deadtime and junction), respectively. The inverter model is arbitrary, as it does not relate exactly to the exact nonlinear parameters, but can be used to develop a model of the inverter. In order to characterize the machine with this model, a range of direct currents are applied to the machine at standstill. This arbitrary model parameters are found with a least squares fit method. [14] uses a method similar to [5], but relates the quantities found from the DC standstill method to the actual nonlinear quantities of the inverter. The paper also utilizes a model, utilizing actual parameters of the machine, to derive the V-I characteristic of the machine. Because of the relationship between the results and the actual inverter nonlinearities, and its accuracy in characterization, this method is chosen for initial testing.

## 1.4 Chosen Characterization Method

The paper by [14] discusses the most model-focused method of inverter characterization. The issue, much like the other issues related to sensorless control, is to characterize the behavior of the inverter in order to more accurately know the voltage command. This paper looks to compensate for the effects of both deadtime and the on-state voltage drops. This method characterizes the inverter with only a current control scheme. A modification to this scheme is used to find the voltage characteristics. A lookup table (LUT) is used to relate the voltage error with respect to the current. The voltage error is in the space vector frame, and as such, the voltage error is a vector value itself, dependent upon the phase current vector value.

The final concept evidenced is the alignment and how it affects the machine equations. The vector equation (1.4) can be decomposed into its two dimensional value as in equation (1.6). This can be either the rotor oriented or the stator oriented axes,  $\alpha\beta/DQ$ . This holds for the sign functions in equation (1.5). If the machine  $D$  axis is aligned to the  $\alpha$  axis, then a current

applied in  $D$  will result in only  $\alpha$  current. This can be used to simplify the stator equations if only  $D$  current is applied. The simplification is useful for two reasons. First, only one half of the equation needs to be used, and the equation can be simplified into a scalar value function. Secondly, the alignment simplifies the sign equation so that only the  $\alpha$  axis has a voltage drop in it. This can be used to obtain the result of equation (1.6).

$$\text{sign}(\bar{i}) = \frac{1}{2} \left[ 1 - e^{j(2\pi/3)} - e^{j(4\pi/3)} \right] = i_\alpha + j i_\beta \quad (1.5)$$

$$\bar{v}_{err} = v_{err,\alpha} + j0 = \frac{4}{3} V'_{th} + R_d i_\alpha \quad (1.6)$$

With these concepts in place, the V-I characteristics of the IGBTs are derived. Note that for the previous assumptions only the average drop can be found for any device. This assumption will have to remain until later when further analysis can be performed. The machine is first aligned such that the  $\alpha$  and  $D$  axes are aligned. The resistance is found by applying two  $\alpha$ -axis currents and measuring the voltages induced at these applied currents. Manipulation of these equations will result in the resistance for the machine windings and inverter.

$$V_\alpha^* = \frac{4}{3} V'_{th} + (R_d + R_s) I_\alpha \quad (1.7)$$

$$R_d + R_s = R'_s = \frac{V_\alpha^*}{I_{test}} = \frac{V_{\alpha,2}^* - V_{\alpha,1}^*}{I_{test,2} - I_{test,1}} \quad (1.8)$$

The value of resistance should be found near the rated current. Therefore the two  $\alpha$ -axis currents must be near the rated current. The voltage should be measured after some time (the end of the pulse, before zeroing) to reduce the acquisition of any transients.

With this known, the voltage error due to the rest of the voltage distortion can be found. This is used to find the voltage distortion from the deadtime and the forward voltage drop of the device for all currents. Note however that because we know the voltage drop over the resistor and deadtime analytically, we can determine the forward voltage drop term. The equations for this are as follows, found for a stepped ramp of current in the  $\alpha$  axis. The value 'k' is an index which relates the value of current applied to the resulting voltage.

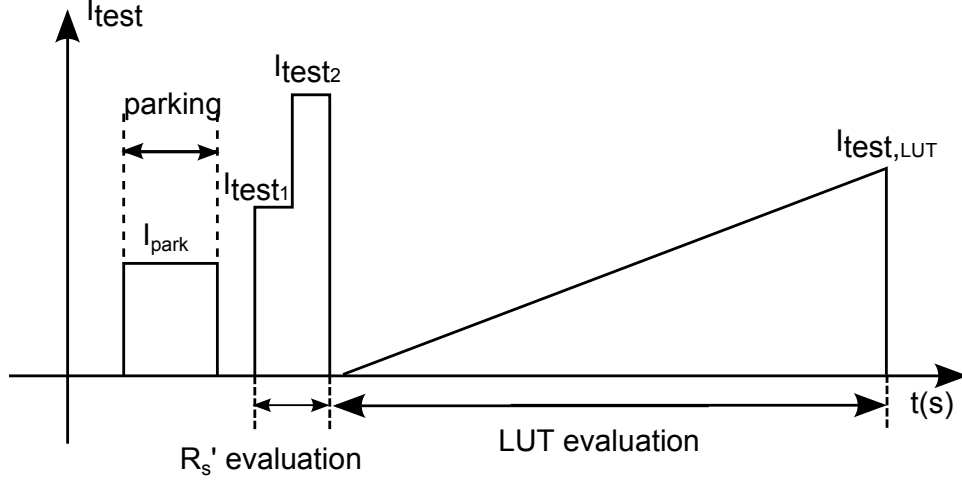


Figure 1.3: Three steps of the testing procedure. (From [14])

$$V_{\alpha}^*(k) = \frac{4}{3} V'_{th} + R'_s I_{\alpha}(k) \quad (1.9)$$

$$V_{err,indexed}(k) = \frac{3}{4} [V_{\alpha}(k)^* - R'_s I_{\alpha}(k)] \quad (1.10)$$

The three steps of this characterization procedure are shown graphically in Fig. 1.3.

This method is generally appropriate for measuring the average drop over a device. This is helpful in condition monitoring. The benefit of this is its simplicity in experimental procedure and detailed results. The detriment is the reliance on voltage sensors and length of the characterization operation. The data must be stored in a large lookup table (LUT) and does not take into account the temperature. Also, the resistance step is redundant with respect to the final stepped ramp. Further, the parking and alignment can become problematic. In operating, the alignment is not always easily possible, and the parking may not actually be able to align the machine even if it could, due to the cogging alignment being different than the magnetic alignment which will result in an error in the calculations.

#### 1.4.1 Details of Method of Choice

The method in [14] was chosen. In order to avoid the problem of cogging torque and alignment, an induction machine is to be used. The temperature will be addressed by measuring the temperature of the drive during data gathering, but the initial tests will be done with the machine



heated up. Voltage sensors are used and a detailed data acquisition system is to be used to allow for a maximally detailed inverter characterization. Alongside this, a simulation has been developed in order to test the applicability of the method.

## **1.5 Conclusion and Future Work**

This document discusses the review of literature in the study of inverter nonlinearities. Improvements in sensorless control schemes and health monitoring are the two main motivations for this study. The papers typically discuss inverter nonlinearities to the end of one of those goals. The main nonlinearities are those of deadtime and forward voltage drop. Some characterization methods found from literature were discussed, and one was chosen as a starting point for the research project. Finally, the application specifics of this method were discussed.

There are some problems with the method that lend themselves to future work. The fact that the method does not distinguish between the diode and IGBT forward voltages is problematic. It is possible that finding the voltage drop while changing the duty cycle so that it is not near 50% will be able to solve this. Such a method would allow for the distinction between diode and IGBT voltage drop. Gathering data at multiple temperatures would also be helpful. This can be accomplished by characterizing once, and then once again (since the machine will then be heated). An online method would be helpful, and will be attempted given time, once the first method is proven. Finally, the use of this characterization in a prognostic algorithm is seen as a long term goal in this project, but requires further study.

# Chapter 2

## Characterization Investigation Results

### 2.1 Introduction

The ability to understand and calculate inverter nonlinearities can serve many purposes. Most notably, it was mentioned that knowledge of the inverter nonlinearities can be used to correct for distorted inverter AC output voltages, or to track the condition of the inverter [2, 4, 10]. When studying these nonlinearities for any purpose, it is important to define what nonlinearities are important for the application. The most pronounced nonlinearities – due to available hardware sensors – are the forward voltage drop and resistance of the inverter semiconductors (i.e. IGBT and diode). There exist other device ‘characteristics’ which may be studied, including the gate current ( $i_g$ ) and gate-emitter voltage ( $V_{GE}$ ), however it is uncommon to sense the gate characteristics. The goal is therefore to find the voltage drop over the collector to the emitter pathway of the semiconductor devices. As it was alluded to, there are four characteristics in all: The resistance ( $R_d$ ) and forward biased junction voltage ( $V_{th,d}$ ) over the diode, and the resistance ( $R_i$ ) and forward biased junction voltage ( $V_{th,i}$ ) over the IGBT. Any characterization procedure to find these parameters should also allow for finding the parameters of every device. In addition, being able to find these characteristics online allows for the use of the values to making controller adjustments, and in condition monitoring algorithms (i.e. estimating remaining useful life).

With this in mind, the task then becomes one of finding the best method of characterization. The previous literature review discussed methods to characterize the inverter, but many could not isolate specific device quantities, such as [14]. In this study, the proposed characterization method seeks to isolate both quantities ( $R$  and  $V$ ) for each device. To do this, new

characterization methods have been developed to improve upon the weaknesses of the methods from literature. The methods approach the problem analytically and algorithmically. The algorithmic method finds the characteristics of the inverter when applying alternating current by observing the voltages and currents. The analytical method works with the application of direct currents by finding two equations to solve for both of the two unknowns,  $V_{igbt}$  and  $V_{diode}$ , using sensed current, voltage, and applied duty cycle. To get the voltage for multiple direct currents, multiple direct currents must be applied. The final goal of any characterization method is to measure the voltage and current relationship for each device. The resistance and forward junction drop for each device can be found from this voltage and current relationship.

The methods assume that voltage and current sensors are available for all phases, as well as a DC link voltage sensor as in Fig. 2.1. Additionally, the methods require a sampling rate above the switching frequency, as the PWM voltage waveform is required for the calculation of the device characteristics. Following the Nyquist rate requirement, the sampling frequency must be greater than twice the signal bandwidth. With filtering of harmonics greater than the first AC harmonic, a sampling rate of only just over the first fundamental harmonic is required. A sampling frequency of 100kHz for a switching frequency of 5kHz is assumed in simulation, and used in experimentation, which is more than required. An induction machine is used for all experimental and simulation results, and operated at standstill for all simulations and experiments.

This report is organized into four sections: introduction, DC method, AC method and conclusion. The DC method in section 2.2.1.1 discusses the first method attempted. Simulations and experimental results are used to demonstrate that this method is not viable. The second DC method in section 2.2.1.2 attempts to use RMS, but also required the mean, a value subject to too much noise, and thus this method is not explored. The third and final DC method in section 2.2.1.3 uses the fourier spectrum of the PWM voltage waveform to find the device voltage drop, and this nonlinearity. The third portion, given in section 2.3, is the AC method section. An algorithmic approach is used to determine the device nonlinearities. In the conclusion, the methods are summarized and commented on.

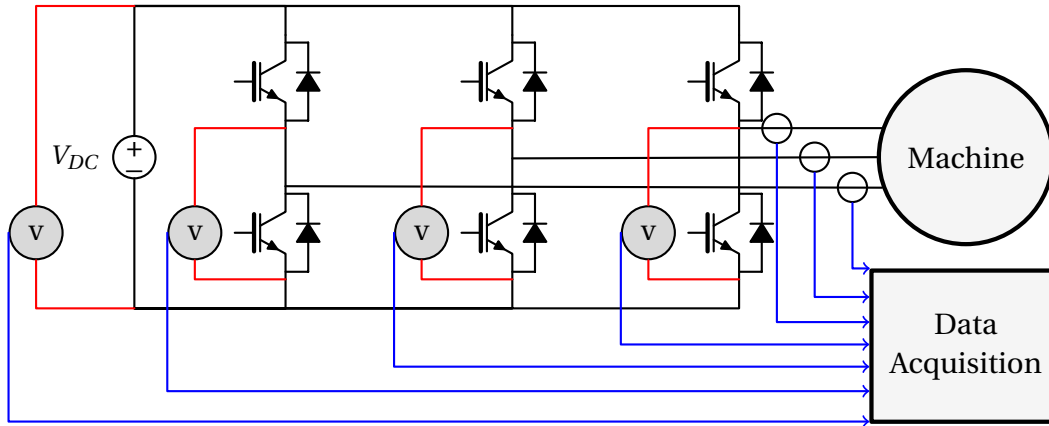
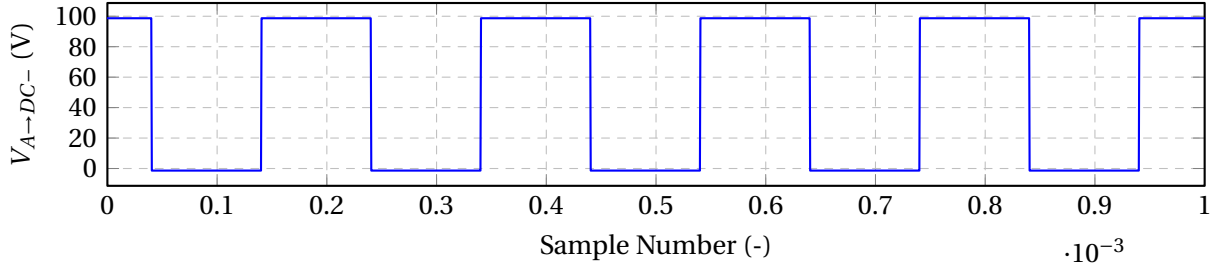


Figure 2.1: Experimental setup for inverter characterization.

## 2.2 Characterization of an Inverter with Applied Direct Current

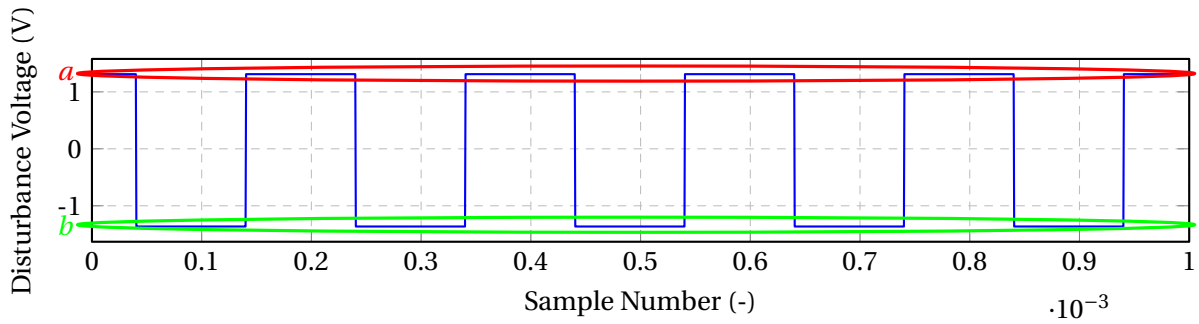
### 2.2.1 Characterization with $V_\phi \rightarrow V_{DC-}$

Assuming the sensors in Fig. 2.1 are available, it is possible to extract the nonlinearity from the PWM waveform of the measured phase voltage. If the voltage with respect to the negative DC link and DC link are measured, all appropriate information is available. The nonlinearity can be represented by a square wave with two different values, one near zero representing the bottom device conducting, and another near the DC link voltage. By subtracting the portion of the square wave that has a value near the DC link value from the measured DC link voltage (i.e.:  $V_{dist} = V_{DC} - V_{A \rightarrow DC-}$ ), the actual nonlinear disturbance voltage is found. This process is illustrated in Fig. 2.2. Note that the values come from the fact that the phase A half bridge of the inverter takes the form of Fig. 2.3. When the IGBT is conducting, the voltage sensor, here represented by  $v_s$  measures the voltage across the bottom diode, which is the DC link voltage less the voltage drop over the top IGBT. Thus, from this voltage and the DC link voltage, the IGBT voltage is found. Conversely, while the diode is conducting, the voltage measured by the sensor is the forward voltage drop of the IGBT. This nonlinear disturbance voltage is shown by the top plot of Fig. 2.4. To correct even further, it is possible to remove the voltage distortion due to the deadtime. This is assumed to be in the overall forward voltage drop, but can be easily removed with the well-defined deadtime voltage distortion equation in the literature review document.



(a) Voltage disturbance with a high sampling rate.

for  $(V_{A \to DC-} \approx V_{DC}) \rightarrow V_{dist} = V_{DC} - V_{A \to DC-}$



(b) Voltage disturbance with a high sampling rate.

Figure 2.2: Extraction of the disturbance waveform from raw  $V_{A \to DC-}$ .

The top nonlinear disturbance waveform in Fig. 2.4 is shown with the ‘a’ quantity representing the IGBT voltage and the ‘b’ quantity representing the diode voltage at a given operating point. The data in the top figure has a very high sampling rate, much higher than is typically available in an inverter drive system. In order to make the analysis more realistic, the sampling rate is reduced in the middle subfigure of Fig. 2.5. The fourier series is shown for this simple waveform for later use in the spectral method.

Additionally, when discussing inverter characterization, the current paths should be made clear, to help in understanding the characterization for each device. Note that in Fig. 2.5 there are four arrows, two pointing toward the center and two pointing away from the center. Those pointing towards the center show the path of current when a positive A-phase current is applied. In this case, the top IGBT and bottom diode conduct. The diode of course conducts in a

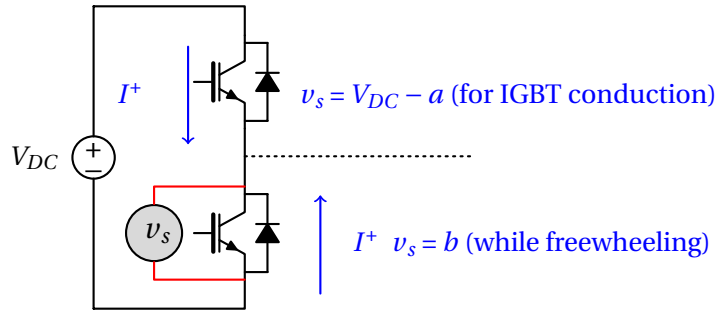
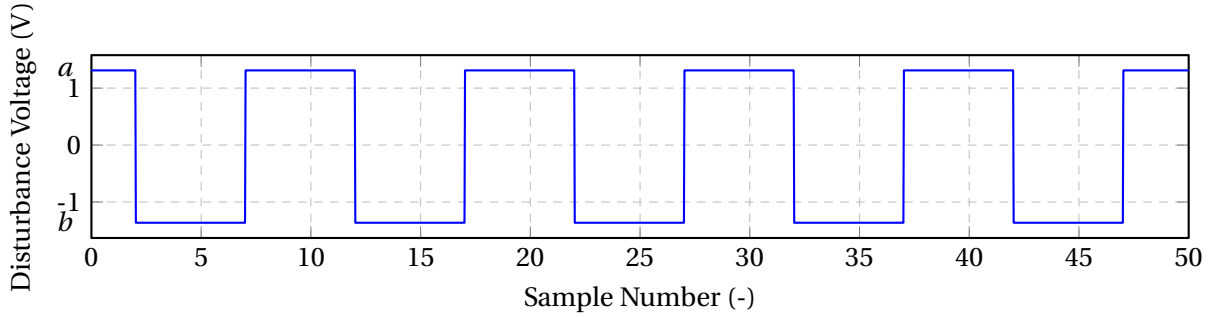


Figure 2.3: The phase A half bridge of the inverter, showing the sensor connection. The purpose of this figure is to demonstrate the paths of current, and how they relate to the voltage measured by the voltage sensor.

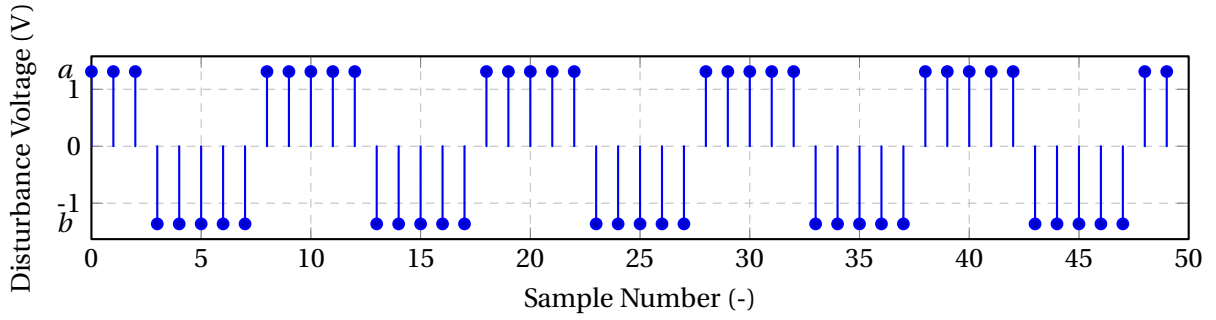
“freewheeling” fashion. Therefore when analysis is done, only those two devices can be characterized, since they are the only active devices in the leg. When the top IGBT is conducting, the bottom diode is blocking the voltage from the DC link less a small voltage drop due to the IGBT. When the diode is conducting, the voltage sensor will only sense the voltage over the diode, as the sensor is applied directly across this device. To characterize the complementary devices – the diode on top and the IGBT on the bottom – a negative current must be applied for any DC method.

### 2.2.1.1 Method 1: Dual Duty Cycle Mean Calculation Method

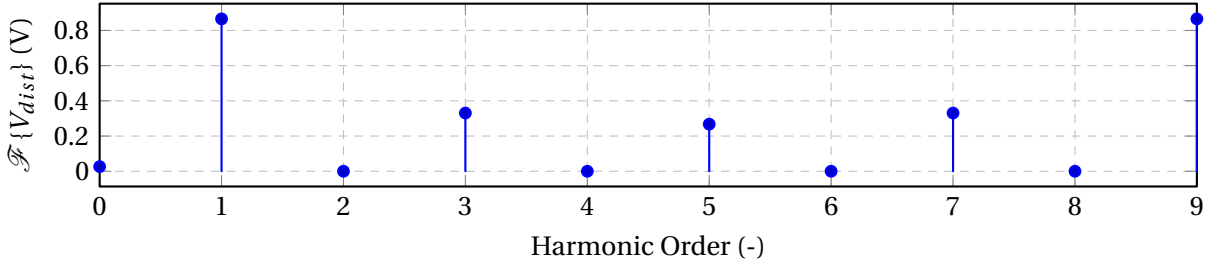
The first DC method from section 2.2 takes advantage of the PWM voltage waveform with knowledge of the duty cycle from the controller output. If the duty cycle is fixed, the voltages can be measured and calculated, resulting in the first two equations in 2.1. By measuring at the same current but two different duty cycles (i.e. this was done by offsetting all by 5% in the second case), the two equations can be subtracted from one another to derive an expression for the voltage drop over the two devices, given by equation 2.3. The method is applied to both simulated and experimental data in Figs. 2.6 and 2.7, respectively.



(a) Voltage disturbance with a high sampling rate.



(b) Voltage disturbance with a low sampling rate.



(c) Fourier transform of voltage disturbance.

Figure 2.4: Waveform approximation to the disturbance at high (MS/s) and low (100kS/s) sample rates.

### 2.2.1.1.1 Derivation

$$\begin{aligned} \mu_{x_1} &= \frac{1}{1-x_1}(b) + \frac{1}{x_1}(a) \\ \mu_{x_2} &= \frac{1}{1-x_2}(b) + \frac{1}{x_2}(a) \end{aligned} \tag{2.1}$$

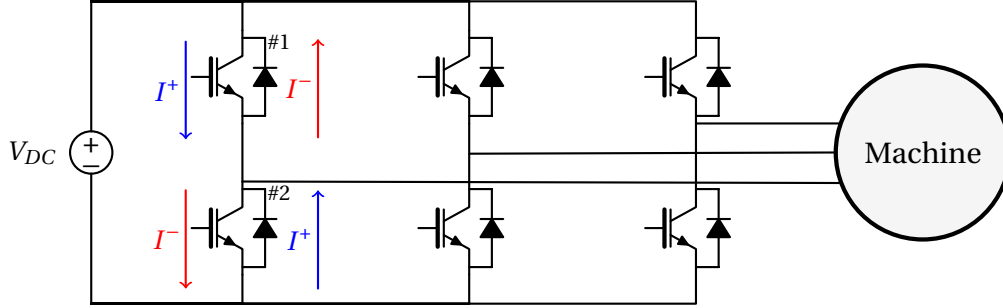


Figure 2.5: Inverter showing the inverter device current paths.  $I^+$  represents the positive current device path, and  $I^-$  represents the negative current device path.

$$\begin{aligned} \frac{x_2}{x_1}(\mu_{x_2} &= \frac{1}{1-x_2}(b) + \frac{1}{x_2}(a)) \\ -(\mu_{x_2} &= \frac{1}{1-x_2}(b) + \frac{1}{x_2}(a)) \end{aligned} \quad (2.2)$$

---

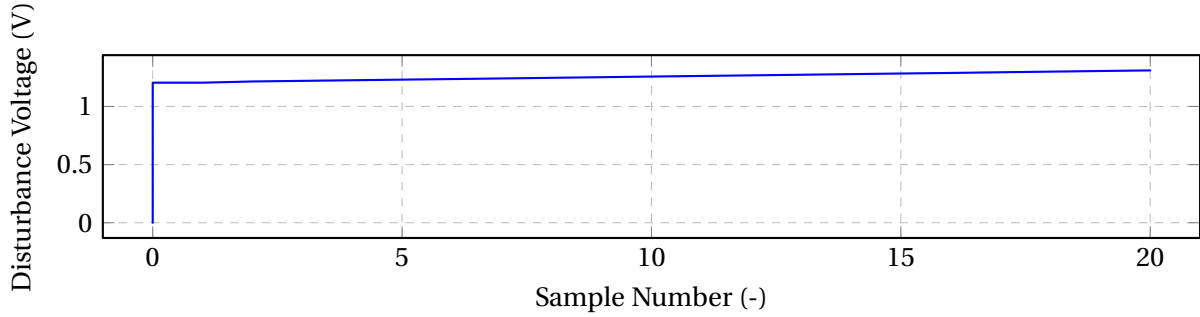

$$\frac{x_2}{x_1}\mu_{x_1} - \mu_{x_2} = (b)\left(\frac{x_2(1-x_1)}{x_1} - (1-x_2)\right)$$

$$\begin{aligned} b &= \frac{\frac{x_2}{x_1}\mu_{x_1} - \mu_{x_2}}{\frac{x_2(1-x_1)}{x_1} - (1-x_2)} \\ a &= \frac{\mu_{x_1} - (1-x_1)b}{x_1} \end{aligned} \quad (2.3)$$

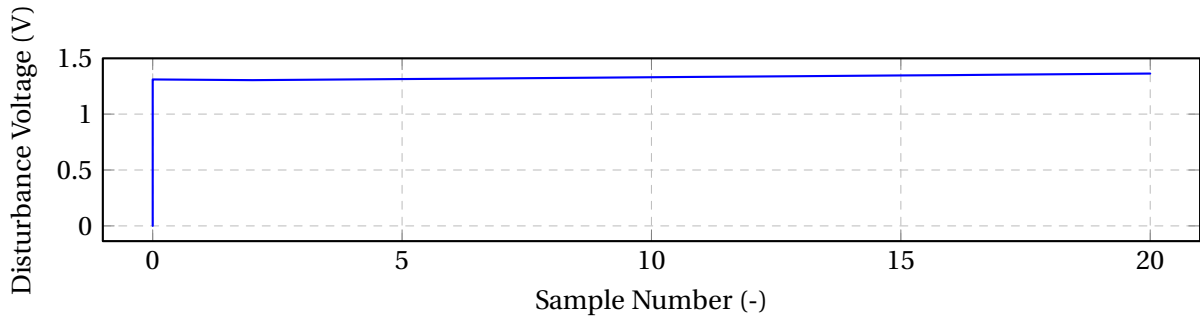
- $a > 0, b < 0$
- $0 \leq x_1, x_2 \leq 1$
- $\mu_{x_1} = \overline{v_{dist,1}}$
- $\mu_{x_2} = \overline{v_{dist,2}}$

**2.2.1.1.2 Simulation** The simulation extracts the V-I characteristic perfectly, and is shown in Fig. 2.6.





(a) Voltage disturbance with a high sampling rate.



(b) Voltage disturbance with a low sampling rate.

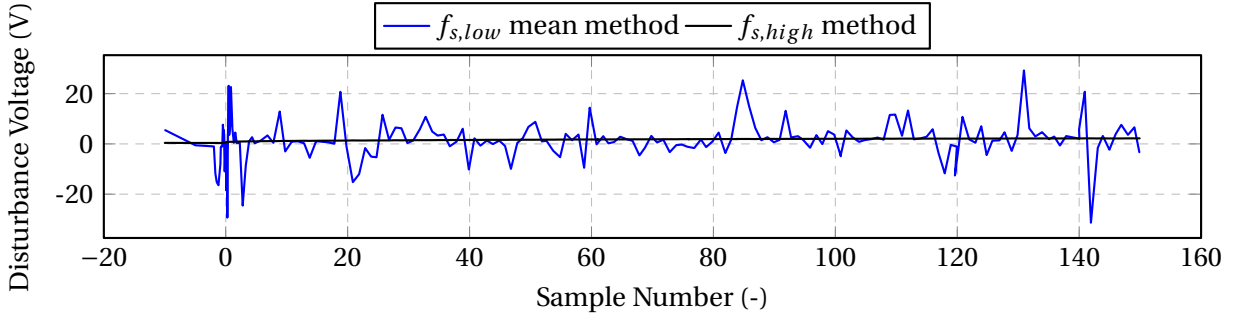
Figure 2.6: Waveform approximation to the disturbance at high (2MS/s) and low (100kS/s) sample rates.

**2.2.1.1.3 Experimental** The method performs poorly with low frequency data. The high frequency data was found by observing the peaks of the PWM waveform.

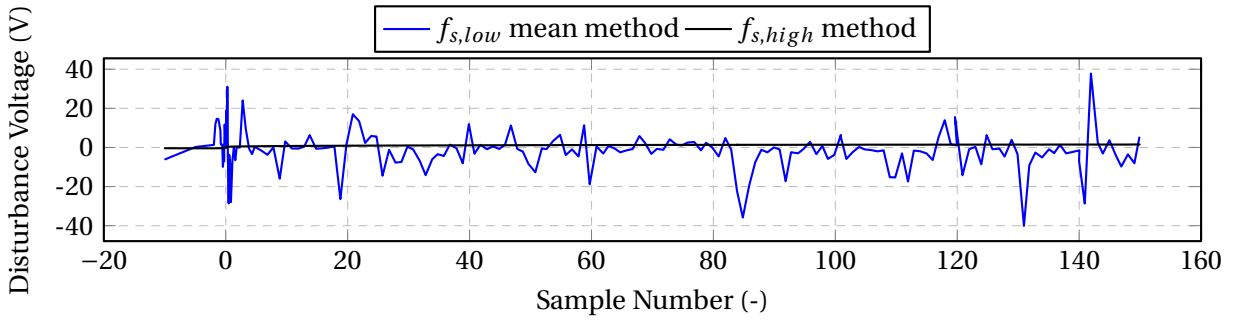
The method performs well in simulation, but noise in the experimentally measured voltage data greatly distorts the results. While this method is computationally and conceptually simple, the fact that noise affects the mean, and thus widely affecting the results, is problematic. Further, this requires results from two experiments, or at least some modification to the controller accompanied by two measurements, to change the duty cycle. Any chosen method should avoid changes the controller.

### 2.2.1.2 Method 2: Mean and RMS Calculation Method

The next approach taken was to find the device parameters with only one experiment, and no controller modifications. With two unknowns, two equations needed to be found which can be used to relate the machine quantities to the measured data. The use of RMS was suggested as a



(a) Voltage disturbance with a high sampling rate.



(b) Voltage disturbance with a low sampling rate.

Figure 2.7: Waveform approximation to the disturbance at high (2MS/s) and low (100kS/s) sample rates.

possibility. This would allow for both the calculation of the RMS and mean, and from this ‘a’ and ‘b’. To do this, an expression for the PWM waveform needed to be developed for a constant duty cycle waveform. This is given as just a sum of two step functions as in equation 2.4. Using this PWM model and applying the general RMS equation, the equation for the RMS of a constant duty cycle waveform is found.

### 2.2.1.2.1 Derivation

$$x[n] = au[n] - (a - b)u[n - (DN + 1)] \quad x[n + N] = x[n] \quad (2.4)$$

$$\begin{aligned}
RMS &= \sqrt{\frac{1}{N} \sum_{n=0}^{N-1} x^2[n]} \\
RMS_{v_{dist}} &= \sqrt{a^2 + (a-b)^2 \left(1 - \frac{2N_1+1}{N}\right) + -2a(a-b) \left(1 - \frac{2N_1+1}{N}\right)}
\end{aligned} \tag{2.5}$$

This solves the controller modification and multiple experiments problem, but the same noise issues from the mean are present. Further, the expression for RMS is not a trivial equation. For these reasons, this method was not explored.

### 2.2.1.3 Method 3: DFT Spectral Method

Instead of the mean duty cycle and RMS methods, the fourier transform was used to generate two equations. Assuming the noise occurs at higher frequencies, finding the Fourier coefficients at a few lower frequencies can allow for the calculation of the device nonlinearities. Using the step function model, a calculation to find ‘a’ and ‘b’ was developed. The fourier series of the PWM signal of fixed duty cycle is given in equation 2.6. This allows for the development of an equation which can use the Fourier coefficients – found from any FFT algorithm, perhaps the Cooley-Tukey algorithm – to find the “a” and “b” quantities.

#### 2.2.1.3.1 Derivation

$$\begin{aligned}
x[\hat{k}] &= \frac{1}{N} \sum_{n=0}^{N-1} x[n] e^{-2\pi i \frac{kn}{N}} \\
x[\hat{k}] &= \left(b + \frac{a-b}{N} (2N_1+1)\right) \delta(k) + \frac{(a-b)}{N} \sum_{k=1}^{N-1} \frac{\sin\left(\frac{2\pi k(N_1+0.5)}{N}\right)}{\sin\left(\frac{\pi k}{N}\right)}
\end{aligned} \tag{2.6}$$

Therefore, the square wave values ‘a’ and ‘b’ can be found with a four step calculation:

- STEP 1: Calculate the FFT with a fast, efficient algorithm (perhaps the Cooley-Tukey algorithm)

- STEP 2: Calculate:

$$(a - b) = (N)fft(1) \frac{\sin(\frac{\pi}{N})}{\sin(\frac{2\pi}{N}(N_1 + 1/2))} \quad (2.7)$$

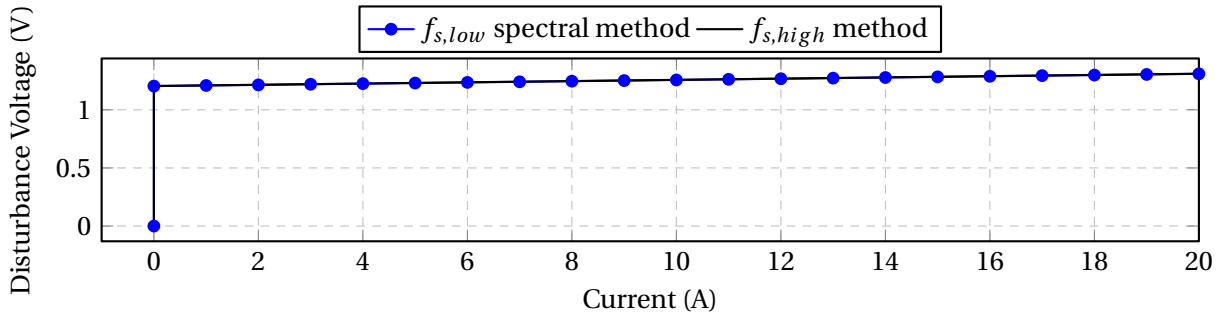
- STEP 3: Calculate 'b'

$$b = fft(0) - \frac{(a - b)}{N}(N_1 + 1) \quad (2.8)$$

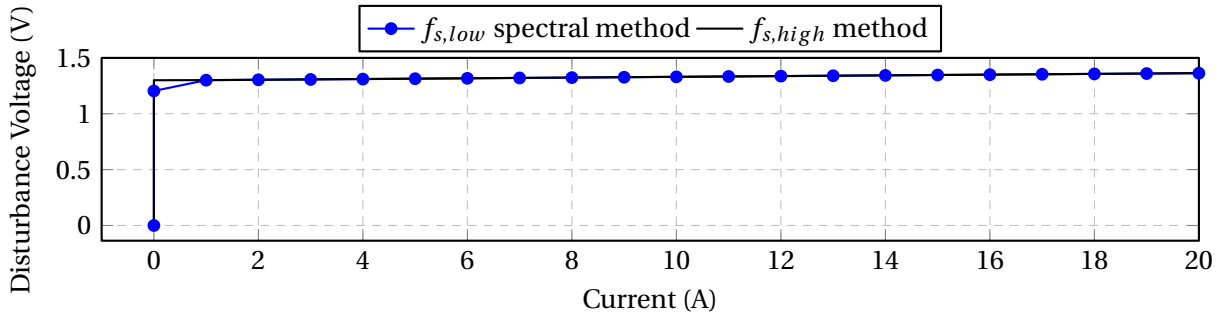
- STEP 4: Calculate 'a'

$$a = (N)fft(1) \frac{\sin(\frac{\pi}{N})}{\sin(\frac{2\pi}{N}(N_1 + 0.5))} + b \quad (2.9)$$

**2.2.1.3.2 Simulation** The simulation results for this method show excellent performance, both for low and high frequency sampling rate data.



(a) IGBT characteristic curve.

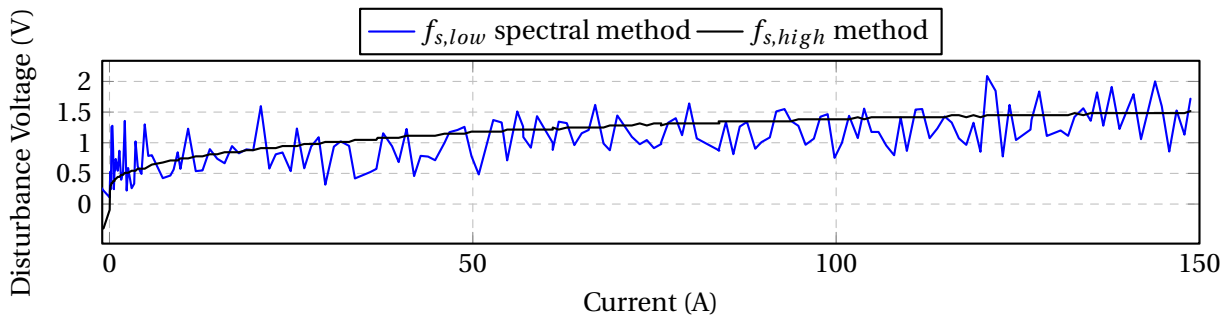


(b) Diode characteristic curve.

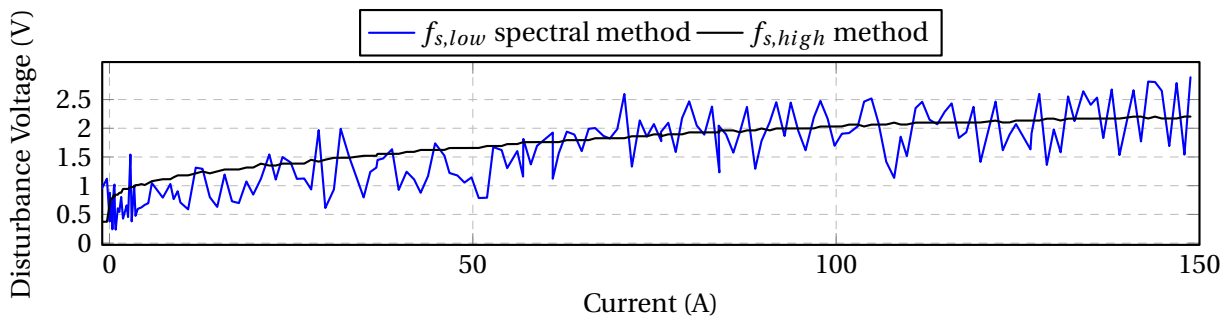
Figure 2.8: Simulation results for nonlinearity voltage drop spectrum extraction.

**2.2.1.3.3 Experimental** The method also shows good performance when applied to experimental data, although the method has noise. The calculation with low frequency data is centered around the actual parameter found from observation of the high frequency waveform.

- Measured using induction machine up to 150A



(a) IGBT characteristic curve.



(b) Diode characteristic curve.

Figure 2.9: Experimental results of nonlinearity voltage drop spectrum extraction,

While this method does show moderate noise, the adequate performance and online capability demonstrates the promise of this method. Unfortunately, it does require the computation of the FFT in the inverter. However, it does not require multiple experiments or controller modifications, is immune to high frequency noise, and gives an easy closed form solution for the device voltage once the FFT is computed.

## 2.2.2 Characterization with $V_\phi \rightarrow V_\phi$

While effective, sensors which measure the phase voltages with respect to the negative DC link voltage are not always available. Thus, modifications must be made which can address the prac-

ticality of this method. Further, the neutral point is not always available in electric machines, and further, three phase inverters do not typically have an interface to the neutral. In most inverters, either the phase voltages with respect to the grid neutral, or the interphase voltages are known. A method using the latter sensor locations over the former is preferable. If no sensors are on the inverter – for characterization purposes – it is assumed that sensors are added. So this section investigates the use of realistic voltage sensors for the detection of inverter nonlinearities. Note that either the use of interphase or phase voltages is equivalent, since one can be calculated from the other as in equation (2.10). With this in mind, the characteristics of a three phase voltage source IGBT inverter are found.

$$\begin{aligned}
 V_A &= \frac{2}{3}V_{AB} - \frac{1}{3}V_{BC} \\
 V_B &= V_A - V_{AB} \\
 V_C &= V_B - V_{BC}
 \end{aligned}
 \tag{2.10}$$

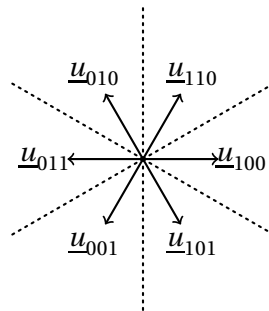


Figure 2.10: Voltage vectors of tests.

The equivalent circuit of the inverter was implicit in the previous analysis, and assumed that each device had an independent relationship between its voltage and current. Finding the voltage values with respect to current can be done by solving the inverter circuit in Fig. 2.13 given that different current vectors are applied. To get the parameters, multiple currents were applied to the machine and information gathered with measurements, and the changing voltage to current relationship (V-I) was found. Since the V-I was determined by direct measurement of the device, the problem was only of finding the best method to determine this. When lacking di-

rect measurement, this problem becomes a slightly more complex one of system identification. Without direct measurement, the equations from before become more complex, and more tests to get the required number of equations for the same number of unknowns is necessary (one equation per unknown is required). This is further complicated by the fact that this equation-unknown method requires that the unknowns be constant; the constant requirement is not fulfilled by looking to find this voltage component. If a device had different current, each device would introduce another unknown. Luckily, the V-I relationship of each device can be approximated by two constant, a voltage source and resistor. For proper modeling, an ideal switch and diode is required for each respective IGBT or diode; this equivalent circuit is shown in Fig. 2.14. These values are constant, allowing us now to find the relationship between these constant values, and measurements taken during multiple tests. Tests are performed by applying current vectors along the 6 fundamental directions: [100], [011], [010], [101], [001], and [110]. The appropriate representative circuits are found for each current vector applied. Note that the current in each direction is controlled, so the voltage vector will alternate between between [100] and [011] (as well as [111]/[000]) for the [100] current vector case. In this case however, since the current is always positive, only the top IGBT and bottom diode (freewheeling mode) will conduct. It is important that the current applied be DC and the current be twice that which is required to be in the saturation region of the IGBT, to assure that the resistance is constant. This method will allow for the determination of constant parameters in the face of varying currents.

With the equivalent circuit and its resistive and voltage components, a method is then developed in order to find these resistances and voltages by the use of multiple tests. The method can use the equivalent circuit to build a model as well as the voltage of the DC link, phase voltages and phase currents. Two circuits can be found for each of the tests, or operation modes, representing the primary conduction through the IGBT and the freewheeling conduction through the diodes which is present in all machines due to their inductive nature. Two equations can be found for each circuit using KVL on the two resulting loops. With the machine at standstill, the same fundamental voltage vector is used to control the current in that vector direction, too. Doing this for all six fundamental vectors allows for the derivation of 24 equations for the 24 unknowns in Fig. 2.14. This analysis is investigated in Appendix 2.5, with the resulting matrix

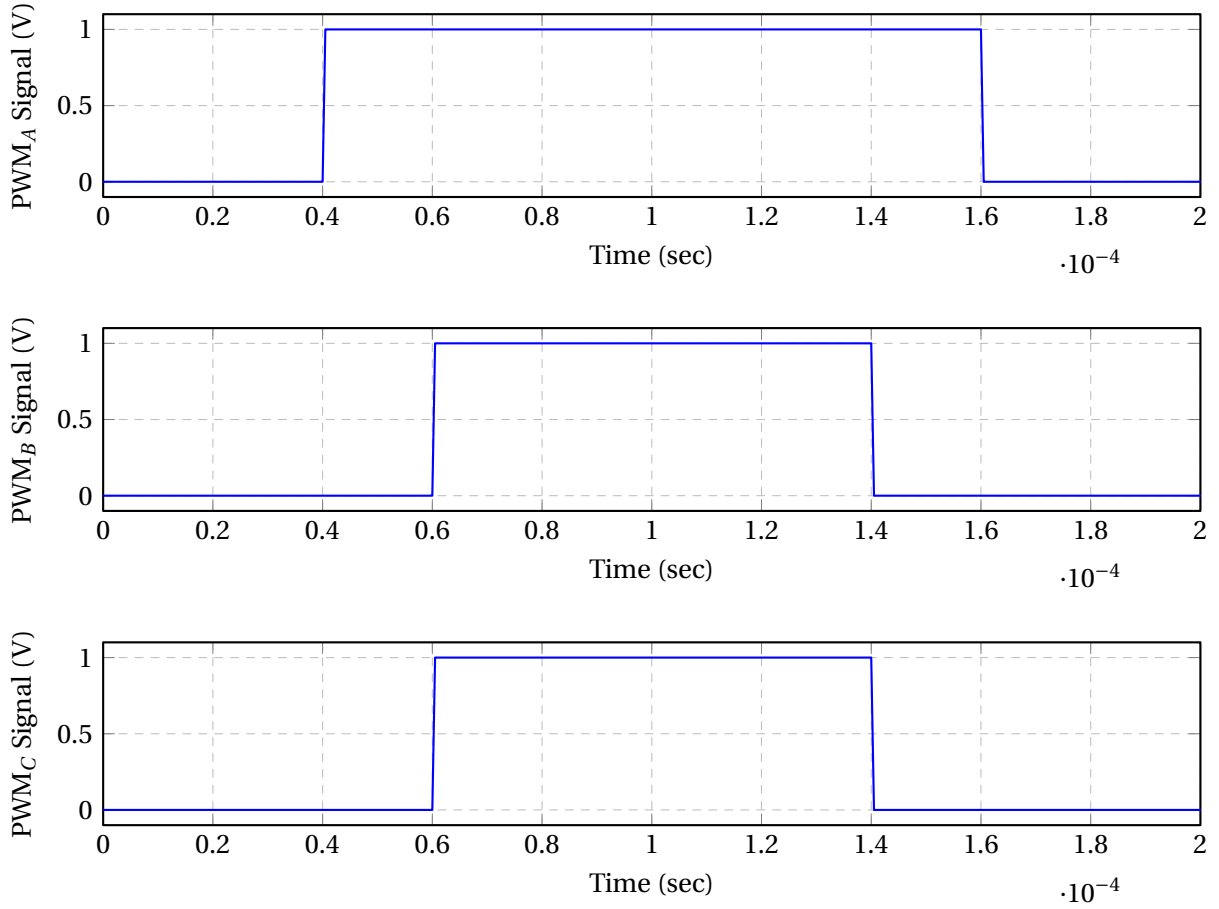


Figure 2.11: Waveforms for ideal PWM signals for a Duty cycle command of <60%,40%,40%>.

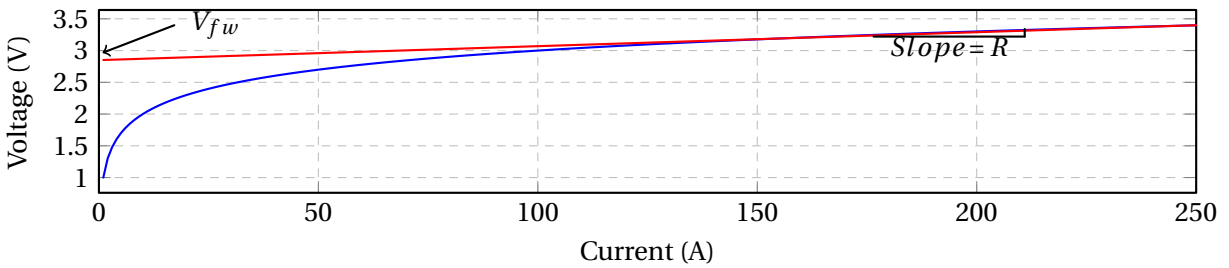


Figure 2.12: Waveforms showing a generalized semiconductor nonlinearity, given as its VI characteristic and the linear approximation to this with its equivalent parameters.

given by equation 2.11. This is the relationship used to derive the device parameters.

$$x = A^{-1}b \tag{2.11}$$



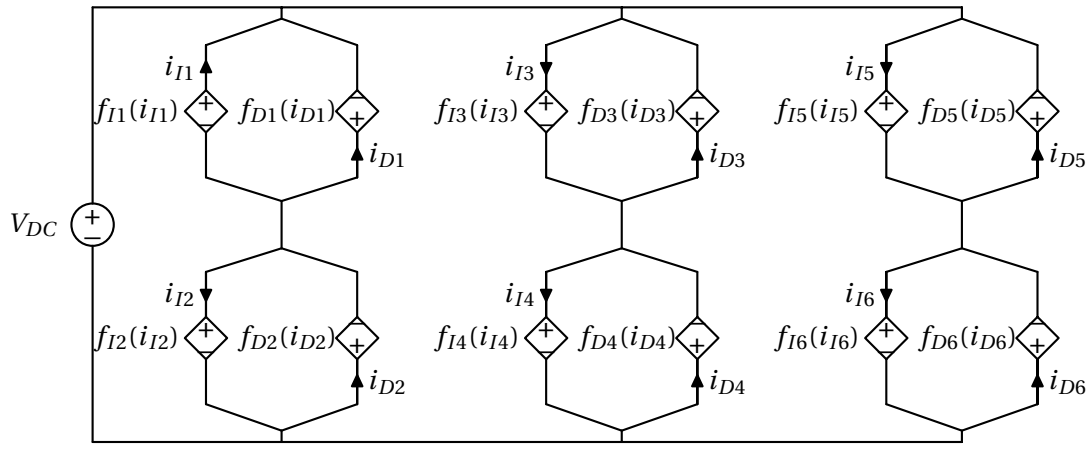


Figure 2.13: Inverter showing the inverter devices' voltage representation.

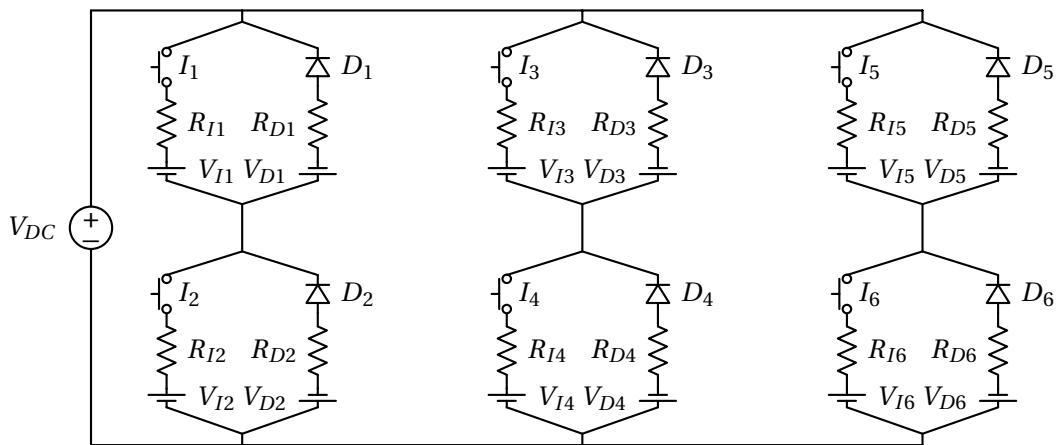


Figure 2.14: Inverter showing the inverter devices' idealized equivalent circuits.

This approach however results in a matrix which is not full rank. For this method to be viable, the matrix should be full rank. Appendix 2.5 ends by showing that equation 2.39 depends on equations 2.75 and 2.111, equation 2.66 depends on equations 2.30 and 2.102, equation 2.93 depends on equations 2.57 and 2.21, and equation 2.120 depends upon equations 2.48 and 2.84.

## **2.3 Characterization of an Inverter with Applied Alternating Current**

Application of the spectral method to the alternating current case is nontrivial. Calculation of the fourier series of an AC pwm waveform often involves complex functions, like the use of bessel functions, or information on switching times of the inverter with different current levels, and is thus impractical for DSP or microcontroller use. [15–17] Instead, the direction of current and voltage levels will be used to observe the voltage with respect to current, and averaged to find the current and voltage relationship.

In Fig. 2.15, the nonlinear disturbance voltage of phase A is shown respect to the current. Note that again, the DC link voltage has been subtracted out where it is appropriate. In this waveform, we have voltages when the current is in both directions, so we can characterize the top and bottom IGBTs, as well as their respective freewheeling diodes. Additionally, the voltage, either positive or negative, allows us to isolate the IGBT and the diode from one another. The fact that we have all of this with respect to current allows us to, for each point, associate the voltage disturbance with the current in the device. If values of the current are associated with their respective voltage values, a model can be easily constructed for each device. In implementation, only integer valued currents are stored, by rounding all current readings to the nearest integer (this reduces the number of points in the model). Then, the voltage associated with that rounded current value is added, with a mean calculation, to the running mean calculation for that current. The flowchart in Fig. 2.16 shows the path to find the appropriate voltage with respect to current. The inverter can be characterized by one alternating current point, if a sinusoidal current of peak amplitude is applied (which is the maximum peak current of the inverter), as every intermediate current is also contained in that data.

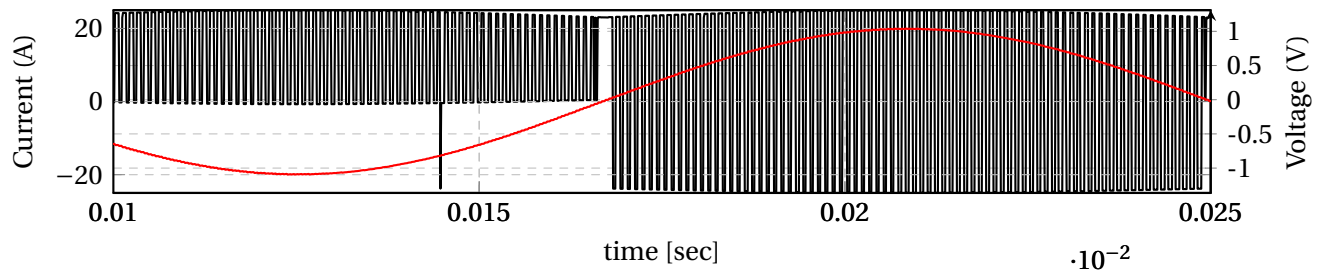


Figure 2.15: Waveform approximation to the disturbance at high (2MS/s) and low (100kS/s) sample rates.

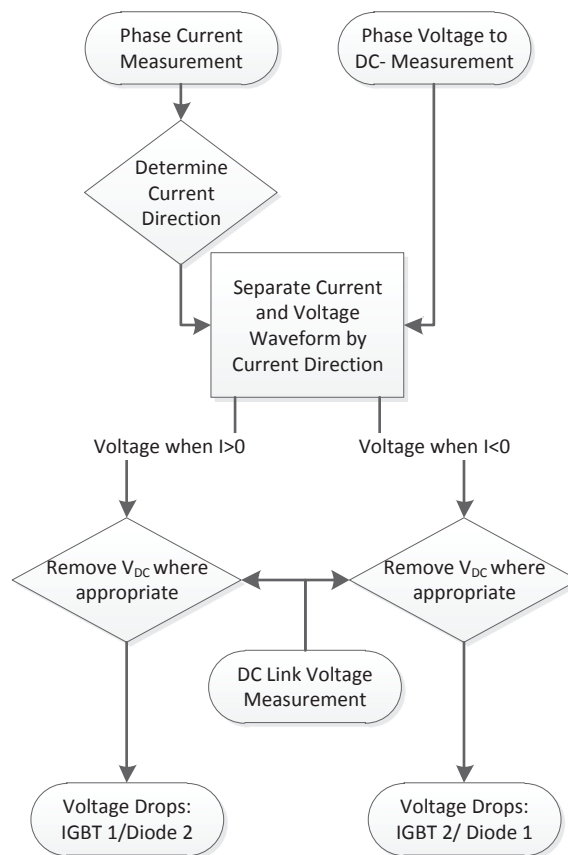
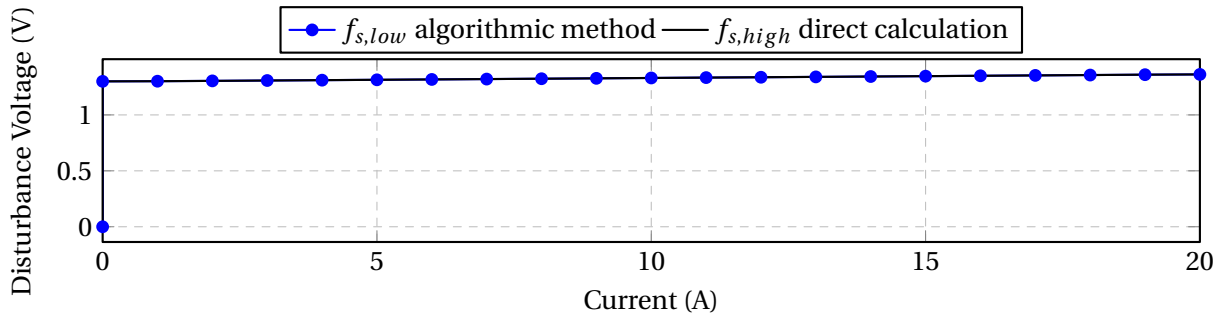


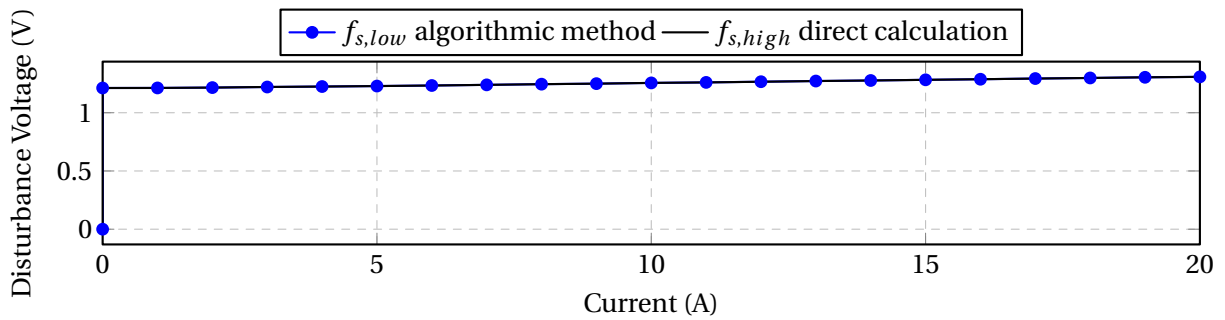
Figure 2.16: Flowchart showing the algorithm used to extract the device characteristics with applied alternating current.

Note that the simulation results demonstrate that the method performs well, although the results are noisy. Note that the enlarged waveform (zoomed) makes this appear to be a larger problem. Also, this is not an average, but all values for the voltages found plotted with respect

to the current.



(a) IGBT characteristic curve.



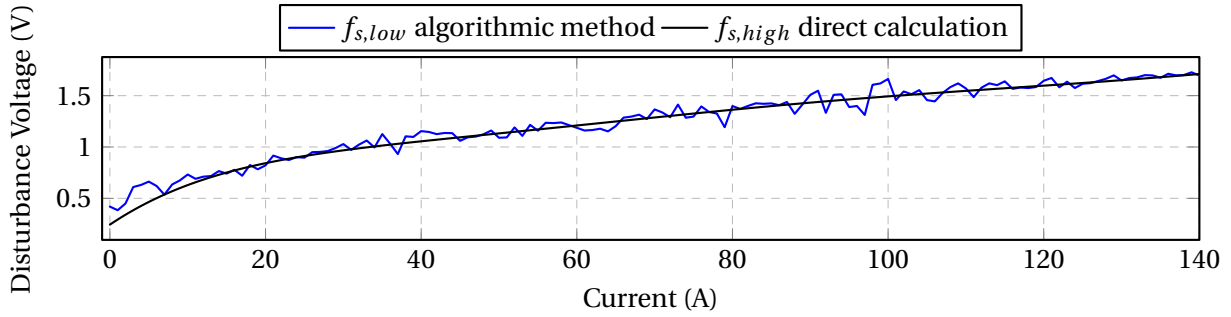
(b) Diode characteristic curve.

Figure 2.17: Experimental results of nonlinearity voltage drop spectrum extraction.

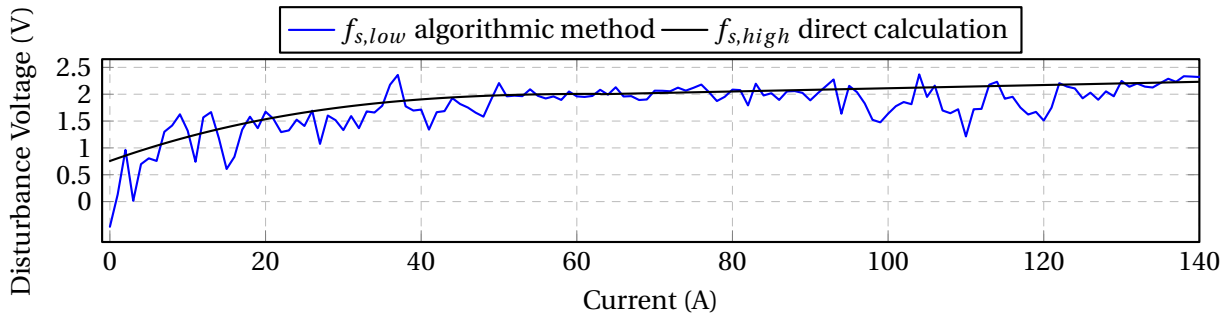
The experimental results match well to what is expected by observing the high frequency PWM waveforms. Here the values have been averaged, and as such there is only one line for either set of data.

## 2.4 Conclusion

In this report, the results of inverter characterization are given. The methods attempted were found with the goal of having a detailed, online method for inverter parameter calculation. The ‘analytical’ spectral method is best for the direct current methods. This method finds the entire behavior by applying multiple direct currents. The ‘algorithmic’ method is found to be the most appropriate method as it pertains to the alternating current case. The benefit of this is that only one experiment must be performed, the maximum peak current sinusoid case. Overall, these methods show a distinct ability to calculate the nonlinearity voltage of the inverter for each



(a) IGBT characteristic curve.



(b) Diode characteristic curve.

Figure 2.18: Experimental results of nonlinearity voltage drop spectrum extraction.

device for use in prognosis, etc. These methods also accomplish the goals of an online method which can find accurate and fairly precise results.

## 2.5 Appendix: Derivation of Phase Voltage Sensor Method

A method basis was established in section 2.2.2, which requires the finding of equivalent circuits. The parameters are found by developing a relationship between inverter measurements and the known parameters using a relationship between the two. This is done with the resistance/voltage version of the inverter equivalent circuit, breaking this into the equivalent circuits for the respective applied current vector. KVL is performed on each of these. The resulting equations are used to synthesize the relationship in equation 2.12.

$$A \begin{bmatrix} V_{I1} \\ V_{I2} \\ V_{I3} \\ V_{I4} \\ V_{I5} \\ V_{I6} \\ V_{D1} \\ V_{D2} \\ V_{D3} \\ V_{D4} \\ V_{D5} \\ V_{D6} \\ R_{I1} \\ R_{I2} \\ R_{I3} \\ R_{I4} \\ R_{I5} \\ R_{I6} \\ R_{D1} \\ R_{D2} \\ R_{D3} \\ R_{D4} \\ R_{D5} \\ R_{D6} \end{bmatrix} = b \quad (2.12)$$

### 2.5.1 Equivalent Circuits for Current Vector Along [100]

In the following equations (2.13)-(2.21) the diode circuit from Fig. 2.20 for positive phase A current is analyzed. Equations are extracted with clockwise KVL between the loops for phases

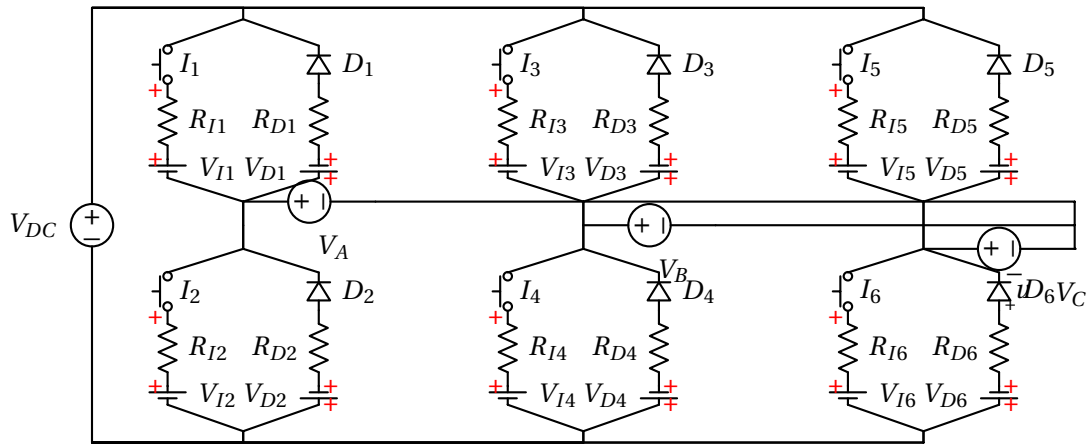


Figure 2.19: Inverter showing the inverter devices' idealized equivalent circuits.

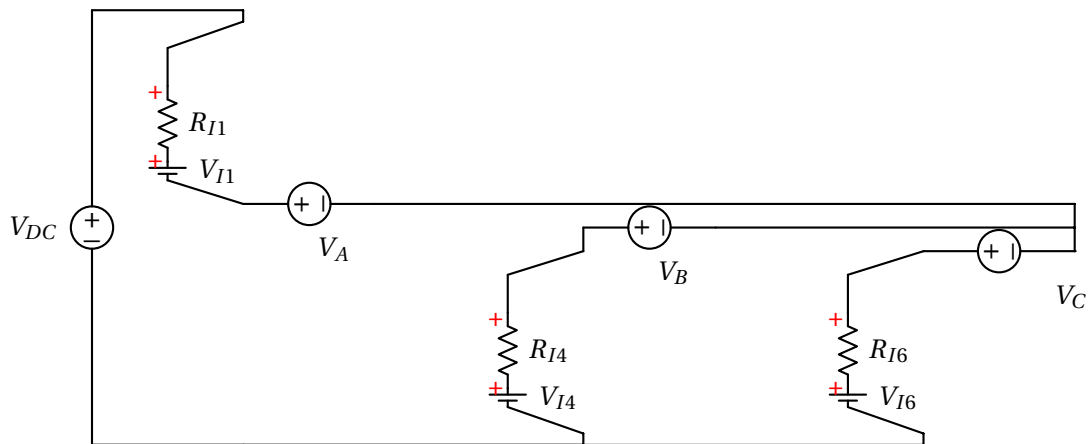


Figure 2.20: Inverter showing the inverter devices' idealized equivalent circuits.

A and B, then B and C.

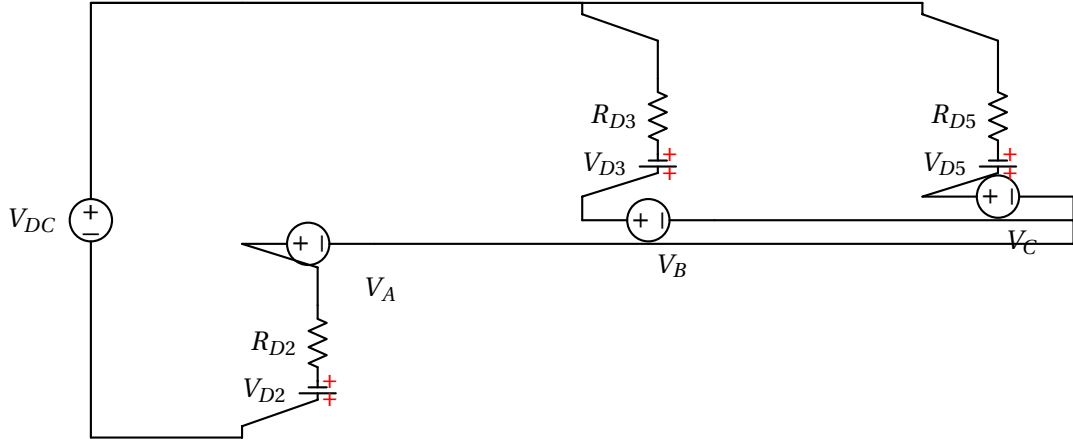


Figure 2.21: Inverter showing the inverter devices' idealized equivalent circuits.

$$i_A = I \quad (2.13)$$

$$i_B = -\frac{I}{2} \quad (2.14)$$

$$i_C = -\frac{I}{2} \quad (2.15)$$

$$V_{DC} + V_B = R_{I1} i_A + V_{I1} - R_{I4} i_B + V_{I4} + V_A \quad (2.16)$$

$$V_{DC} + V_B - V_A = R_{I1} i_A + V_{I1} - R_{I4} i_B + V_{I4} \quad (2.17)$$

$$V_{DC} + V_B - V_A = R_{I1} I + V_{I1} + R_{I4} \frac{I}{2} + V_{I4} \quad (2.18)$$

$$V_B - R_{I6} i_C + V_{I6} = V_{I4} - R_{I4} i_B + V_C \quad (2.19)$$

$$V_B - V_C = V_{I4} - R_{I4} i_B + R_{I6} i_C - V_{I6} \quad (2.20)$$

$$V_B - V_C = V_{I4} + R_{I4} \frac{I}{2} - R_{I6} \frac{I}{2} - V_{I6} \quad (2.21)$$

In the following equations (2.22)-(2.30) the diode circuit from Fig. 2.21 for positive phase A current is analyzed. Equations are extracted with clockwise KVL between the loops for phases A and B, then B and C.



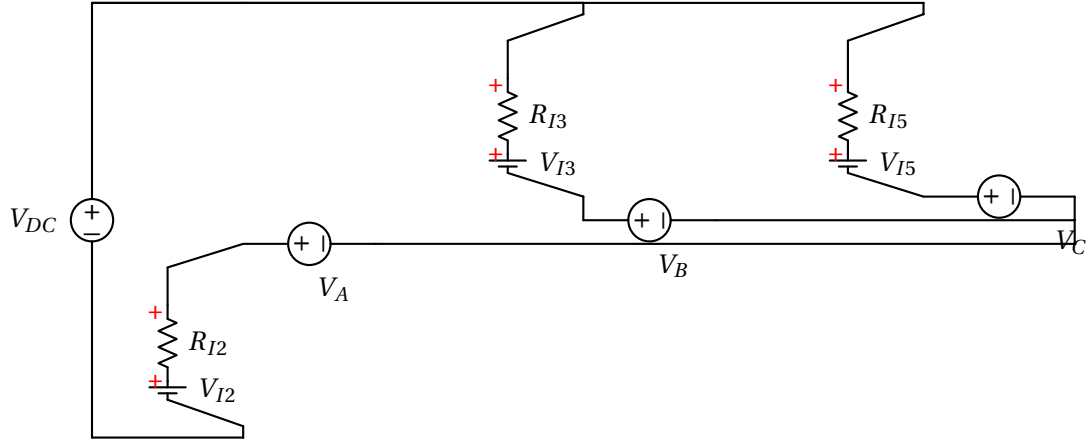


Figure 2.22: Inverter showing the inverter devices' idealized equivalent circuits.

$$i_A = I \quad (2.22)$$

$$i_B = -\frac{I}{2} \quad (2.23)$$

$$i_C = -\frac{I}{2} \quad (2.24)$$

$$V_B = V_{DC} - R_{D3}i_B + V_{D3} + V_A + R_{D2}i_A + V_{D2} \quad (2.25)$$

$$V_B - V_{DC} - V_A = -R_{D3}i_B + V_{D3} + R_{D2}i_A + V_{D2} \quad (2.26)$$

$$V_B - V_{DC} - V_A = +R_{D3}\frac{I}{2} + V_{D3} + R_{D2}I + V_{D2} \quad (2.27)$$

$$V_B - R_{D5}i_C + V_{D5} = V_{D3} - R_{D3}i_b + V_C \quad (2.28)$$

$$V_B - V_C = V_{D3} - R_{D3}i_b + R_{D5}i_C - V_{D5} \quad (2.29)$$

$$V_B - V_C = V_{D3} + R_{D3}\frac{I}{2} - R_{D5}\frac{I}{2} - V_{D5} \quad (2.30)$$

## 2.5.2 Equivalent Circuits for Current Vector Along [011]

In the following equations (2.31)-(2.39), the Fig. 2.22 circuit is analyzed with KVL clockwise in the B and A loop as well as the B and C loop.

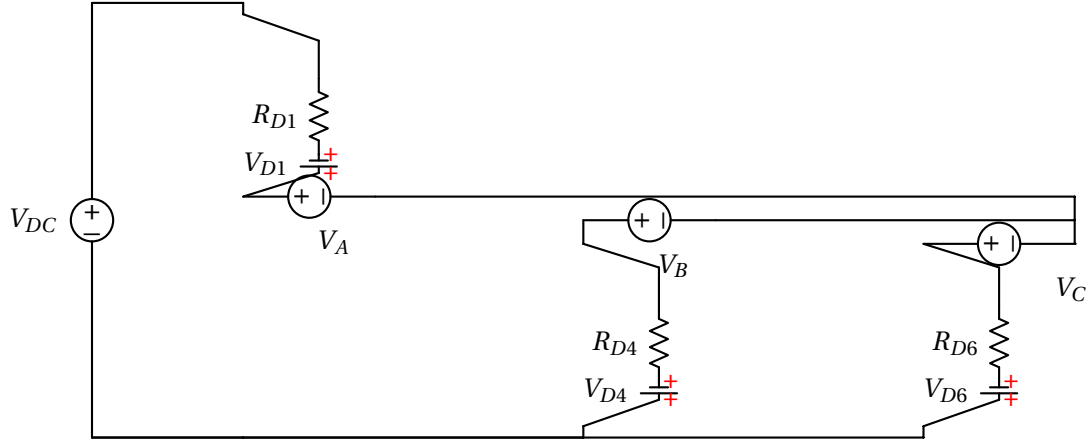


Figure 2.23: Inverter showing the inverter devices' idealized equivalent circuits.

$$i_A = -I \quad (2.31)$$

$$i_B = \frac{I}{2} \quad (2.32)$$

$$i_C = \frac{I}{2} \quad (2.33)$$

$$V_{DC} + V_A = R_{I3}i_B + V_{I3} + V_B - R_{I2}i_A + V_{I2} \quad (2.34)$$

$$V_{DC} + V_A - V_B = R_{I3}i_B + V_{I3} - R_{I2}i_A + V_{I2} \quad (2.35)$$

$$V_{DC} + V_A - V_B = R_{I3}\frac{I}{2} + V_{I3} + R_{I2}I + V_{I2} \quad (2.36)$$

$$V_{I3} + R_{I3}i_B + V_B = R_{I5}i_C + V_{I5} + V_C \quad (2.37)$$

$$V_B - V_C = R_{I5}i_C + V_{I5} + -V_{I3} - R_{I3}i_B \quad (2.38)$$

$$V_B - V_C = R_{I5}\frac{I}{2} + V_{I5} + -V_{I3} - R_{I3}\frac{I}{2} \quad (2.39)$$

In the following equations (2.40)-(2.48), the Fig. 2.23 circuit is analyzed with KVL clockwise in the A and B loop as well as the B and C loop.

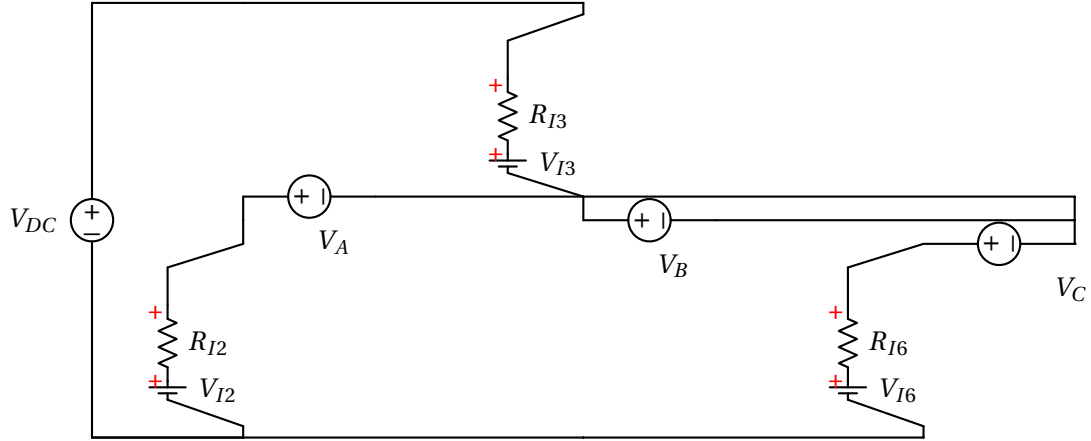


Figure 2.24: Inverter showing the inverter devices' idealized equivalent circuits.

$$i_A = -I \quad (2.40)$$

$$i_B = \frac{I}{2} \quad (2.41)$$

$$i_C = \frac{I}{2} \quad (2.42)$$

$$V_A = -R_{D1}i_A + V_{D1} + R_{D4}i_B + V_{D4} + V_B + V_{DC} \quad (2.43)$$

$$V_A - V_B - V_{DC} = -R_{D1}i_A + V_{D1} + R_{D4}i_B + V_{D4} \quad (2.44)$$

$$V_A - V_B - V_{DC} = +R_{D1}I + V_{D1} + R_{D4}\frac{I}{2} + V_{D4} \quad (2.45)$$

$$V_C + R_{D6}i_C + V_{D6} = V_{D4} + R_{D4}i_B + V_B \quad (2.46)$$

$$V_C - V_B = V_{D4} + R_{D4}i_B - R_{D6}i_C - V_{D6} \quad (2.47)$$

$$V_C - V_B = V_{D4} + R_{D4}\frac{I}{2} - R_{D6}\frac{I}{2} - V_{D6} \quad (2.48)$$

### 2.5.3 Equivalent Circuits for Current Vector Along [010]

In the following equations (2.49)-(2.57), the Fig. 2.24 circuit is analyzed with KVL clockwise in the B and A loop as well as the A and C loop.

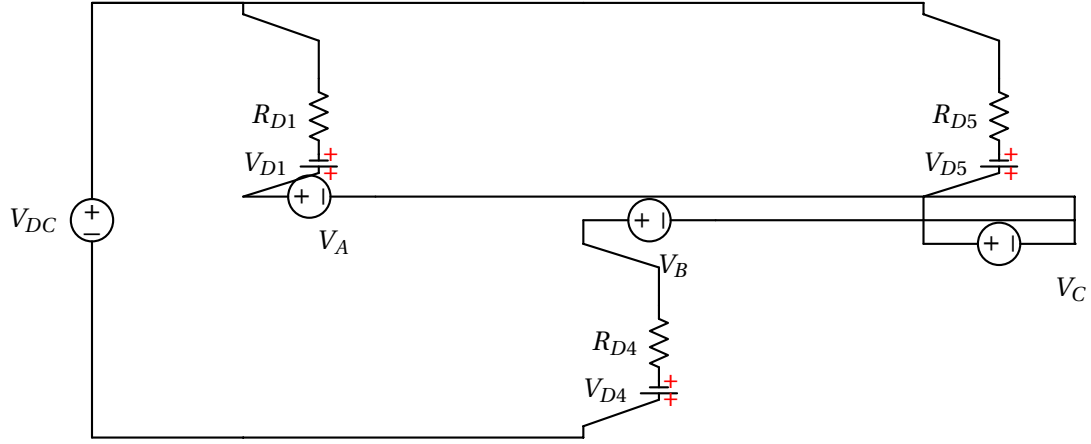


Figure 2.25: Inverter showing the inverter devices' idealized equivalent circuits.

$$i_A = -\frac{I}{2} \quad (2.49)$$

$$i_B = I \quad (2.50)$$

$$i_C = -\frac{I}{2} \quad (2.51)$$

$$V_{DC} + V_A = R_{I3}i_B + V_{I3} + V_B - R_{I2}i_A + V_{I2} \quad (2.52)$$

$$V_{DC} + V_A - V_B = R_{I3}i_B + V_{I3} - R_{I2}i_A + V_{I2} \quad (2.53)$$

$$V_{DC} + V_A - V_B = R_{I3}I + V_{I3} + R_{I2}\frac{I}{2} + V_{I2} \quad (2.54)$$

$$V_{I2} - R_{I2}i_A + V_C = V_A - R_{I6}i_C + V_{I6} \quad (2.55)$$

$$V_C - V_A = -R_{I6}i_C + V_{I6} - V_{I2} + R_{I2}i_A \quad (2.56)$$

$$V_C - V_A = +R_{I6}\frac{I}{2} + V_{I6} - V_{I2} - R_{I2}\frac{I}{2} \quad (2.57)$$

In the following equations (2.58)-(2.66), the Fig. 2.25 circuit is analyzed with KVL clockwise in the B and A loop as well as the A and C loop.

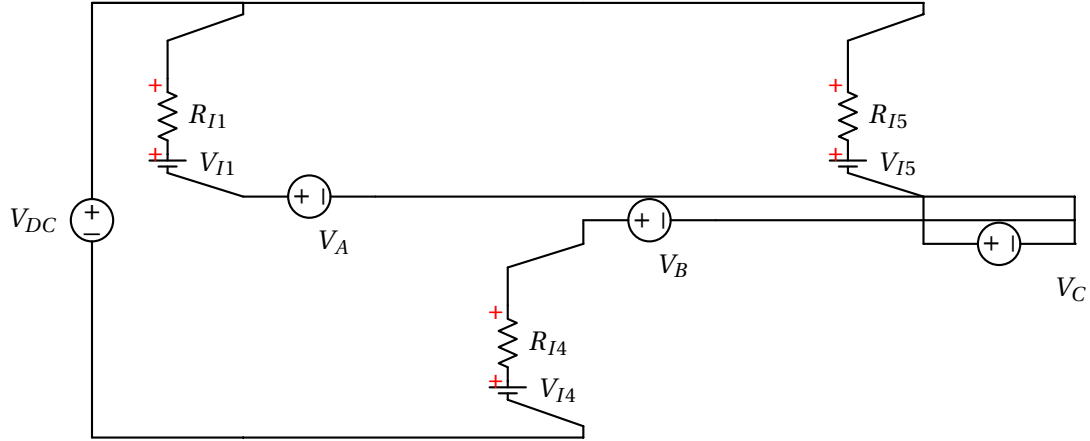


Figure 2.26: Inverter showing the inverter devices' idealized equivalent circuits.

$$i_A = -\frac{I}{2} \quad (2.58)$$

$$i_B = I \quad (2.59)$$

$$i_C = -\frac{I}{2} \quad (2.60)$$

$$V_A = V_{DC} - R_{D1}i_A + V_{D1} + V_B + R_{D4}i_B + V_{D4} \quad (2.61)$$

$$V_A - V_{DC} - V_B = -R_{D1}i_A + V_{D1} + R_{D4}i_B + V_{D4} \quad (2.62)$$

$$V_A - V_{DC} - V_B = +R_{D1}\frac{I}{2} + V_{D1} + R_{D4}I + V_{D4} \quad (2.63)$$

$$V_A - R_{D5}i_C + V_{D5} = -R_{D1}i_A + V_{D1} + V_C \quad (2.64)$$

$$V_A - V_C = -R_{D1}i_A + V_{D1} + R_{D5}i_C - V_{D5} \quad (2.65)$$

$$V_A - V_C = +R_{D1}\frac{I}{2} + V_{D1} - R_{D5}\frac{I}{2} - V_{D5} \quad (2.66)$$

#### 2.5.4 Equivalent Circuits for Current Vector Along [101]

In the following equations (2.67)-(2.75), the Fig. 2.26 circuit is analyzed with clockwise KVL in the A and B loop as well as the A and C loop.

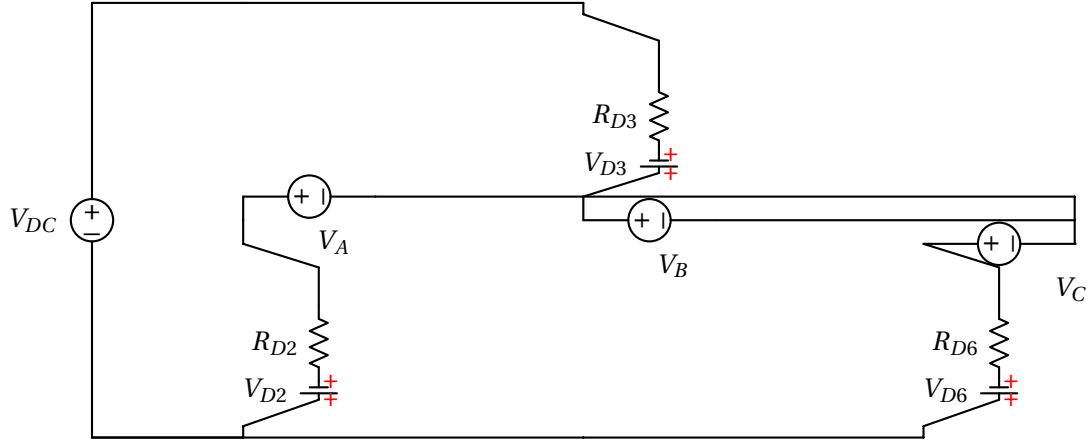


Figure 2.27: Inverter showing the inverter devices' idealized equivalent circuits.

$$i_A = \frac{I}{2} \quad (2.67)$$

$$i_B = -I \quad (2.68)$$

$$i_C = \frac{I}{2} \quad (2.69)$$

$$V_{DC} + V_B = R_{I1} i_A + V_{I1} + V_A - R_{I4} i_B + V_{I4} \quad (2.70)$$

$$V_{DC} - V_A + V_B = R_{I1} i_A + V_{I1} - R_{I4} i_B + V_{I4} \quad (2.71)$$

$$V_{DC} - V_A + V_B = R_{I1} \frac{I}{2} + V_{I1} + R_{I4} I + V_{I4} \quad (2.72)$$

$$V_A + V_{I1} + R_{I1} i_A = R_{I5} i_C + V_{I5} + V_C \quad (2.73)$$

$$V_A - V_C = R_{I5} i_C + V_{I5} - V_{I1} - R_{I1} i_A \quad (2.74)$$

$$V_A - V_C = R_{I5} \frac{I}{2} + V_{I5} - V_{I1} - R_{I1} \frac{I}{2} \quad (2.75)$$

In the following equations (2.76)-(2.84), the Fig. 2.27 circuit is analyzed with clockwise KVL in the B and A loop as well as the A and C loop.

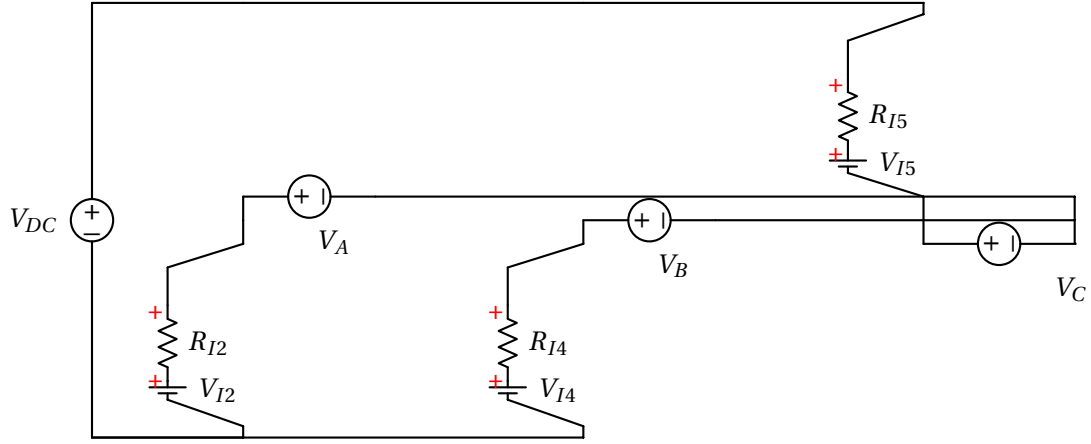


Figure 2.28: Inverter showing the inverter devices' idealized equivalent circuits.

$$i_A = \frac{I}{2} \quad (2.76)$$

$$i_B = -I \quad (2.77)$$

$$i_C = \frac{I}{2} \quad (2.78)$$

$$V_B = V_{DC} - R_{D3}i_B + V_{D3} + V_A + R_{D2}i_A + V_{D2} \quad (2.79)$$

$$V_B - V_{DC} - V_A = -R_{D3}i_B + V_{D3} + R_{D2}i_A + V_{D2} \quad (2.80)$$

$$V_B - V_{DC} - V_A = +R_{D3}I + V_{D3} + R_{D2}\frac{I}{2} + V_{D2} \quad (2.81)$$

$$V_C + R_{D6}i_C + V_{D6} = V_{D2} + R_{D2}i_A + V_A \quad (2.82)$$

$$V_C - V_A = V_{D2} + R_{D2}i_A - R_{D6}i_C - V_{D6} \quad (2.83)$$

$$V_C - V_A = V_{D2} + R_{D2}\frac{I}{2} - R_{D6}\frac{I}{2} - V_{D6} \quad (2.84)$$

### 2.5.5 Equivalent Circuits for Current Vector Along [001]

In the following equations (2.85)-(2.93), the Fig. 2.28 circuit is analyzed with clockwise KVL in the C and A loop as well as the A and B loop.

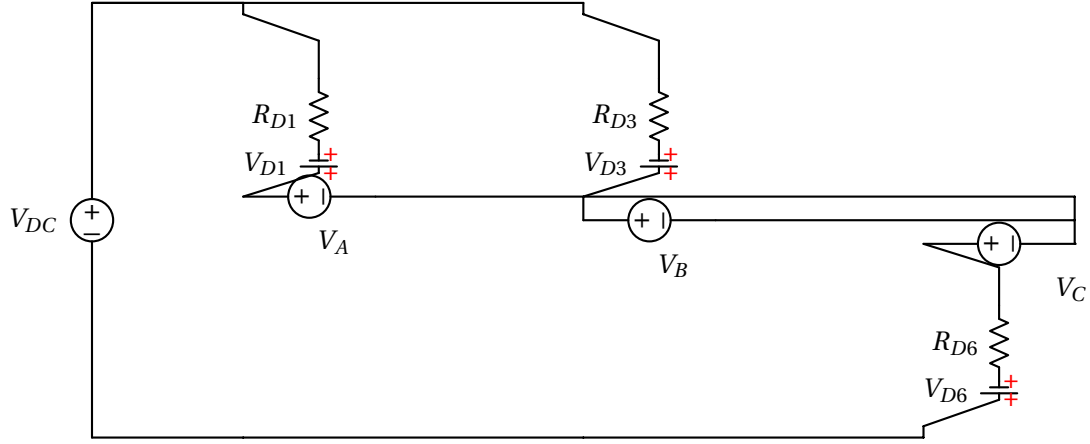


Figure 2.29: Inverter showing the inverter devices' idealized equivalent circuits.

$$i_A = -\frac{I}{2} \quad (2.85)$$

$$i_B = -\frac{I}{2} \quad (2.86)$$

$$i_C = I \quad (2.87)$$

$$V_{DC} + V_A = +R_{I5}i_C + V_{I5} + V_C - R_{I2}i_A + V_{I2} \quad (2.88)$$

$$V_{DC} + V_A - V_C = +R_{I5}i_C + V_{I5} - R_{I2}i_A + V_{I2} \quad (2.89)$$

$$V_{DC} + V_A - V_C = +R_{I5}I + V_{I5} + R_{I2}\frac{I}{2} + V_{I2} \quad (2.90)$$

$$V_{I2} - R_{I2}i_A + V_B = V_A - R_{I4}i_B + V_{I4} \quad (2.91)$$

$$V_B - V_A = -R_{I4}i_B + V_{I4} - V_{I2} + R_{I2}i_A \quad (2.92)$$

$$V_B - V_A = +R_{I4}\frac{I}{2} + V_{I4} - V_{I2} - R_{I2}\frac{I}{2} \quad (2.93)$$

In the following equations (2.94)-(2.102), the Fig. 2.29 circuit is analyzed with clockwise KVL in the A and C loop as well as the A and B loop.



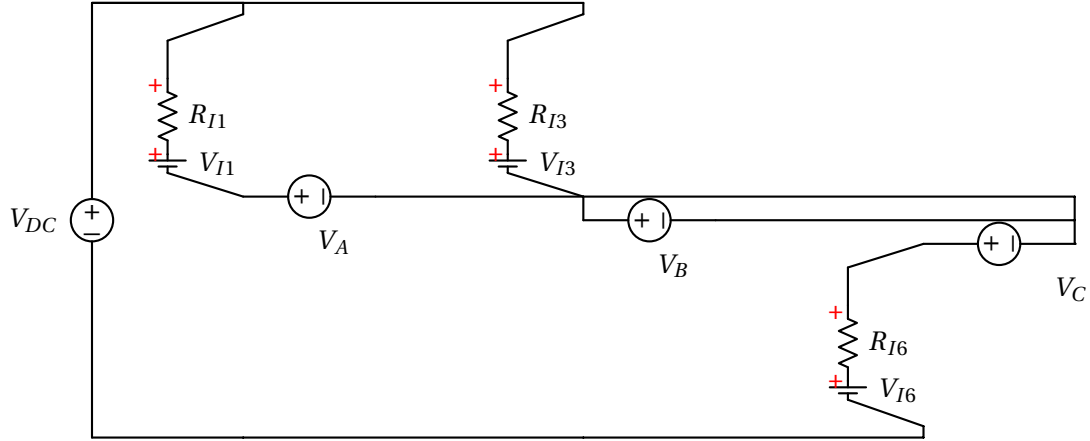


Figure 2.30: Inverter showing the inverter devices' idealized equivalent circuits.

$$i_A = -\frac{I}{2} \quad (2.94)$$

$$i_B = -\frac{I}{2} \quad (2.95)$$

$$i_C = I \quad (2.96)$$

$$V_A = V_{DC} - R_{D1}i_A + V_{D1} + V_C + R_{D6}i_C + V_{D6} \quad (2.97)$$

$$V_A - V_{DC} - V_C = -R_{D1}i_A + V_{D1} + R_{D6}i_C + V_{D6} \quad (2.98)$$

$$V_A - V_{DC} - V_C = +R_{D1}\frac{I}{2} + V_{D1} + R_{D6}I + V_{D6} \quad (2.99)$$

$$V_A - R_{D3}i_B + V_{D3} = V_{D1} - R_{D1}i_A + V_B \quad (2.100)$$

$$V_A - V_B = V_{D1} - R_{D1}i_A + R_{D3}i_B - V_{D3} \quad (2.101)$$

$$V_A - V_B = V_{D1} + R_{D1}\frac{I}{2} - R_{D3}\frac{I}{2} - V_{D3} \quad (2.102)$$

### 2.5.6 Equivalent Circuits for Current Vector Along [110]

In the following equations (2.103)-(2.111), the Fig. 2.30 circuit is analyzed with clockwise KVL in the A and C loop as well as the A and B loop.

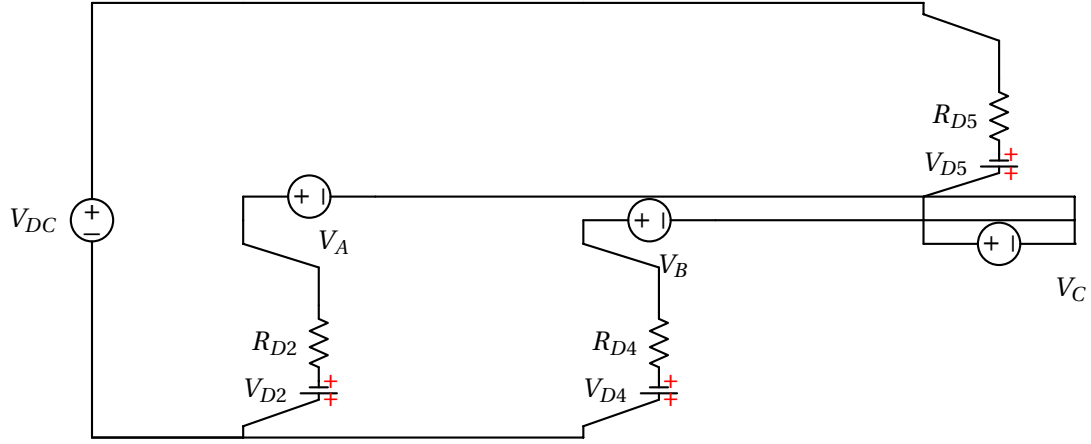


Figure 2.31: Inverter showing the inverter devices' idealized equivalent circuits.

$$i_A = \frac{I}{2} \quad (2.103)$$

$$i_B = \frac{I}{2} \quad (2.104)$$

$$i_C = -I \quad (2.105)$$

$$V_{DC} + V_C = R_{I1} i_A + V_{I1} + V_A - R_{I6} i_C + V_{I6} \quad (2.106)$$

$$V_{DC} + V_C - V_A = R_{I1} i_A + V_{I1} - R_{I6} i_C + V_{I6} \quad (2.107)$$

$$V_{DC} + V_C - V_A = R_{I1} \frac{I}{2} + V_{I1} + R_{I6} I + V_{I6} \quad (2.108)$$

$$V_A + V_{I1} + R_{I1} i_A = R_{I3} i_B + V_{I3} + V_B \quad (2.109)$$

$$V_A - V_B = R_{I3} i_B + V_{I3} - V_{I1} - R_{I1} i_A \quad (2.110)$$

$$V_A - V_B = R_{I3} \frac{I}{2} + V_{I3} - V_{I1} - R_{I1} \frac{I}{2} \quad (2.111)$$

In the following equations (2.112)-(2.120), the Fig. 2.31 circuit is analyzed with clockwise KVL in the C and A loop as well as the A and B loop.

$$i_A = \frac{I}{2} \quad (2.112)$$

$$i_B = \frac{I}{2} \quad (2.113)$$

$$i_C = -I \quad (2.114)$$

$$V_C = V_{DC} - R_{D5}i_C + V_{D5} + V_A + R_{D2}i_A + V_{D2} \quad (2.115)$$

$$V_C - V_A - V_{DC} = -R_{D5}i_C + V_{D5} + R_{D2}i_A + V_{D2} \quad (2.116)$$

$$V_C - V_A - V_{DC} = +R_{D5}I + V_{D5} + R_{D2}\frac{I}{2} + V_{D2} \quad (2.117)$$

$$V_B + R_{D4}i_B + V_{D4} = V_{D2} + R_{D2}i_A + V_A \quad (2.118)$$

$$V_B - V_A = V_{D2} + R_{D2}i_A - R_{D4}i_B - V_{D4} \quad (2.119)$$

$$V_B - V_A = V_{D2} + R_{D2}\frac{I}{2} - R_{D4}\frac{I}{2} - V_{D4} \quad (2.120)$$

With the individual circuit analysis completed, we now gather all of the resulting equations into one list, given by the equation sets (2.121) and (2.122).

$$\begin{aligned}
V_{DC} + V_B - V_A &= R_{I1}I + V_{I1} + R_{I4}\frac{I}{2} + V_{I4} \\
V_B - V_C &= V_{I4} + R_{I4}\frac{I}{2} - R_{I6}\frac{I}{2} - V_{I6} \\
V_B - V_{DC} - V_A &= +R_{D3}\frac{I}{2} + V_{D3} + R_{D2}I + V_{D2} \\
V_B - V_C &= V_{D3} + R_{D3}\frac{I}{2} - R_{D5}\frac{I}{2} - V_{D5} \\
V_{DC} + V_A - V_B &= R_{I3}\frac{I}{2} + V_{I3} + R_{I2}I + V_{I2} \\
V_B - V_C &= R_{I5}\frac{I}{2} + V_{I5} - V_{I3} - R_{I3}\frac{I}{2} \\
V_A - V_B - V_{DC} &= +R_{D1}I + V_{D1} + R_{D4}\frac{I}{2} + V_{D4} \\
V_C - V_B &= V_{D4} + R_{D4}\frac{I}{2} - R_{D6}\frac{I}{2} - V_{D6} \\
V_{DC} + V_A - V_B &= R_{I3}I + V_{I3} + R_{I2}\frac{I}{2} + V_{I2} \\
V_C - V_A &= +R_{I6}\frac{I}{2} + V_{I6} - V_{I2} - R_{I2}\frac{I}{2} \\
V_A - V_{DC} - V_B &= +R_{D1}\frac{I}{2} + V_{D1} + R_{D4}I + V_{D4} \\
V_A - V_C &= +R_{D1}\frac{I}{2} + V_{D1} - R_{D5}\frac{I}{2} - V_{D5} \\
V_{DC} - V_A + V_B &= R_{I1}\frac{I}{2} + V_{I1} + R_{I4}I + V_{I4} \\
V_A - V_C &= R_{I5}\frac{I}{2} + V_{I5} - V_{I1} - R_{I1}\frac{I}{2} \\
V_B - V_{DC} - V_A &= +R_{D3}I + V_{D3} + R_{D2}\frac{I}{2} + V_{D2} \\
V_C - V_A &= V_{D2} + R_{D2}\frac{I}{2} - R_{D6}\frac{I}{2} - V_{D6} \\
V_{DC} + V_A - V_C &= +R_{I5}I + V_{I5} + R_{I2}\frac{I}{2} + V_{I2} \\
V_B - V_A &= +R_{I4}\frac{I}{2} + V_{I4} - V_{I2} - R_{I2}\frac{I}{2} \\
V_A - V_{DC} - V_C &= +R_{D1}\frac{I}{2} + V_{D1} + R_{D6}I + V_{D6} \\
V_A - V_B &= V_{D1} + R_{D1}\frac{I}{2} - R_{D3}\frac{I}{2} - V_{D3} \\
V_{DC} + V_C - V_A &= R_{I1}\frac{I}{2} + V_{I1} + R_{I6}I + V_{I6} \\
V_A - V_B &= R_{I3}\frac{I}{2} + V_{I3} - V_{I1} - R_{I1}\frac{I}{2}
\end{aligned} \tag{2.121}$$

$$\begin{aligned}
V_C - V_A - V_{DC} &= +R_{D5}I + V_{D5} + R_{D2}\frac{I}{2} + V_{D2} \\
V_B - V_A &= V_{D2} + R_{D2}\frac{I}{2} - R_{D4}\frac{I}{2} - V_{D4}
\end{aligned}
\tag{2.122}$$

Given this, it is now possible to put the equations into the  $Ax = b$  form.

$$\begin{bmatrix}
V_{DC} + V_B - V_A \\
V_B - V_C \\
V_B - V_{DC} - V_A \\
V_B - V_C \\
V_{DC} + V_A - V_B \\
V_B - V_C \\
V_A - V_B - V_{DC} \\
V_C - V_B \\
V_{DC} + V_A - V_B \\
V_C - V_A \\
V_A - V_{DC} - V_B \\
V_A - V_C \\
V_{DC} - V_A + V_B \\
V_A - V_C + V \\
V_B - V_{DC} - V_A \\
V_C - V_A \\
V_{DC} + V_A - V_C \\
V_B - V_A \\
V_A - V_{DC} - V_C \\
V_A - V_B \\
V_{DC} + V_C - V_A \\
V_A - V_B \\
V_C - V_A - V_{DC} \\
V_B - V_A
\end{bmatrix} = \tag{2.123}$$





$$\begin{aligned}
V_{DC} + V_B - V_A &= f_{I1} + f_{I4} \\
V_B - V_C &= f_{I4} - f_{I6} \\
V_B - V_{DC} - V_A &= f_{D3} + f_{D2} \\
V_B - V_C &= f_{D3} - f_{D5} \\
V_{DC} + V_A - V_B &= f_{I3} + f_{I2} \\
V_B - V_C &= f_{I5} - f_{I3} \\
V_A - V_B - f_{DC} &= f_{D1} + f_{D4} \\
V_C - V_B &= f_{D4} - f_{D6} \\
V_{DC} + V_A - V_B &= f_{I3} + f_{I2} \\
V_C - V_A &= f_{I6} - f_{I2} \\
V_A - V_{DC} - V_B &= f_{D1} + f_{D4} \\
V_A - V_C &= f_{D1} - f_{D5} \\
V_{DC} - V_A + V_B &= f_{I1} + f_{I4} \\
V_A - V_C &= f_{I5} - f_{I1} \\
V_B - V_{DC} - V_A &= f_{D3} + f_{D2} \\
V_C - V_A &= f_{D2} - f_{D6} \\
V_{DC} + V_A - V_C &= f_{I5} + f_{I2} \\
V_B - V_A &= f_{I4} - f_{I2} \\
V_A - V_{DC} - V_C &= f_{D1} + f_{D6} \\
V_A - V_B &= f_{D1} - f_{D3} \\
V_{DC} + V_C - V_A &= f_{I1} + f_{I6} \\
V_A - V_B &= f_{I3} - f_{I1} \\
V_C - V_A - V_{DC} &= f_{D5} + f_{D2} \\
V_B - V_A &= f_{D2} - f_{D4}
\end{aligned} \tag{2.126}$$



Although there are 24 equations, calculating the rank of the A matrix in equation 2.125 makes it clear that the matrix is insufficient to characterize the entire inverter; the rank is only 20/24. By performing the algorithm shown in Fig. 2.33, the row dependency is found, and thus the circuits which are interdependent.

From this algorithm, the rows which the dependent row is dependent upon are found. This allows for understanding how to proceed. The algorithm shows that equations (2.39), (2.66), (2.93), and (2.120) are dependent upon equations (2.75) and (2.111), (2.30) and (2.102), (2.57) and (2.21), as well as (2.48) and (2.84), respectively. This dependency is exemplified by equations 2.127, 2.128, 2.129, and 2.130. These equations make it clear that the method proposed is not sufficient. One of the four examples of this is Fig. 2.34, which shows the circuits used to build equations (2.39), dependent upon (2.75) and (2.111). The circuits are clearly not independent, as the third can be made from a linear combination of the other two. Overall, this means that finding the device characteristics requires either more tests to generate more equations for the system which are not linearly dependent, or that the method is not viable for this purpose, and the novel sensor setup in Fig. 2.1 is required.

$$\begin{array}{l} -(V_A - V_B = R_{I3}\frac{I}{2} + V_{I3} - V_{I1} - R_{I1}\frac{I}{2}) \\ (V_A - V_C = R_{I5}\frac{I}{2} + V_{I5} - V_{I1} - R_{I1}\frac{I}{2}) \\ \hline (V_B - V_C = R_{I5}\frac{I}{2} + V_{I5} - V_{I3} - R_{I3}\frac{I}{2}) \end{array} \quad (2.127)$$

$$\begin{array}{l} (V_B - V_C = V_{D3} + R_{D3}\frac{I}{2} - R_{D5}\frac{I}{2} - V_{D5}) \\ (V_A - V_B = V_{D1} + R_{D1}\frac{I}{2} - R_{D3}\frac{I}{2} - V_{D3}) \\ \hline (V_A - V_C = +R_{D1}\frac{I}{2} + V_{D1} - R_{D5}\frac{I}{2} - V_{D5}) \end{array} \quad (2.128)$$

$$\begin{array}{l} (V_C - V_A = +R_{I6}\frac{I}{2} + V_{I6} - V_{I2} - R_{I2}\frac{I}{2}) \\ (V_B - V_C = V_{I4} + R_{I4}\frac{I}{2} - R_{I6}\frac{I}{2} - V_{I6}) \\ \hline (V_B - V_A = +R_{I4}\frac{I}{2} + V_{I4} - V_{I2} - R_{I2}\frac{I}{2}) \end{array} \quad (2.129)$$

$$\begin{array}{l}
-(V_C - V_B = V_{D4} + R_{D4}\frac{I}{2} - R_{D6}\frac{I}{2} - V_{D6}) \\
(V_C - V_A = V_{D2} + R_{D2}\frac{I}{2} - R_{D6}\frac{I}{2} - V_{D6}) \\
\hline
(V_B - V_A = V_{D2} + R_{D2}\frac{I}{2} - R_{D4}\frac{I}{2} - V_{D4})
\end{array} \tag{2.130}$$

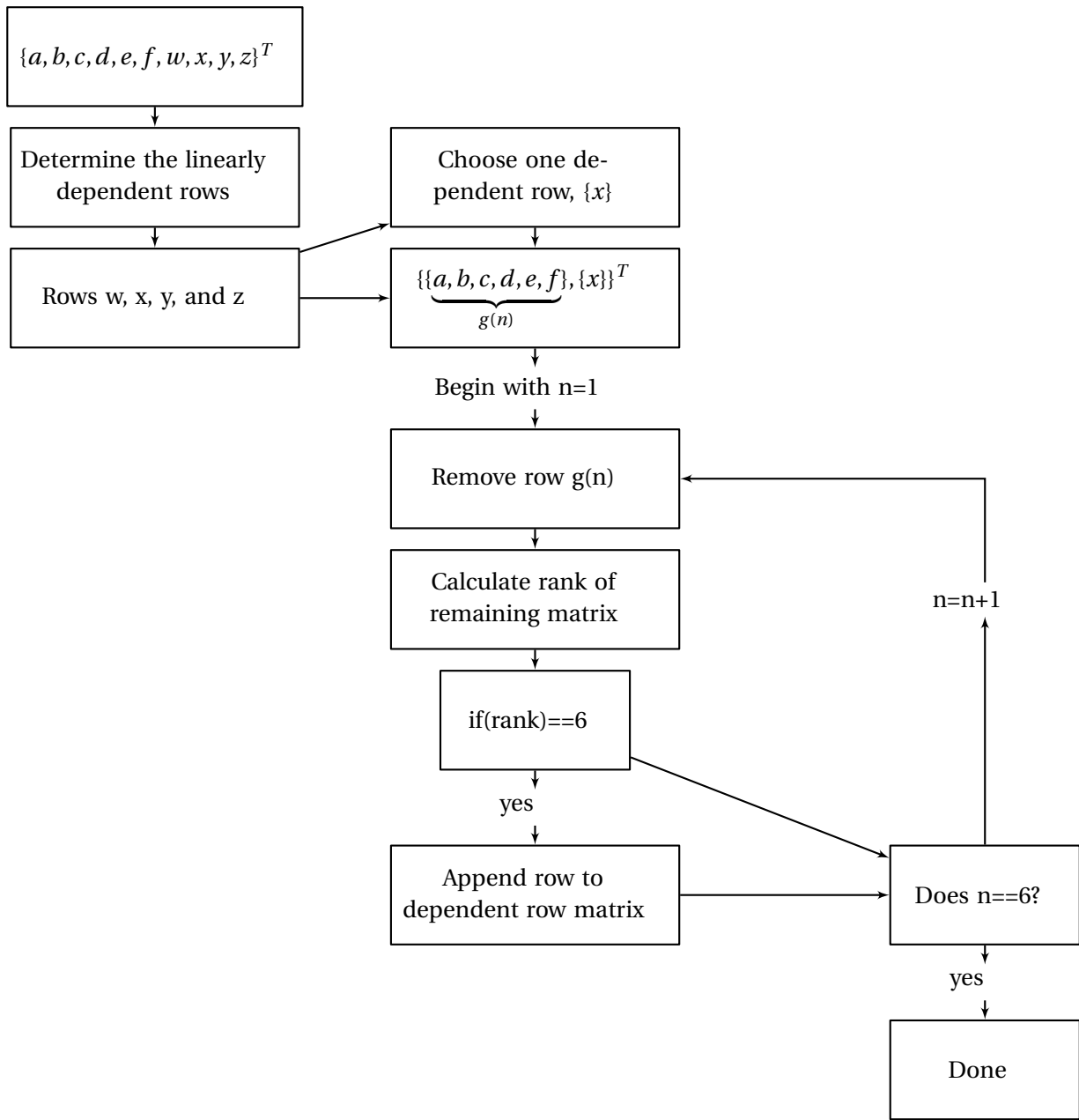


Figure 2.33: Flowchart used to determine which rows the linearly dependent rows are dependent upon.

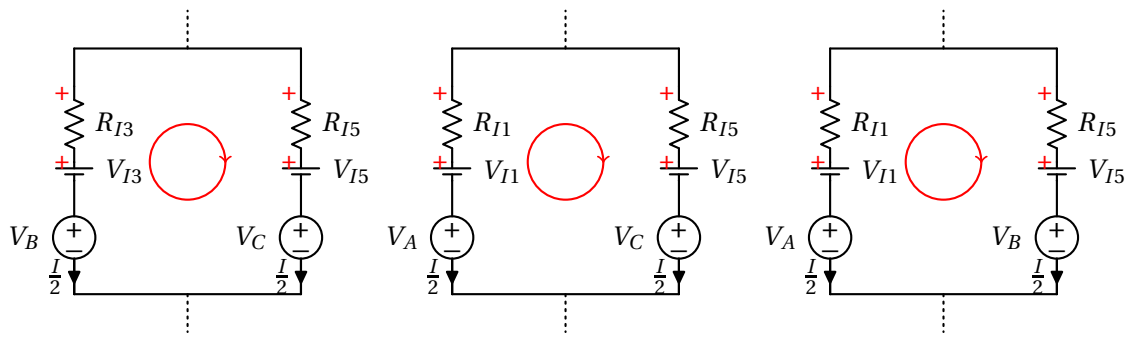


Figure 2.34: Linearly dependent circuit set.

# Chapter 3

## APEC 2014 Conference Submission:

### “Inverter Device Nonlinearity

### Characterization Technique for Use in a

### Motor Drive System”

#### 3.1 Introduction

##### 3.1.1 Motivation

The characteristic of semiconductor devices is such that they have a nonlinear voltage and current characteristic. Coupled with the use of pulsewidth modulation (PWM) to control the current in three phase inverters and the complications associated with this, the output voltage of a three phase voltage source inverter (VSI) is distorted. These phenomena resulting in the distortion of the output voltage of an inverter are termed inverter nonlinearities.

Typically because the distortion caused by such nonlinearities is small it is ignored, or maybe only one nonlinearity is mitigated. The case where all are studied or accounted for is rare. There are, however, situations where it is important to understand these inverter nonlinearities. The nonlinearities themselves may contain information about the health of the drive. Diagnosis and prognosis (D&P) studies attempt to take advantage of the information the nonlinearities hold in order to evaluate the condition of the inverter and predict the future health. The use of inverter nonlinearities for D&P has been discussed at various lengths in [1–3].

Inverter nonlinearities, if not mitigated, may have a negative effect upon the operation of sensorless drive schemes. Sensorless schemes, typically using flux and position observers, suffer observer performance degradation in the presence of inverter nonlinearities. The observers must not only take into account the machine model, which is typical, but also that of the inverter nonlinearities. Further, other studies seek to remove the effect of inverter nonlinearities in order to achieve a smoother output voltage. Removing these effects is especially important at low speeds and currents, where the voltage distortion can be significant with respect to the power frequency fundamental. Removing effects from voltage applied to the machine can improve the current and torque controller stability and performance. Discussion of the nonlinear effects, and methods to mitigate inverter nonlinearities have been studied in [4–12]. The problem with not accounting for inverter nonlinearities is clearly seen in situations where the voltage command is used to estimate machine voltage. For instance, in [13] accounting for inverter nonlinearities is used to simplify the characterization procedure by avoiding the use of voltage sensors.

This paper is concerned with the detailed characterization of these inverter nonlinearities over the entire device operating current. The motivation for this is in finding the inverter nonlinearity curve and using this to determine the condition of the inverter. This method achieves this, while other literature does not, as it can separate all of the inverter devices and thus determine the condition of each of the inverter devices individually.

### **3.1.2 Outline**

The paper is organized according to the various methods used in the characterization. The structure is given in the following:

- Section 3.2 discusses the nonlinearity classification and the approach chosen in this paper.
- Section 3.3 develops a representation for the disturbance analytically and graphically.
- Section 3.4 develops characterization methods which utilize the application of direct cur-

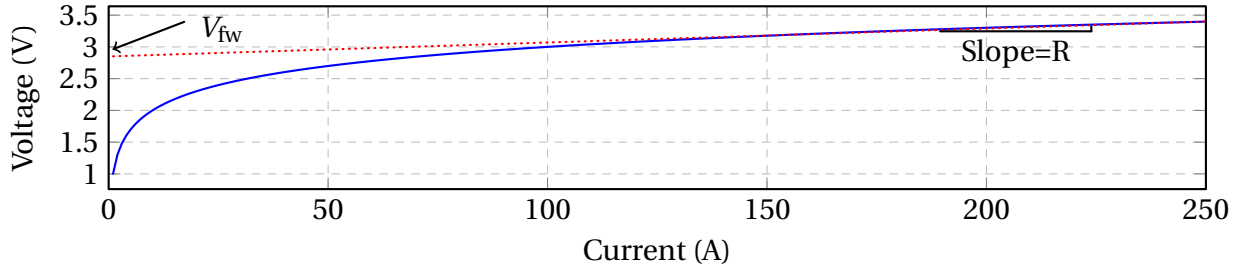


Figure 3.1: Waveforms showing a generalized semiconductor nonlinearity, given as its VI characteristic and the linear approximation to this with its equivalent parameters; this is the key characteristic for a device.

rent to the machine at standstill.

- Section 3.5 develops characterization methods which utilize the application of alternating current to the machine at standstill.

## 3.2 Study of Nonlinearities

### 3.2.1 Nonlinearity Classification

When studying these nonlinearities for any purpose, it is important to define which nonlinearities are important for the application. The most pronounced nonlinearities – due to commonly available hardware sensors – are the forward voltage drop and resistance of the inverter semiconductors (i.e. IGBT and diode). There exist other device characteristics which may be studied, including the gate current ( $i_g$ ) and gate-emitter voltage ( $V_{GE}$ ), however it is uncommon to sense the gate characteristics given that there are rarely sensors added to the IGBT gates. The goal is, therefore, to find the voltage drop over the collector to the emitter pathway of each of the semiconductor devices. As stated, there are four characteristics in all: The resistance ( $R_d$ ) and forward biased junction voltage ( $V_{th,d}$ ) over the diode, and the resistance ( $R_i$ ) and forward biased junction voltage ( $V_{th,i}$ ) over the IGBT. These quantities can be used to approximate the inverter nonlinearity, as shown in Fig. 3.1.

### 3.2.2 Requirements on the Procedure

Any characterization procedure should also allow for finding the parameters of every device. The authors in [4, 5, 7, 14] all investigate methods which do not find the exact device parameters, but some average effect of the diode and IGBT in any given situation; their goal is removing the effect of the nonlinearity, not condition monitoring. From the literature review done here, no paper has found an effective method to determine the complete inverter device  $V_{CE}$  parameters. To isolate each individual quantity, new characterization methods have been developed. With this in mind, the task then becomes one of finding the best method of characterization. Several methods described in literature characterize the inverter, but many such as [14], could not isolate specific device quantities. The final goal of any characterization method is to develop a method and record the voltage and current relationship for each device. The resistance and forward junction drop for each device can be found from this voltage and current relationship.

Additionally, the methods require a sampling rate above the switching frequency, as the PWM voltage waveform is required for the calculation of the device characteristics. Following the Nyquist rate requirement, the sampling frequency must be greater than twice the signal bandwidth. With filtering of harmonics greater than the first AC harmonic, a sampling rate of only just over twice the switching frequency is required. A sampling frequency of 100 kHz for a switching frequency of 5 kHz is assumed in simulation and used in experimentation, which is more than required per the Nyquist criterion. Note that this sampling rate is chosen to be reasonable in a typical drive system which uses an embedded microcontroller.

### 3.2.3 General Approach

This problem of device characterization in an inverter is solved in two ways for direct currents. The first method works with the application of direct currents by finding two equations related to the mean of the sensed voltage to solve for both of the two unknown nonlinearity voltages,  $V_{igbt}$  and  $V_{diode}$ , using sensed currents, voltages, and applied duty cycle. To get the voltage for multiple direct currents, multiple direct currents must be applied, and the mean equation for a



constant duty cycle waveform used. The second method uses the same sensed quantities, but utilizes the PWM spectrum instead. For DC, the current spectrum method is extended for use in the case of alternating currents. The methods are then modified in order to determine the device parameters with line-to-line voltage sensing.

### **3.2.4 Experimental Setup**

The test setup consists of a three-phase induction machine with a current rating of 200 A connected to the SEMIKRON SKiiP 2 three phase inverter with a current rating of 250 A. The inverter lacks microcontroller control, but instead uses a dSPACE system for control. The dSPACE system is programmed to allow for either AC or direct current control, and has all phase current sensors as well as a DC link voltage sensor. The PWM, and sampling frequency of this system is 5 kHz. In parallel to the dSPACE data acquisition, an HBM GEN2i data acquisition system is used to sense all voltages and currents (phase and DC link) as shown in Fig. 3.2 as well as two different phase voltage sensing arrangements i.e. line-to-line and line to negative DC link. The GEN2i system samples at 2 MS/sec, which can be down-sampled to the appropriate testing frequency. An identical connection setup is used for simulation purposes, but device characteristics are chosen as follows:  $V_{th,d} = 1.2V$ ,  $V_{th,i} = 1.3V$ ,  $R_d = 4 m\Omega$ , and  $R_i = 6 m\Omega$ .

## **3.3 Representing the Voltage Disturbance**

For analysis purposes, representations for the disturbances must be found. The first set of methods introduced in this paper assume that voltage and current sensors are available for all phases with respect to the negative DC link, as well as a DC link voltage sensor. The second set of methods assumes a small difference in sensor location; this method set assumes that the measurements are either across the machine line-to-line or line-to-neutral. The voltage current relationship being the goal, a test – or series of tests – must determine the entire device's V-I relationship. This is done by applying a current to each device and somehow determining the voltage during this current application. Some calculations can be done on the various volt-

ages to calculate this device voltage. The linear region is of note, and occurs when the linear approximation and actual characteristic curve meet, as in Fig. 3.1 at 125 A. The characteristic below this is also useful, but in order to characterize the device fully, the linear region must be captured.

The methods all require that the disturbance voltage be isolated from the phase voltage sensor measurements. With the phase and DC link voltage sensors, the information required to characterize the devices is available.

### 3.3.1 Representing the Voltage Disturbance with Direct Current

To demonstrate that this waveform is all that is required, assume for a moment that phase A of the inverter is used to conduct a positive current into the load. Per the current direction, the top IGBT will conduct, with the bottom diode freewheeling, as long as the positive current is maintained. Note that Fig. 3.3 demonstrates this. Also note the placement of the voltage sensor. When the bottom diode is conducting, during freewheeling, it is clear that the voltage measured by the sensor will be that of the bottom diode. When the IGBT is conducting, the voltage will be that of the DC link, less the IGBT voltage drop. The IGBT voltage drop can be determined with the DC link voltage measurement by  $V_{DC} - V_{A \rightarrow DC}$ . This DC link subtraction is only done when the IGBT is conducting, determined when the voltage measured is greater than zero. By measuring the diode voltage directly, and using the expression to determine the top IGBT voltage, a square wave results, and is shown in Fig. 3.4. The IGBT voltage is given by  $a$ , whereas the diode voltage is given by  $b$ . This is shown for a PWM waveform resulting from applied direct current. This is herein referred to as the disturbance voltage waveform,  $V_{dist}$ . The problem now becomes using this fact to extract the inverter nonlinearities from all devices.

#### 3.3.1.1 Analytic Expression of the DC Waveform

An expression for the PWM waveform, or disturbance waveform should be found analytically. An analytic expression is derived using the sensor voltages as given in Fig. 3.2. The PWM waveform when constant direct current is applied is first discussed, similar to that found in Fig. 3.4

for only the disturbance signal. There are two cases which should be discussed for direct current operation; the positive and negative current cases result in different device measurements. In Fig. 3.3 positive current is seen, where only the top IGBT of phase A (IGBT 1/I1) and the bottom diode of phase A (Diode 2/D2) conduct. The phase A sensor measurement here is given by equation (3.1). Note that this assumes that the rising edge of the rectangular pulse PWM signal occurs at time  $t=0$  and that  $V_{A \rightarrow DC}^{+/-}(t) = V_{A \rightarrow DC}^{+/-}(t + T)$ . Conversely, negative current results in the analytic expression given by equation (3.2). Using these two expressions, a complete phase voltage waveform can be given as in equation (3.3). The interphase version of this is simply found by subtracting two of these, for whatever phase combination is desired as in equation (3.4), given for phases A and B.

$$V_{A \rightarrow DC}^{+}(t) = [V_{DC} - V_{I1}(i_a)] u(t) - [(V_{DC} - V_{I1}(i_a)) + V_{D2}(i_a)] u(t - DT_c) \quad (3.1)$$

$$V_{A \rightarrow DC}^{-}(t) = [V_{I2}(i_a)] u(t) - [V_{I2}(i_a) - (V_{DC} + V_{D1}(i_a))] u(t - DT_c) \quad (3.2)$$

$$V_{A \rightarrow DC}(t) = V_{A \rightarrow DC}^{-}(t) \left\{ \frac{1}{2}(\text{sgn}(i_a) + 1) \right\} + V_{A \rightarrow DC}^{+}(t) \left\{ \frac{1}{2}(1 - \text{sgn}(i_a)) \right\} \quad (3.3)$$

$$V_{A \rightarrow B}(t) = V_{A \rightarrow DC}(t) - V_{B \rightarrow DC}(t) \quad (3.4)$$

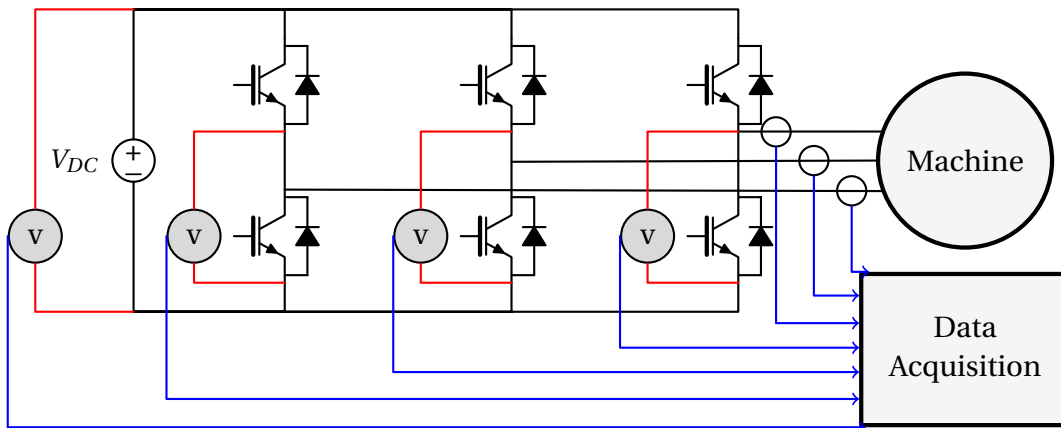


Figure 3.2: Experimental setup for inverter characterization showing the sensor connections which allow for line-to-line and line-to-DC-.

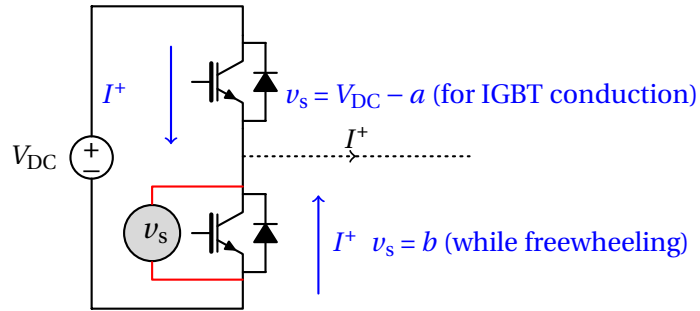


Figure 3.3: The phase A half bridge of the inverter, showing the sensor connection. The purpose of this figure is to demonstrate the paths of current, and how they relate to the voltage measured by the voltage sensor.

### 3.3.2 Extension of the DC Representation to AC

In most applications, alternating currents are applied to the machine. This necessitates the development of an AC waveform representation, of which there are two approaches. The first is representing the AC waveform analytically as was done with the DC PWM signal. The second is representing the AC waveform as many DC PWM waveforms. The holistic analytic representation of the sensor measurement is given in equation (3.5) for a trailing edge PWM signal with natural sampling [18]. The line-to-line quantity can be calculated using equation (3.4). Note that  $f_c$  is the carrier frequency,  $f_1$  is the modulating frequency,  $M$  is the modulating index,  $k$  is the carrier harmonic number,  $n$  is the order of the Bessel function of the first kind,  $T_c$  is the PWM period,  $J_n$  is the  $n^{\text{th}}$  order Bessel function of the first kind, and  $t$  is of course time. Due to the complexity, a DSP cannot calculate this quickly, as this uses many Bessel functions, thus this is avoidable. [15–17]

Instead of this method requiring complex calculation, the other method is explored. The second looks to approximate the AC waveform shown in Fig. 3.5(a) as many DC waveforms, like that in Fig. 3.4. Fig. 3.5(b) gives the current corresponding to Fig. 3.5(a), which is important to note, as this contains both positive and negative currents; this means that all devices in that phase can be measured with this one test. Further, given the range of currents, as long as the amplitude of the current is high enough, the phase leg can be completely characterized. Looking in a local area, as with the circle in Fig. 3.5(a), the DC method can be extended to the AC

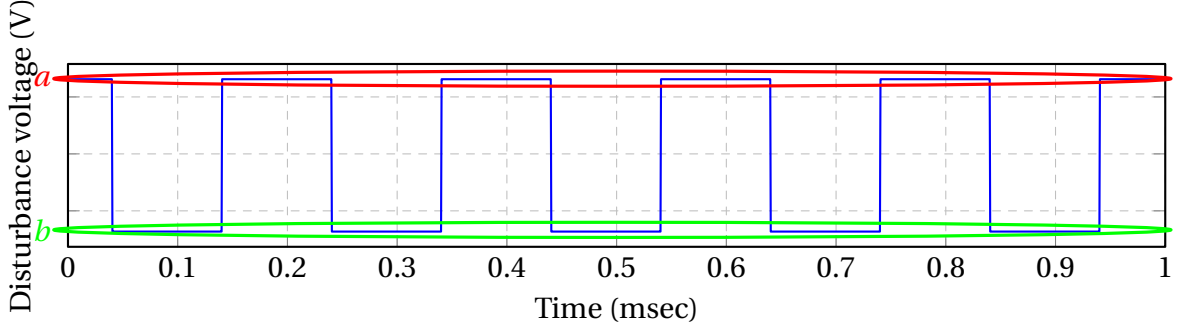


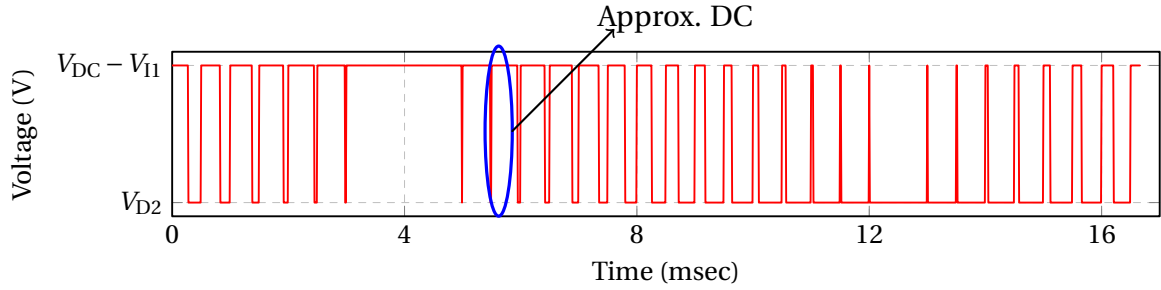
Figure 3.4: Extracted disturbance waveform from raw  $V_{A \rightarrow DC-}$  used in the disturbance estimation methods.

method with no loss of information.

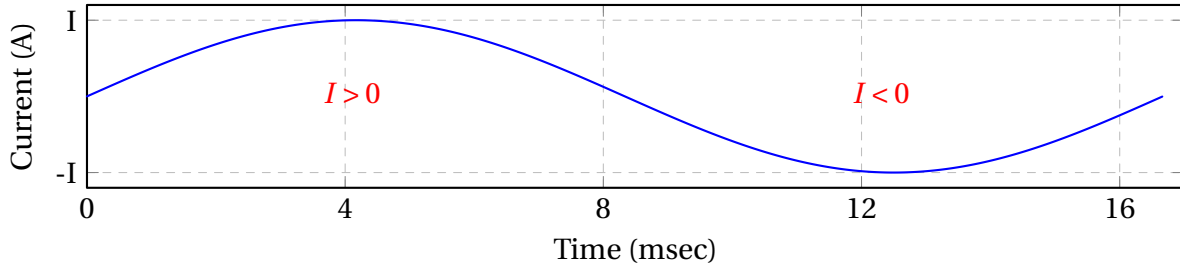
$$\begin{aligned}
 V_{A \rightarrow DC-}(t, M, f_1, V_{DC}, V_{I1}, V_{I2}, V_{D1}, V_{D2}, i_a, f_c) = & \left\{ \frac{1}{2}(\text{sgn}(i_a) + 1) \frac{V_{DC} - V_{I1} - V_{D2}}{2} \right. \\
 & + \frac{1}{2}(-\text{sgn}(i_a) + 1) \frac{V_{I2} - (V_{D1} + V_{DC})}{2} \left. \right\} \{ M \sin(2\pi f_1 t) \\
 & + \sum_{k=1}^{\infty} \frac{2}{k\pi} [1 - (-1)^k J_0(k\pi M)] \sin(2\pi k f_c t) \\
 & - \sum_{k=1}^{\infty} (-1)^k \sum_{n=1}^{\infty} \frac{J_n(k\pi M)}{k\pi} [\sin(2\pi(k f_c - n f_1) t) \\
 & \quad + (-1)^n \sin(2\pi(k f_c + n f_1) t)] \left. \right\} \\
 & + \frac{1}{2}(\text{sgn}(i_a) + 1) \frac{V_{DC} - V_{I1} - V_{D2}}{2} \\
 & - \frac{1}{2}(-\text{sgn}(i_a) + 1) \frac{V_{I2} - (V_{D1} + V_{DC})}{2}
 \end{aligned} \tag{3.5}$$

### 3.4 Methods Utilizing Direct Current

In these DC methods, a direct current goes through one phase, and returns through the other two phases of the machine with half the magnitude. Thus, for a given current command, only the phase with the maximum magnitude is studied. By repeating these tests for every device in each phase, the relationship between voltage nonlinearity and applied current is found. The methods also require the measurement of the: phase duty cycle commands, the phase voltages with respect to the negative DC link, and the phase current, recorded during each sampling period. The methods should also be operable at a sampling rate of 100 kS/sec in order to be



(a) Simulated voltage nonlinearity for an IGBT.



(b) Simulated Voltage nonlinearity for an IGBT.

Figure 3.5:  $V_{A \rightarrow DC}$  measurement for an AC waveform showing the relationship between current and the measured PWM voltage.

realizable in a drive system, since 2 MS/sec is too high for most microcontrollers in drives. As mentioned earlier, a sampling rate of 2 MS/sec is available for experimental and simulated data in order to verify the results. Four seconds of data is available for the simulation and experimental verification. To test the performance of the proposed methods, the high sampling rate data was used to estimate the voltage disturbance by taking the average of the top and bottom of the square disturbance waveform shown in Fig. 3.4 over four seconds. This is done by averaging all upper values, defined whenever the voltage is above zero; for the bottom, this is done by averaging the voltage when it is below zero.

### 3.4.1 Method Utilizing the Waveform Mean

The first method attempted utilizes the fact that the mean of this square wave disturbance signal ( $\mu_x$ ) along with the duty cycle ( $D$ ) contains information about the nonlinearity at that spe-

cific current, seen by this equation (3.6).

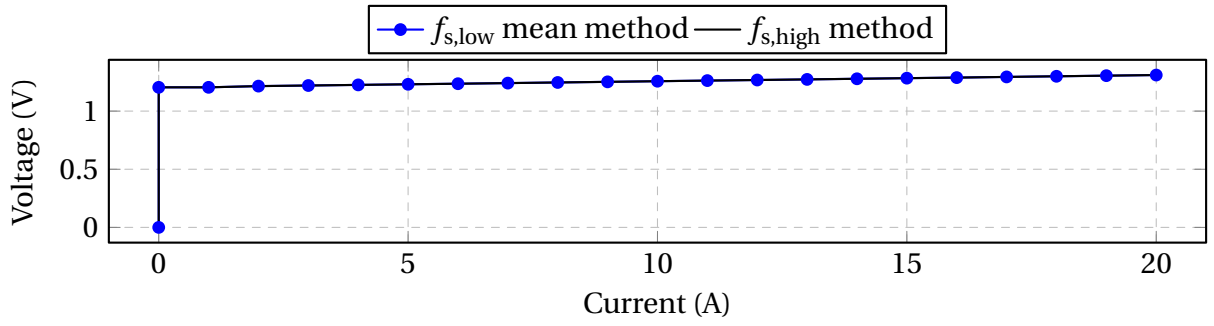
$$\mu_x = (1 - D)(b) + (D)(a) \quad (3.6)$$

While this equation contains both nonlinearity terms  $a$  and  $b$ , another equation is required to find both quantities. This can be accomplished by artificially increasing the duty cycle command in each phase in order to create two equations for the two unknowns. The measurement is taken once, and then a second time by adding 5% to the duty cycle of each phase PWM command. By manipulation of the basic duty cycle equations from these two tests, the nonlinearities at a given current can be found by equation set (3.7). The method is first tested in simulation with the voltage measurement, duty cycle commands and equations in (3.7). This test is repeated for one phase for demonstration, at all currents from 0 to 20 A in steps 1 A. The method performs well in simulation as seen in Figs. 3.6(a) and 3.6(b), matching the high sampling frequency results. Experimentally, calculation of the mean of the square wave is very susceptible to noise in the data, which is seen in the resulting nonlinearity waveforms of Figs. 3.6(c) and 3.6(d). The higher order harmonics of the PWM switching frequency cannot be filtered; doing so would produce a signal which is no longer a square wave and thus invalidate the analysis in equation (3.7).

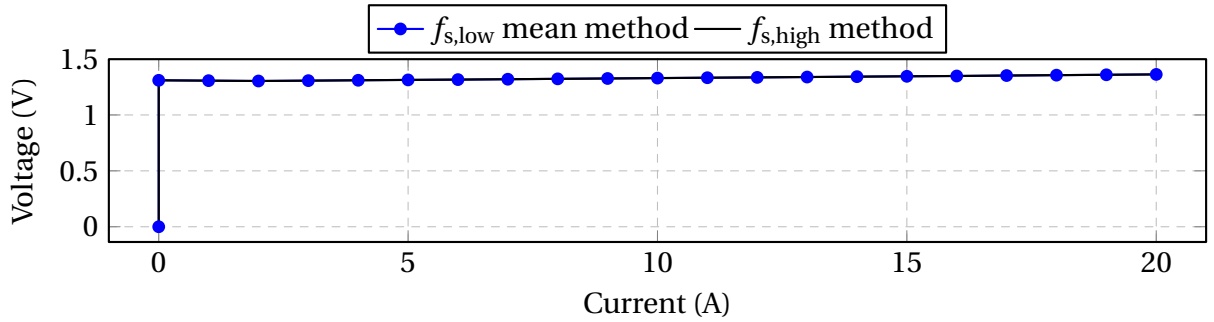
$$\begin{aligned} \frac{D_2}{D_1}\mu_1 - \mu_2 &= b \left( \frac{D_2(1-D_1)}{D_1} - (1-D_2) \right) \\ b &= \frac{\frac{D_2}{D_1}\mu_1 - \mu_2}{\frac{D_2(1-D_1)}{D_1} - (1-D_2)} \\ a &= \frac{\mu_1 - (1-D_1)b}{D_1} \end{aligned} \quad (3.7)$$

### 3.4.2 Method Utilizing the Waveform Spectrum

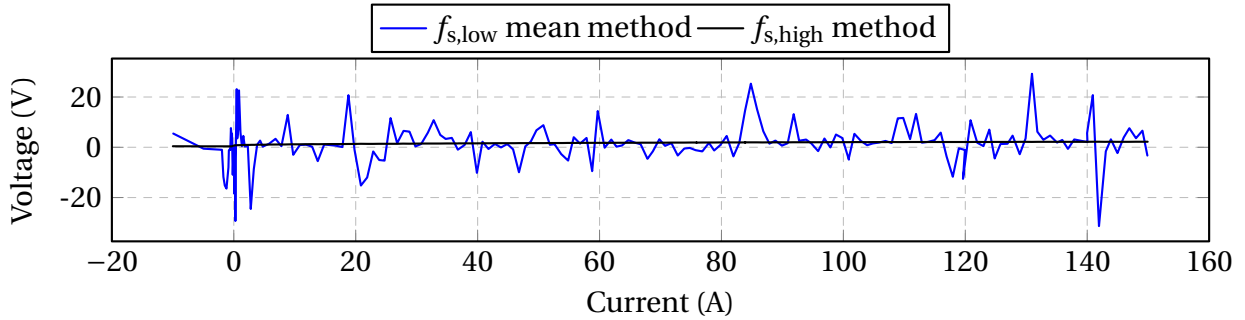
Given that the mean method is fairly noise-prone, another method is required that is less prone to noise, using the same conditions of the mean method. The Fourier spectrum of the PWM



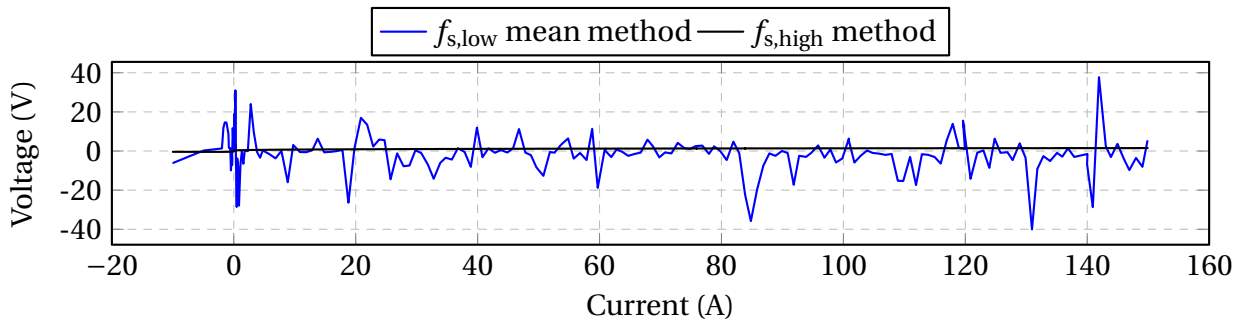
(a) Simulated voltage nonlinearity for an IGBT.



(b) Simulated voltage nonlinearity for a diode.



(c) Experimental voltage nonlinearity for an IGBT.



(d) Experimental Voltage nonlinearity for a Diode.

Figure 3.6: The resulting simulation and experimental waveforms for voltage nonlinearity with the mean method.



waveform was therefore investigated to find the disturbance values, since, if no aliasing occurs, the spectrum harmonics should not reflect high frequency noise. The discrete Fourier transform of the disturbance waveform in equation 3.9 was found with an analytic expression for this waveform in equation 3.8. Note that  $N_1$  in equation 3.10 represents the number of samples to the right of the halfway point of the positive portion of the PWM signal, including the middle.

$$x[n] = au[n] - (a - b)u[n - (DN + 1)] = x[n + N] \quad (3.8)$$

$$x[\hat{k}] = b + \frac{a - b}{N} ((2N_1 + 1))\delta(k) + \sum_{k=1}^{N-1} \frac{\sin(\frac{2\pi k(N_1+0.5)}{N})}{\sin(\frac{\pi k}{N})} \quad (3.9)$$

$$N_1 = \lfloor \frac{[DN] + 1}{2} \rfloor \quad (3.10)$$

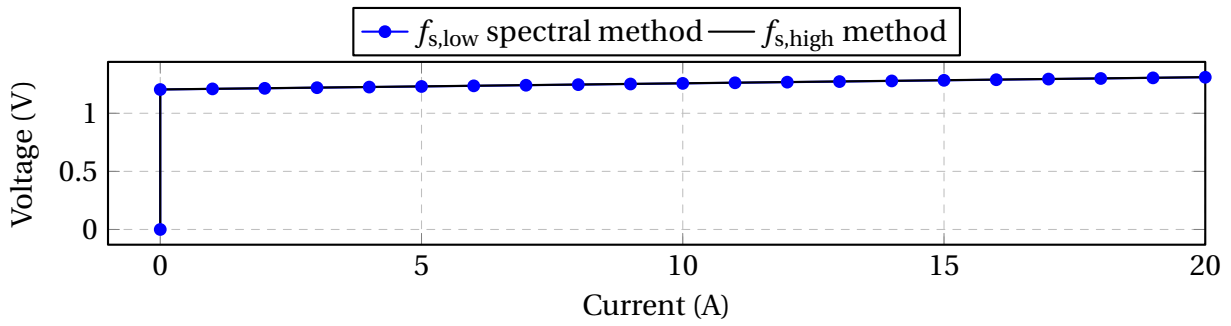
Given this, the nonlinearity can be calculated with the DFT and FFT as in equation (3.11) results given in Fig. 3.7(a) and 3.7(b) in simulation, as well as 3.7(c) and 3.7(d) experimentally. For this method to work, the spectral component at the switching frequency (FFT(1)) and DC component (FFT(0)) of the FFT must be computed in the embedded system, with an algorithm such as the Cooley-Tukey algorithm. This method can, with some loss of precision due to noise, effectively estimate the inverter nonlinearities for a given applied direct current.

$$b = \text{FFT}(0) - \frac{(N)\text{FFT}(1) \frac{\sin(\frac{\pi}{N})}{\sin(\frac{2\pi}{N}(N_1+1/2))}}{N} (N_1 + 1) \quad (3.11)$$

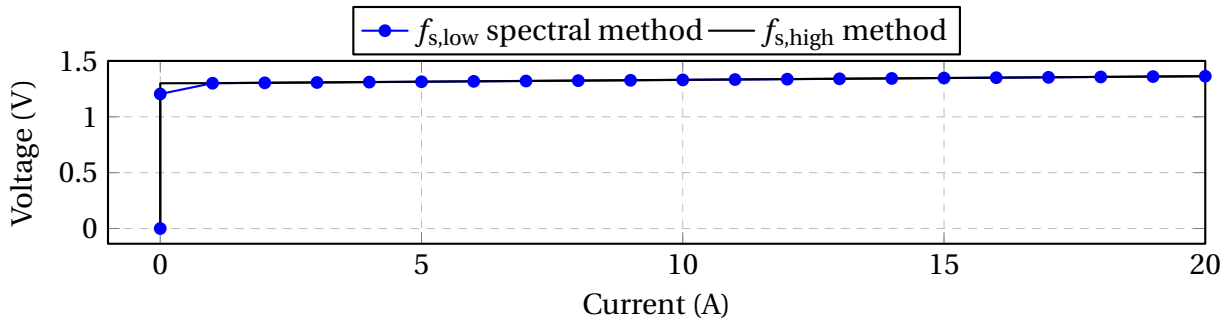
$$a = (N)\text{FFT}(1) \frac{\sin(\frac{\pi}{N})}{\sin(\frac{2\pi}{N}(N_1 + 0.5))} + b$$

### 3.5 Methods Utilizing Alternating Current

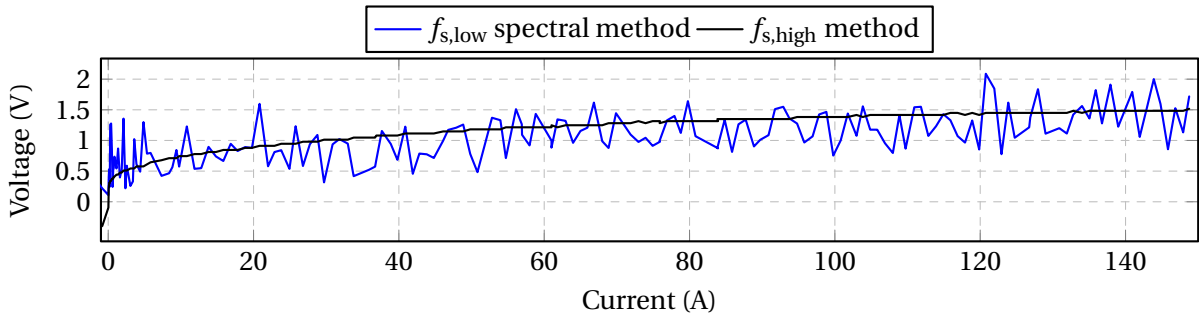
Application of the analytic procedure used in the DC spectral method to the alternating current case is nontrivial, given the complex analytic representation in equation (3.5). Calculation of the Fourier series of an AC PWM waveform is impractical as discussed in section 3.3.2 and is



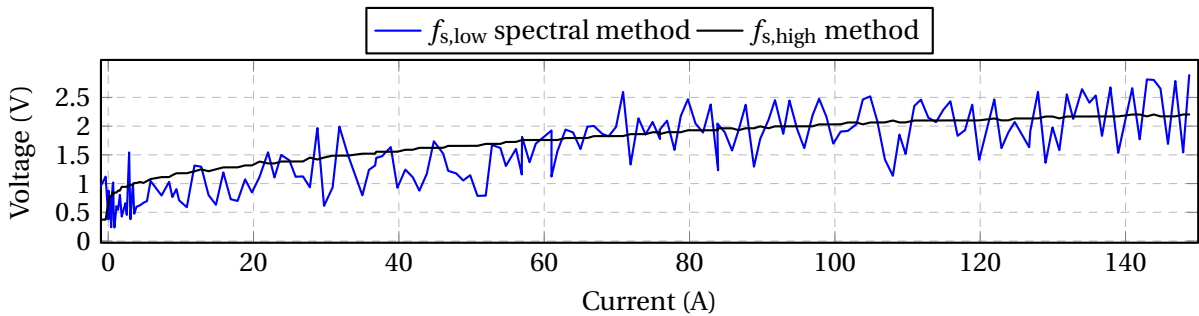
(a) Simulated Voltage nonlinearity for an IGBT.



(b) Simulated voltage nonlinearity for a diode.



(c) Experimental voltage nonlinearity for an IGBT.



(d) Experimental voltage nonlinearity for a Diode.

Figure 3.7: The resulting simulation and experimental waveforms for voltage nonlinearity with the spectrum method.

thus impractical for DSP or microcontroller use. To test the performance of the proposed AC methods, the high sampling rate data was used to estimate the voltage disturbance by reading the voltage levels from the data directly. This is done in a similar manner as the DC high frequency method, but is not average over a long period, but only uses measurements at the appropriate current level and direction.

### **3.5.1 Method Using Developed Algorithm**

Instead, the direction of current and voltage levels will be used to observe the voltage with respect to current, and finding the current and voltage relationship from this. In Fig. 3.5(a), the nonlinear disturbance voltage of phase A is shown with respect to the current without the DC link subtracted. This waveform contains voltage data for both directions of current, so it is possible to characterize the top and bottom IGBTs, as well as their respective freewheeling diodes. Additionally, the voltage PWM waveform, allows us to isolate the IGBT and the diode from one another. The fact that we have all of this with respect to current allows us to, for each point, associate the voltage disturbance with the current in the device. If values of the current are associated with their respective voltage values, a model can be easily constructed for each device. In implementation, only integer valued currents are stored, by rounding all current readings to the nearest integer (this reduces the number of points in the model). Then, the voltage associated with that rounded current value is added, with a mean calculation, to the running mean calculation for that current value. The flowchart in Fig. 3.8 shows the algorithm to find the appropriate voltage with respect to current. The inverter can be characterized by one alternating current point, if a sinusoidal current of peak amplitude is applied (which is the maximum peak current of the inverter), as every intermediate current is also contained in that data.

The results in Figs. 3.9 and 3.10 match well to what is expected by observing the high frequency PWM waveforms. Here the values have been averaged, and as such there is only one line for either set of data.

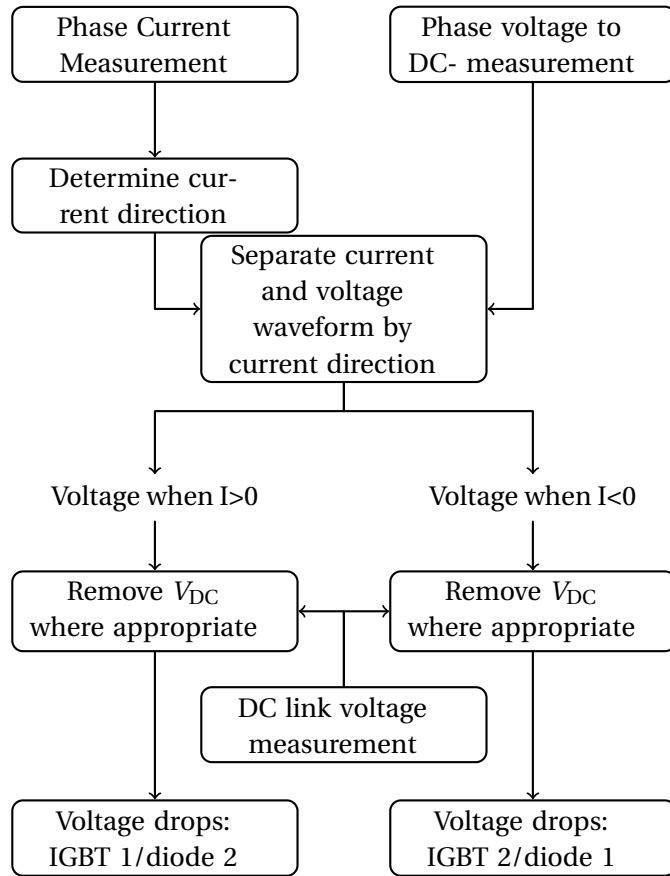
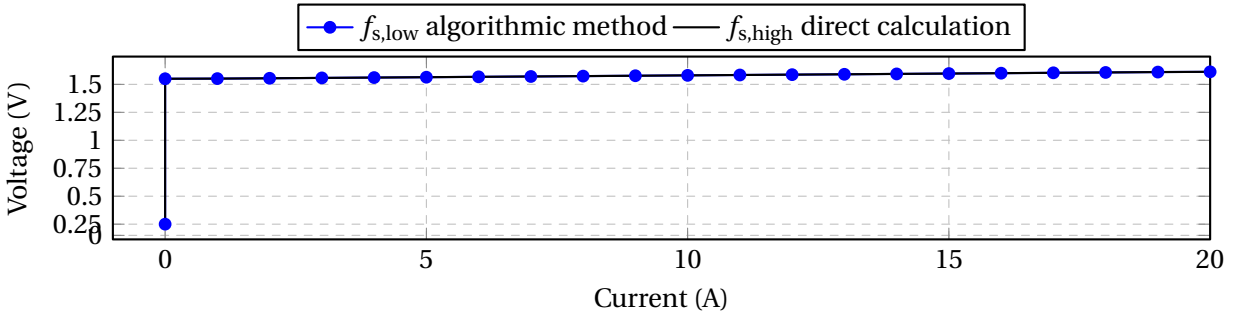
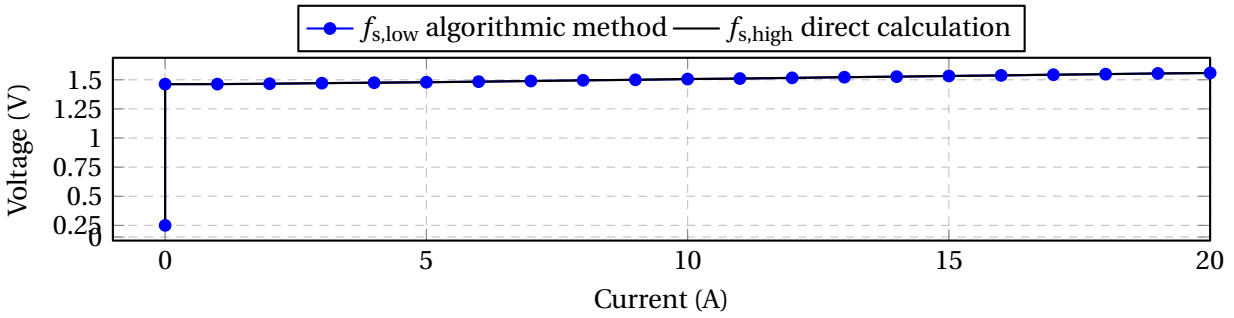


Figure 3.8: Characterization method used to determine the voltage and current relationship of inverter devices.

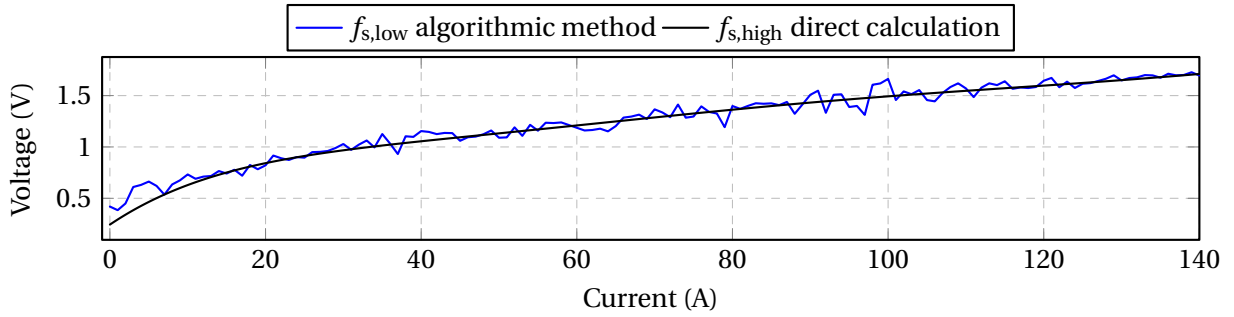


(a) IGBT characteristic curve.

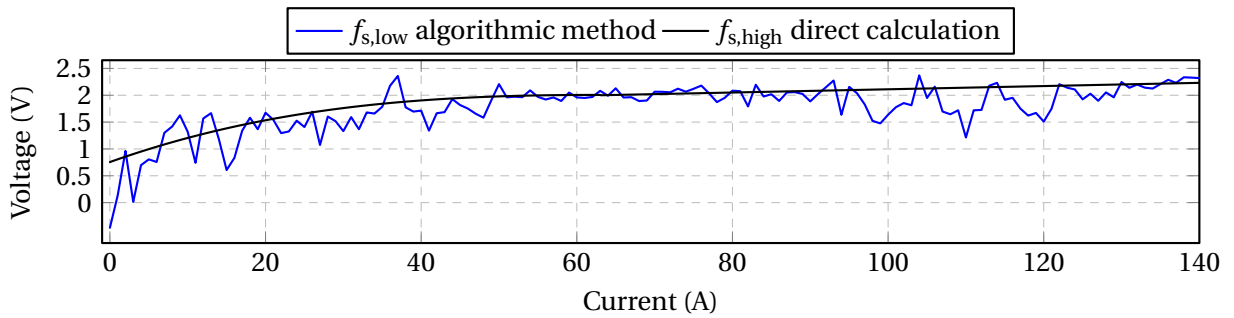


(b) Diode characteristic curve.

Figure 3.9: Simulation results of nonlinearity voltage drop spectrum extraction.



(a) IGBT characteristic curve.



(b) Diode characteristic curve.

Figure 3.10: Experimental results of nonlinearity voltage drop spectrum extraction.

### 3.5.2 Method Using DC Approximation with STFT

The problem with the application of the spectral method to the AC signal, is that the spectral method calculates the FFT for the entire range of data, which is typically a stationary signal. A stationary signal is one in which the harmonics do not change in time; with a varying duty cycle waveform like in ACPWM, this is not the case. It is possible to calculate the FFT of the entire signal, but the current/voltage relationship would be lost, as the harmonics are for the entire length of time. Taking the FFT in a localized region would remedy this, if we could take the FFT in the local DC-like area. This is possible with the Short Time Fourier Transform (STFT), which does this using equation (3.12) [19].

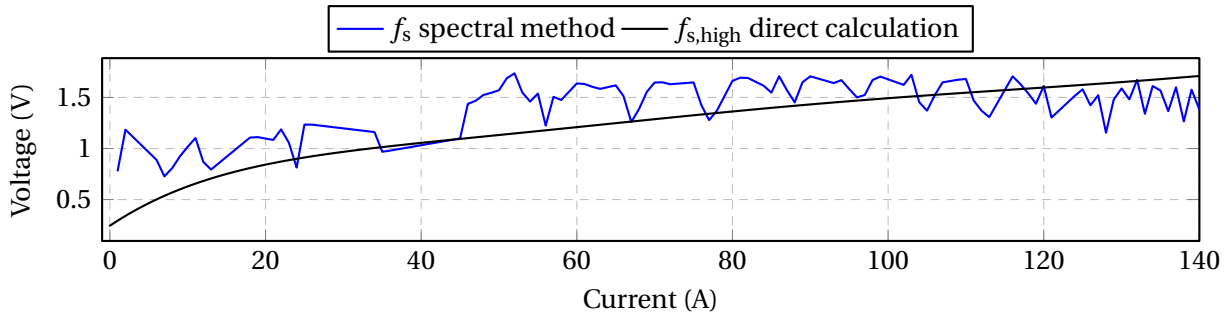
$$\text{STFT}(t, f) = \int h(t - \tau) s(\tau) e^{-j2\pi f\tau} d\tau \quad (3.12)$$

Note in equation (3.12), the  $h(t - \tau)$  term is a window function. The window function is how the time data is broken up, and must be chosen to appropriately balance the time period (T) and frequency bandwidth (B), as there is a tradeoff between the two of these.

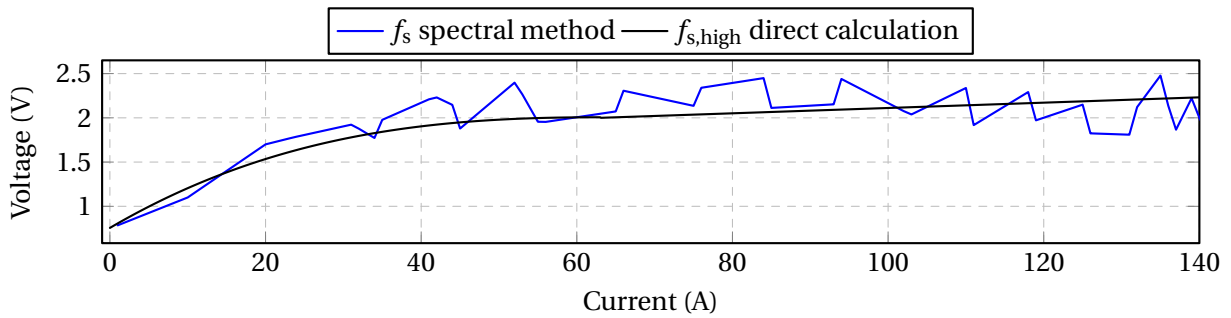
$$TB \geq \frac{1}{2} \quad (3.13)$$

The takeaway is that equation (3.13) defines the tradeoff between information in the time domain, and information in the frequency domain. The matlab function *spectrogram* is used with a *window* size to be five times the number of samples per period, *overlap*, and *nfft* is set to the *window* size. A rectangular window is used in order to match the FFT results instead of the Hamming window.

The DC method equations given by the equations in (3.11) are used with the spectrum information found using the STFT to arrive at the results of Figs. 3.11(a) and 3.11(b). The methods are only applied to the phase A positive current quantities, IGBT1 and Diode2, although all devices can be characterized using this method.



(a) IGBT characteristic curve.



(b) Diode characteristic curve.

Figure 3.11: Experimental results of nonlinearity voltage drop spectrum extraction for AC using STFT.

### 3.6 Conclusions

In this paper, a novel inverter characterization procedure is investigated. The benefit of this method over those in literature lies in its ability to identify individual device parameters, an important goal in inverter health monitoring. The mean method was introduced, but the fact that it was noise-prone hampered the performance of this method. The benefit of the spectral method is that it is an effective, noise-resistant method of characterization. With the spectral method, and an adequate fast Fourier transform in the embedded system, the nonlinearities of interest are easily found with only some effects of noise. This is extended to the alternating current case by way of the STFT. With the simulated and experimental work, these methods prove useful for the monitoring of inverter nonlinearities with both direct and alternating current.

# Chapter 4

## Manuscript for ECCE 2014: “Effects of Detailed Nonlinearity Characterization upon Condition Monitoring”

### 4.1 Introduction

#### 4.1.1 Motivation and Background

Electric drive systems, and the inverters that accompany them are quickly becoming ubiquitous in applications ranging from home appliances, to the aerospace and automotive sectors. Inverters are not only used to operate traction drive systems, but also the electric machines which are replacing automotive and aerospace systems which were previously hydraulic. This comes with added benefits, but the chief concern is guaranteeing that the systems are reliable.

Industry agrees with this notion [20], saying that the field of condition monitoring and reliability studies in general needs to be expanded upon to allow for the greater proliferation of reliability methods. This holds most true for capacitors and power devices in the inverter, reported to be the most fragile, or failure-prone. Given their applicability to drive systems, MOSFETs and IGBTs were reported to be of the most interest. Since IGBTs typically have a higher power rating and so are used more often in traction drive systems, the discussion in this paper will be limited to IGBTs. Further, the duty of these devices is such that they are typically used daily, making reliability important in order to prevent downtime. Being able to predict and determine the problem ahead of time would allow for a shorter downtime if the catastrophic failure can



be avoided, as well as less expensive repair cost if the system can perform the diagnostic itself. Note that the interest is in the ability to detect a failure in an inverter correctly and as early as possible [19]. This failure typically shows some observable signature before the failure occurs. The fault is defined as this early detectable condition which allows for continued operation but will lead to a catastrophic failure of the system.

#### **4.1.2 State of the Art**

The summary works of [2] and [1] give an overview of the field of inverter reliability studies, still in its early stages. The basic reliability information is surveyed, the various reliability prediction metrics are discussed as well as assessments. Additionally, [18] clearly explains the four main areas of reliability design:

1. diagnosis
2. prognosis
3. fault mitigation
4. redundant or fault-tolerant design

These four areas provide tools useful in the attempt to improve reliability.

##### **4.1.2.1 Diagnosis**

Diagnosis is the term for the determination of the presence and severity of a fault in a system. This is the most mature portion of the field of reliability; many methods have been discussed in literature. The work in [21] involves a method which finds the current vector trajectory, and uses deviations in this to identify the faulty switch. The paper [22] monitors low order harmonics introduced by faulty switching due to poor solder bonding to determine whether solder fatigue exists. [23] uses a measure similar to the equivalent resistance of a phase in order to detect the presence of a fault with the measured currents and voltage commands. Semikron developed a simple circuit in [24] to determine whether a bond lift-off was worsening or had lifted

off completely. The work [25] also uses an external circuit to measure the on-state resistance of the devices in order to detect whether a fault is taking place. In [26] intermittent misfiring is represented as pulses in the machine model and is manifested in the torque-producing component of the machine current. The paper [27] determines whether an open-circuit of a device is occurring by monitoring the  $V_{CE}$  of the lower switch.

#### **4.1.2.2 Prognosis**

Prognosis is the study which seeks to determine the time until the final catastrophic failure, as well as the probability of it occurring and worsening, for a particular fault. Ideally, a prognostic method would be able to determine the amount of time or cycles that the device has before the fault becomes substantial and catastrophic failure occurs. [28] measures the gate current required to operate and is able to build a predictable failure model with this. This does however require expensive sensing which is not typically in place in an inverter. By doing power cycling testing and observing the  $V_{CE}$  quantity at each cycle, [3] was able to determine a pattern for change in  $V_{CE}$  that could be used to predict failure of an IGBT.

#### **4.1.2.3 Fault Tolerant Design**

Fault-tolerant design is the design of a system such that the system is resistant to failure. Redundancy is the typical example of this with multilevel inverters in [29–33]. But as this work seeks to leave the inverter intact, this reliability tool will not be investigated.

#### **4.1.2.4 Fault Mitigation**

Mitigation is the change in operation, such as operating at a lower power, in order to allow for some limited operation in the presence of a fault. Fault mitigation is typically applied to the aforementioned redundant topologies, since there are IGBTs that can operate in place of the failed IGBTs. Again, this work focuses on diagnosis and prognosis, so this is not investigated. The state of the art of remedial strategies is discussed in [2].

### **4.1.3 Aim of This Work**

This paper determines the effect of inverter nonlinearities on an example condition monitoring scheme of an inverter. The method both diagnoses the existence of a fault, determines its severity, and determines how much remaining life exists in the inverter. There are two main goals: improving prognosis with the study of nonlinearities, and improving diagnosis with this study. With this, the first task is to find a method which accurately determines the existence of a fault and its severity. This is done by finding a relationship between the device characteristics and the fault status, as well as the phase voltage harmonics and the fault status. The study of inverter nonlinearity can improve this by estimating the fault level directly, or improving a more traditional method. With diagnosis complete, the prognosis portion of the work begins. With the relationship between the device characteristics, operating cycle and fault status, the paper finds a prognostic model which can estimate the remaining useful life of each device. This is improved upon using the aforementioned diagnostic methods. The benefit of these diagnostic and prognostic methods is that they can find the fault status and remaining useful life of every IGBT and diode in the inverter given an accurate model. This does not average values or view a phase as one unit. This means one could see a small difference in one device, and possibly service the part or operate in a limited capacity.

### **4.1.4 Outline**

The paper is organized according to the various methods used in the condition monitoring. The structure is given by the following:

- Section 4.2 discusses inverter modeling, both the nonlinear voltage and fault modeling. Additionally, the experimental implementation of the bond wire lift-off is discussed.
- Section 4.3 discusses the diagnostic procedures performed in this paper: characterization and classification of fault into discrete fault levels.
- Section 4.4 discusses the chosen reliability model. Additionally, it introduces the relationship between the fault progression and the device characteristics. It then discusses

the prognostic approach using the chosen reliability model.

## 4.2 Inverter Modeling

### 4.2.1 Relationship Between Fault and Measured Quantities

In order to determine the type of fault that exists based upon the characterization data or other methods, a relationship between the fault and the measured quantities must be understood. The measured quantity here is  $V_{CE}$ , and the saturation region voltage,  $V_{CE,sat}$ , is of interest given that the resistance is to be found to detect a fault. In the saturation region of the device, the voltage can be represented by the different contributions from the various device effects in equation (4.1) [34]. There are four contributions to the total forward voltage in the saturation region:

1. The junction drop (Boltzmann approximation)
2. the voltage drop across the lightly doped storage region
3. the voltage drop over the space charge region
4. the ohmic voltage drop due to the bond wire

$$V_{CE,sat} = V_{p+n-} + V_B + V_{MOS} + V_{bondwire} \quad (4.1)$$

In the junction voltage drop, the  $n_i$  is the intrinsic carrier concentration,  $V_T$  is the MOS-gate threshold voltage, and  $p_{x1}$  and  $p_{x2}$  refer to the excess carrier concentrations at the p+ side and p-body side, respectively.

$$V_{p+n-} = V_T \ln \left( \frac{p_{x1} p_{x2}}{n_i^2} \right) \quad (4.2)$$

The drop over the lightly doped storage region depends upon the collector current  $I_C$ , the doping concentration in the drift region  $N_B$ , the silicon area  $A_{Si}$ , the excess carrier concentration  $p(x)$ , the electron mobility  $\mu_n$ , and the hole mobility  $\mu_p$ .

$$V_B = \frac{I_C}{q A_{Si}} \int_{x=0}^W \frac{dx}{p(x)(\mu_n + \mu_p) + \mu_n N_B} \quad (4.3)$$

The voltage drop over the space charge region depends upon the aforementioned excess carrier concentration in the p+ body side and K, a large constant given by the semiconductor manufacturer.

$$V_{\text{MOS}} = \begin{cases} 0 & \text{if } p_{x2} > 0, \\ K p_{x2} & \text{if } p_{x2} < 0. \end{cases} \quad (4.4)$$

Finally, the bondwire voltage drop is the ohmic drop due to the wires bonded to the semiconductor. This depends upon the resistance and temperature coefficient of resistance at 20°C as well as the measured temperature  $\theta$ .

$$V_{\text{bondwire}} = I_C R = I_C R_{20} (1 + \alpha_{20}(\theta - 20)) \quad (4.5)$$

#### 4.2.2 Chosen Example: Bond Wire Lift-Off

Because the bond wire lift-off is the most common failure mode [1], this failure mode will be the principal concern of this paper. The lifted bonds can clearly be related to the equation for forward voltage, especially the resistance equation given in (4.5). Here, the resistance is clearly shown in relation to the output voltage.  $V_{\text{bondwire}}$  is however not the only voltage quantity that depends upon the current, since the term  $V_B$  has this dependency, too. It is assumed that the resistance term dominates the drop over the lightly doped storage region.

With this information, it is necessary to build a simple bond lift-off model which can be used to show the benefits of the study of inverter characterization and the study of nonlinearities. Given that the resistance can be used for the bond wire lift-off, the voltage equation which depends upon resistance is used. The chips have a structure where each chip's emitter has multiple bond wires attached to it, while the collectors are usually connected at the chip-level. These connectors form a parallel connection between the external emitter connection and the chip with a resistance of  $R_i/m$  where  $m$  is the number of wire bonds connected to the chip. This means that as each connector breaks, the resistance increases. Furthermore, it is typical for different chips to be connected in parallel, but this does not change the fact that the resistance

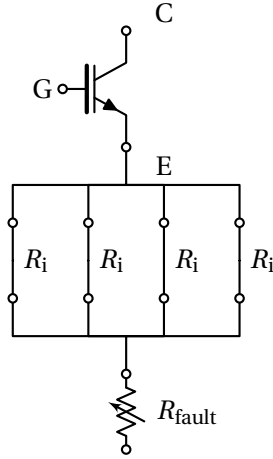


Figure 4.1: An IGBT with bond wires and their resistance with added fault resistance.

Table 4.1: Experimental observations for diagnostic and prognostic nonlinearity evaluation.

fault	Freq Hz	$I_{\text{Range,lin}} \text{ A}$	$I_{\text{Range,non}} \text{ A}$
Nom	60, 120, 180	0, 10 ... 40	50, 75 ... 150
$f_1$	60, 120, 180	0, 10 ... 40	50, 75 ... 150
$f_2$	60, 120, 180	0, 10 ... 40	50, 75 ... 150
$f_3$	60, 120, 180	0, 10 ... 40	50, 75 ... 150
$f_4$	60, 120, 180	0, 10 ... 40	50, 75 ... 150

depends on the  $m$  term, representing the number of bonds for all chips which are parallel in a given phase. Bonds may partially break before finally lifting, but the effect of this is left for future work; partially lifted bonds are discussed in [1, 35, 36].

### 4.2.3 Imposition of Artificial Faults for Simulations and Experiments

Experiments are performed by controlling current in an induction machine using the SEMIKRON inverter.

Experiments are conducted by applying currents of different magnitudes and frequencies; this is done for different fault levels by adding a resistor in series with one of the phases as in Fig. 4.1. The resistors placed in series are given by Table (4.3).

Table 4.2: Experimental resistances added.

	Nominal	Short	3/3	2/3	3/3
$R_{\text{fault}}$	0 m $\Omega$	4 m $\Omega$	13 m $\Omega$	17 m $\Omega$	24 m $\Omega$

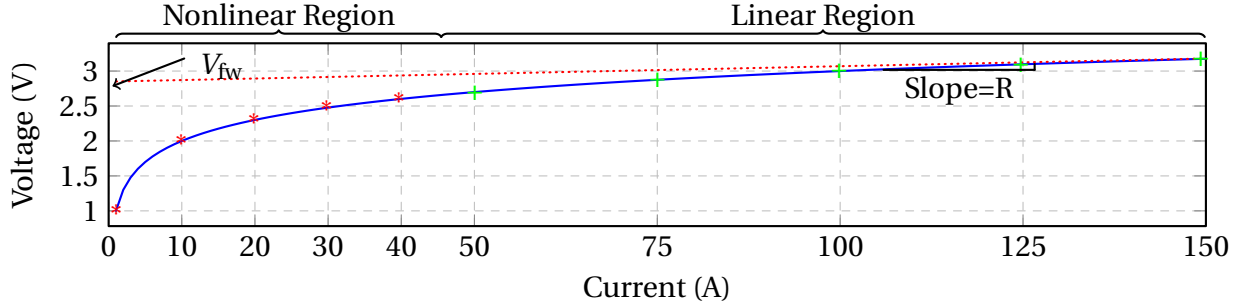


Figure 4.2: Waveforms showing a generalized semiconductor nonlinearity are given as its VI characteristic and the linear approximation to this with its equivalent parameters; this is the key characteristic for a device. The nonlinear and linear region points are shown.

### 4.3 Diagnosis

Diagnosis is first performed with characterization, for a typical, off-the-shelf classification case, and then for the typical diagnostic procedure considering the device nonlinearity. It is possible to estimate the resistance by inverter characterization, and with accurate enough characterization, this suffices. This is done by determining the relationship between the voltage and current of the devices in the inverter, and then the equivalent resistance in the saturation region of the device. However, if one is unable to characterize the inverter online, another method can be used to detect fault severity. This could occur if only the phase voltage instead of the phase to negative DC link voltage measurement is not available, a requirement for characterization of each device. A typical method uses the harmonics which the device characteristics depend on; this is possible because they change with respect to the parameters, and therefore fault level. The harmonics are determined with the fast Fourier transform, which estimates the harmonic content and exports frequency data in the form of coefficients for use in diagnosis and classification. A typical fault classification method uses the harmonics directly. With harmonic data from faulted inverters, a classifier can be used to determine the direct relationship between harmonics and the number of lifted bonds. This method should be able to classify a bond lift-off from other possible effects, such as heating of the entire IGBT module during operation.

This method can be enhanced if the inverter is initially characterized offline, since training the classifier with only linear values can improve the classification percentage.

### 4.3.1 Characterization Diagnosis

Measuring the resistance of the devices directly will allow for the diagnosis of bond wire lift-off faults, because this would allow measurement of the effect of bond wires lifting, and the resistance increasing. This is done by measuring the linear range of the V-I characteristic of the device, and therefore the resistance, as is given in Fig. 4.2. Doing this, accurate information about the fault is found. Overall, with the ability to determine the V-I characteristic of all of the devices in an inverter, it is possible to determine whether bonds have lifted off in any of the devices.

Practically, this is carried out with the procedure in Fig. 4.3, which can determine the characteristics of each device in an inverter. This is done by measuring the current and phase voltage with respect to the negative DC link voltage, given in Fig. 4.4. Using the case of phase A with positive current, the top IGBT and bottom diode can be characterized. When the current is positive and the IGBT is conducting, when the voltage of the measured PWM waveform is near the DC link, the IGBT voltage at that given current can be found by solving for  $a$  in the equation in Fig. 4.4, where  $v_s$  is the voltage measurement with the sensor placed across the phase to the negative DC link. When the diode is conducting, and the measured voltage of the sensor is near zero, the diode voltage is the negative of the measured voltage. With an AC waveform, if these calculations are performed to find the device voltages during each PWM period, the entire current range information can be measured, which results in the plots in Fig. 4.5. The plots in Fig. 4.5 give the voltage and current relationship for the entire range when a balanced three phase sinusoidal current with a magnitude of 140A is applied to each phase of the inverter. Each of these plots contains the information to calculate the resistance in each fault case by determining the slope of these waveforms in the linear region. By determining the equation of the linear approximation to the nonlinear curve, as is shown by the dotted line in Fig. 4.2, the forward voltage and equivalent resistance is found. The result of this test for the top IGBT and bottom



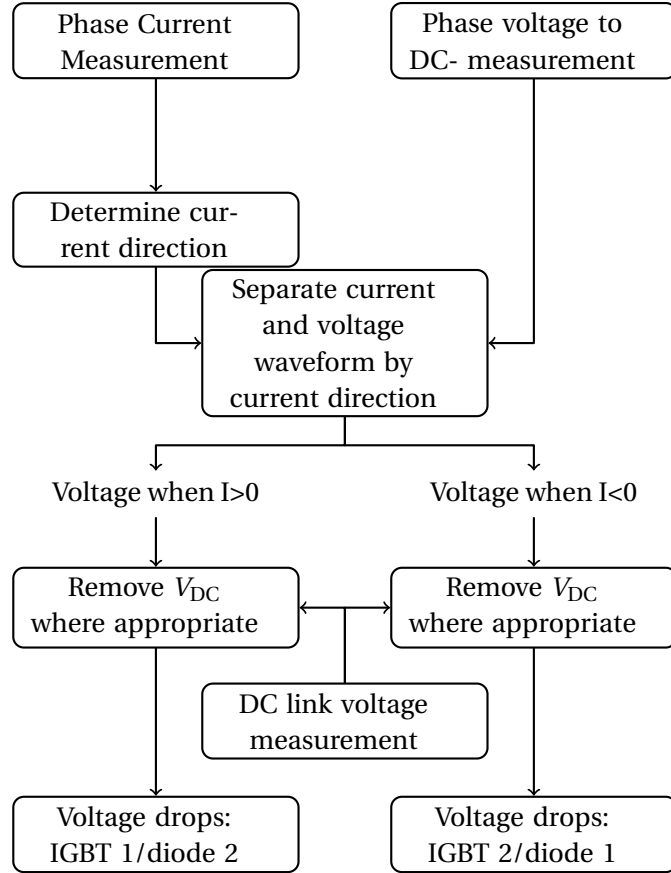


Figure 4.3: Characterization method used to determine the voltage and current relationship of inverter devices.

diode of phase A are given in Table 4.3. Using this information, it can be seen that the different resistances added to simulate the fault are clearly detected.

Table 4.3: Linearization of device nonlinearity with added fault.

	Healthy	$f_{R0}$	$f_{R1}$	$f_{R2}$	$f_{R3}$
$R_{\text{fault,d}}$	5.7 m $\Omega$	11.5 m $\Omega$	17.2 m $\Omega$	20 m $\Omega$	26.4 m $\Omega$
$V_{\text{fault,d}}$	0.85 V	0.71 V	0.70 V	0.66 V	0.67 V
$R_{\text{fault,i}}$	5.7 m $\Omega$	10.4 m $\Omega$	18.7 m $\Omega$	19.8 m $\Omega$	27 m $\Omega$
$V_{\text{fault,i}}$	1.53 V	1.86 V	1.52 V	1.87 V	1.77 V

### 4.3.2 Linear Discriminant Classifier

A second type of classification is achieved using the Linear Discriminant Classifier (LDC). The LDC is initially trained with a set of features. In each set of features, the amount of resistance

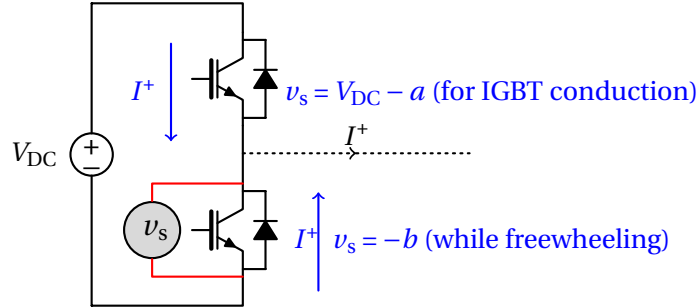
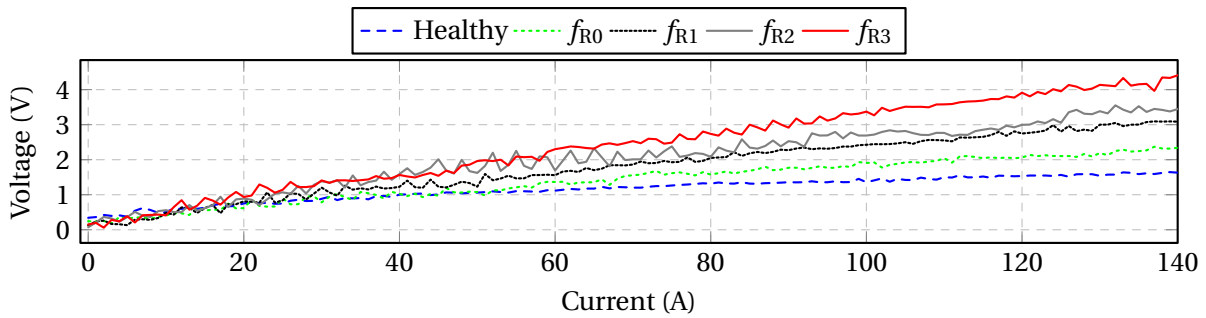
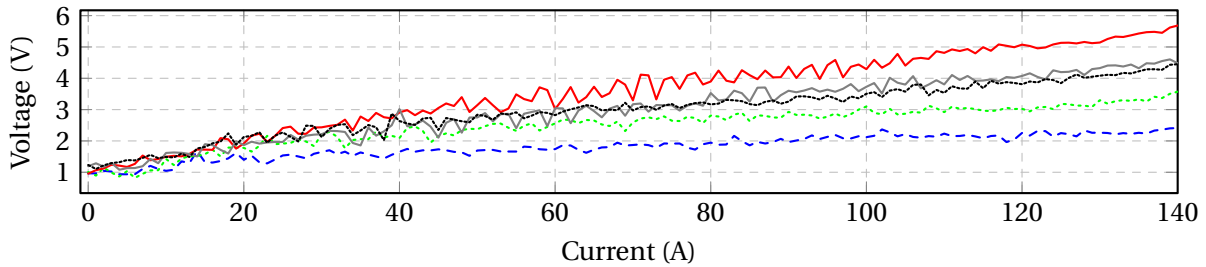


Figure 4.4: The phase A half bridge of the inverter, showing the sensor connection. The purpose of this figure is to demonstrate the paths of current, and how they relate to the voltage measured by the voltage sensor.



(a) Diode characteristic curves.



(b) IGBT characteristic curves.

Figure 4.5: Experimental results of device characterization under different fault levels.

is known, and this is used to train the LDC. The LDC works to maximize the statistical separation between the different fault cases by computing a set of coefficients for the features, and maximizing the coefficients for that class. Thus, when an unknown is tested, whatever linear discriminant function is the largest determines how it is classified. The discriminant function is defined in equation (4.6).

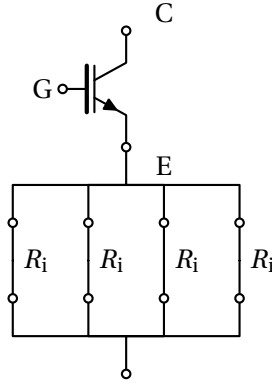


Figure 4.6: An IGBT with bond wires and their resistance.

$$D_C(x) = x_1 \alpha_{1C} + x_2 \alpha_{2C} + \dots + x_k \alpha_{kC} + \alpha_{1C} \quad k = 1, 2, \dots, C \quad (4.6)$$

Note that  $C$  is the number of classes,  $x$  is the feature vector,  $\alpha_{kC}$  is the feature  $k^{\text{th}}$  coefficient for the class  $C$ . A feature vector is classified as class  $j$  if the discriminant function for one class is greater than the discriminant function value for all of the other classes as in equation

$$D_j(x) > D_k(x), \quad k \neq j \quad (4.7)$$

Instead of using the effect of the bond wire lift-off on resistance directly as in the characterization approach, the classifier uses multiple training cases to be able to determine the state of a device of unknown fault level. This is done by gathering spectral information, generating the fast Fourier transform coefficients, and training for test cases where the fault severity is known. The most discriminative frequencies, or features must be chosen. The change in fault level, or here resistance, is represented by the breaking of wire bonds, here assuming for discussion only that there are four wire bonds per phase as in Fig. 4.6. Therefore the nominal has four attached and thus a resistance of  $R_i/4$ . When one detaches the resistance becomes  $R_i/3$ , then for each subsequent detachment the resistance becomes  $R_i/2$ ,  $R_i$ , and then finally an open when all bonds break. To get the faulted cases, a resistance is added in series with phase A. The phase A voltage is then used for the generation of harmonic information. In the experimental case here, the various resistances in Table (4.3) are added.

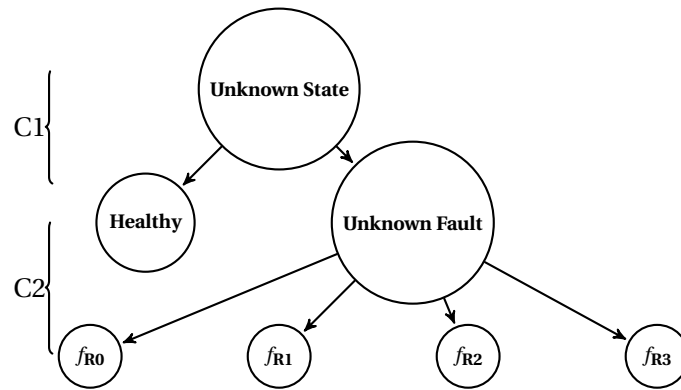


Figure 4.7: Classification algorithm ; the C1 classification step determines whether any fault exist, while the C2 step determines the severity of the fault.

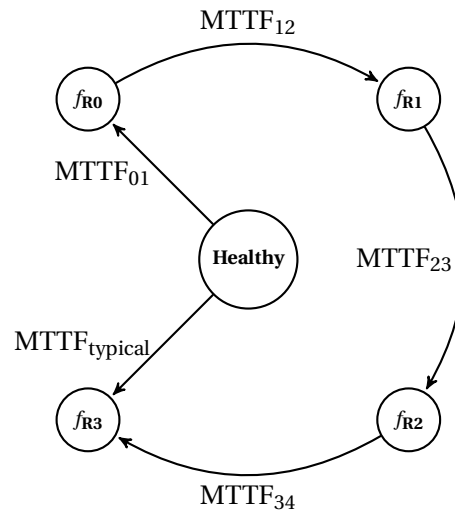


Figure 4.8: Paths to failure for bond wire lift-off in one phase of an IGBT inverter system.

The matlab function *classify* is used to train the classifier. All of these cases are then gathered except one of them, one is “left out”. The remaining cases except the “left out” case are then used to train the classifier. The “left out” case fault severity is then determined using this trained classifier. Each of the training cases are used to test the classifier found with the other cases, thus the number of leave-one-out tests possible is equal to the number of observations. This results in the classifier success rate, or the number of correctly classified values using the leave-one-out method. The frequencies are chosen to optimize the classification rate by using the leave-one-out method results. This is an iterative process to determine which frequencies to use as the features. Doing this with the two-step classification method of Fig. 4.8 results in the success rate in each step using the leave-one-out method in the first row of Table (4.4).

The classifier is then re-trained with different frequencies, or features with only choosing the linear operating points from Fig. 4.2. Choosing the linear region points only was decided to be a plan to improve the classification. The equations defined in section 4.2.1 model the  $V_{CE}$  voltage in the saturation region. To this point, below the linear region, the resistance concept has little meaning. It makes more sense to choose points where the resistance is valid, since this is the main indicator of bond wire lift-off. Using only linear region points should allow for the monotonic increase or decrease in the distinguishing harmonics; a greater inter-class separation is the result of this. Doing this, even with fewer observations, the classification success rate improved 10.6% in the initial classification phase and 4.09% in the fault severity classifier. Therefore the assertion proves to be true, as choosing only the linear range points results in an improved classification percentage, something which would not be expected under traditional frequentist theory without considerations of the nonlinear mode.

Table 4.4: Success rates of the two-step fault classifier.

	C1	C2
All operating points	80.67 %	73.33 %
Linear operating points	91.25 %	77.42 %

## 4.4 Prognosis

For prognosis, once the inverter is thermally and thermal-mechanically modeled, estimating the thermal cycles with different applied currents is important to estimate the relationship between thermal cycles and time. This is done for the datasheet thermal model using actual measurements of the voltage drop over the devices with respect to current. This information allows for the simulation of the device junction temperatures.

### 4.4.1 Thermomechanical Model

In order to build the prognostic model, the reliability must be estimated. In [1] it is seen that the temperature cycling is what contributes to the bond wire lift-off failure, as this is thermally activated. This effect is due to the different coefficients of thermal expansion (CTE), which induces stress on the bond wire as in equation (4.8), where the  $\alpha$ -terms are the CTE for the respective materials,  $\Delta T_j$  is the temperature cycling range and  $\nu$  is the Poisson ratio for the device in the elastic range.

$$\epsilon_{tot} = \frac{(\alpha_{Al} - \alpha_{Si}) \Delta T_j^{-n}}{1 - \nu} \quad (4.8)$$

With uniform temperature cycling (constant amplitude), this results in the estimated number of thermal cycles to failure being  $N_f \propto \epsilon_{tot}^{-\alpha}$ , and with equation (4.8) this is  $N_f \propto \Delta T_j^{-\alpha}$ . Using the Arrhenius relationship from experimentally acquired data, the lift-off reliability in the number of cycles is given by equation (4.9).

$$N_f = A \Delta T_j^{-\alpha} \exp \frac{E_a}{k_B T_m} \quad (4.9)$$

This relationship is used to determine the number of thermal cycles to failure, where  $A=678000$ ,  $\alpha = -5$ ,  $E_a = 9.89e - 20$  and  $k_B = 1.38e - 23$ . Knowing the average number of cycles per a given time period, the failure rate can be found with equation (4.10).

$$\lambda(hour)^{-1} = \frac{\left(\frac{cycles}{hour}\right)}{N_f(cycles)} \quad (4.10)$$

#### 4.4.2 Thermal Model of Inverter

It is important to estimate the temperature accurately for use in the thermomechanical model. Using the information given in the datasheet, the thermal model can be computed with a model such as [37] for use in equation (4.9). The losses in the switches are given by the datasheet with respect to the power applied by that phase. This however fails to take into account changes in the device parameters over time. Knowing the device fault severity accurately allows for more accurate computation of the losses in the switch. These accurate losses can then be used in the thermal model from the datasheet of the inverter (SEMIKRON SKiiP 342GDL 120-4DU) given by Tables 4.5 and 4.6.

Under normal conditions, the power the device delivers to or from the load defines the loss source. This assumes nominal device resistance. In the faulted mode, the resistance increases according to the number of lifted bonds. If half of the bonds are lifted for instance, this translates to the doubling of the equivalent resistance for the same current. Thus, the losses which are used in the model will double; the effect on the thermal model is doubled. This study does just this; the four wire assumption from Fig. 4.6, and the actual resistances are not used. There are four cases, in number of bonds lifted: none (healthy), one, two, three, and all bonds. The losses are therefore: nominal power delivered to load,  $4/3$  of nominal,  $4/2$  of nominal,  $4/1$  of nominal, and 0 with all bonds lifted. Also note that each device does not conduct at all times, given that the induction machine is driven with an alternating current. Each device in a given phase conducts roughly a quarter of the time.

In order to run the thermal simulations, a thermal cycling from the ECE 15 + EUDC driving cycle from the new European driving cycle handbook [38] is used. The cycle translates to 68 thermal cycles per day; the driving cycle has currents applied 34 times, during acceleration or deceleration, and is performed twice per day. The driving cycle used results in the thermal profile as given in Fig. 4.9 under different levels of fault from the healthy to complete open fault assuming that there are four contacts. Using the calculated range of temperatures and the mean temperature once the inverter has warmed up, the mean time to failure (MTTF) in thermal cycles calculation can be made, and is shown in Table 4.7.

Table 4.5: The thermal model from the device losses for the IGBTs, diodes and module.

$R_{th(j-s)I}$	per IGBT	0.09	K/W
$R_{th(j-s)D}$	per diode	0.25	K/W
$R_{th(s-a)}$	per module	0.036	K/W

Table 4.6: The thermal model from the datasheet between the device junctions (j), the sensor (r) and the ambient (a).

$Z_{th}$	$R_i$ (mK/W) (max vals)				$\tau_i$ (s)			
Device:	1	2	3	4	1	2	3	4
$Z_{th(j-r)I}$	10	69	11	0	1	0.13	0.001	1
$Z_{th(j-r)D}$	28	193	30	0	1	0.13	0.001	1
$Z_{th(r-a)}$	1.7	24	7.6	2.6	494	165	20	0.03

In any prognostic algorithm, the calculation of reliability is vital. By improving the reliability calculation based upon the characterization of the inverter, the prognostic algorithm is improved. This is demonstrated in Fig. 4.10, which shows that if the fault severity is not determined in the bond wire lift-off case, as bonds lift off, the error in estimated MTTF is very large. This is because the thermal model used under faulted conditions varies greatly from the healthy case, because the equivalent resistance of all of the bonds will increase. Thus, when inverter characterization is used to estimate the fault severity, the improved MTTF estimation can be used to change the drive behaviour before catastrophic failure occurs. Therefore, the enhanced characterization method along with this thermal model can give a more accurate time to failure estimate.

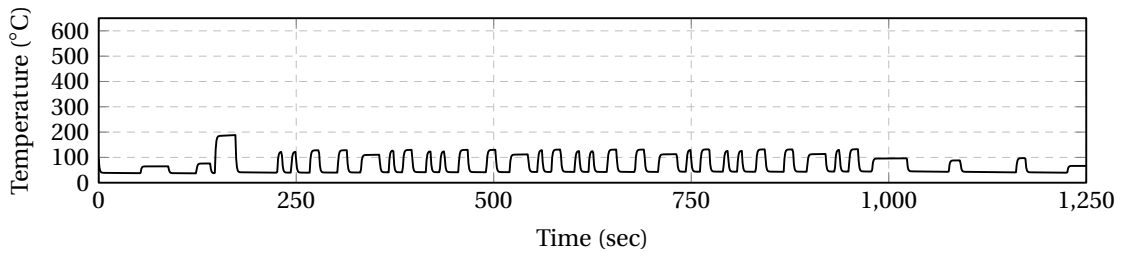
Table 4.7: Enhanced MTTF prediction assuming that there are 68 thermal cycles in a day.

Bonds Lifted	$T_m$ °C	$\Delta T_j$ °C	$N_f$	MTTF (Hours)
0	78	88.6	$750 \times 10^3$	$264.99 \times 10^3$
1	91.2	116.3	$76.4 \times 10^3$	$26.97 \times 10^3$
2	116.1	171.7	$2.3 \times 10^3$	812.91
3	190.8	338.0	2.2	0.776
4 (all)	41.33	5.43	N/A	N/A

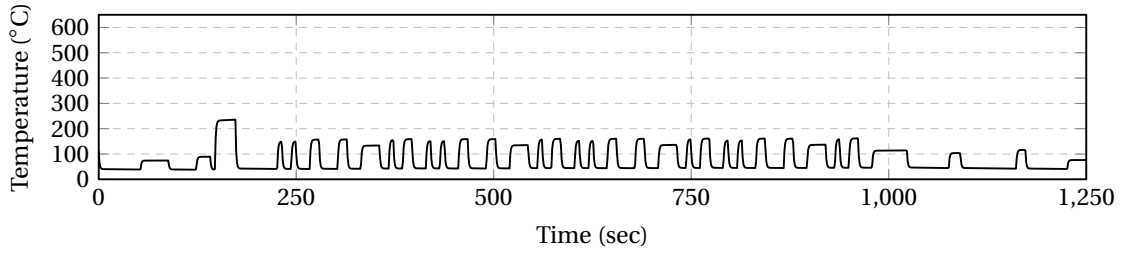


## 4.5 Conclusions

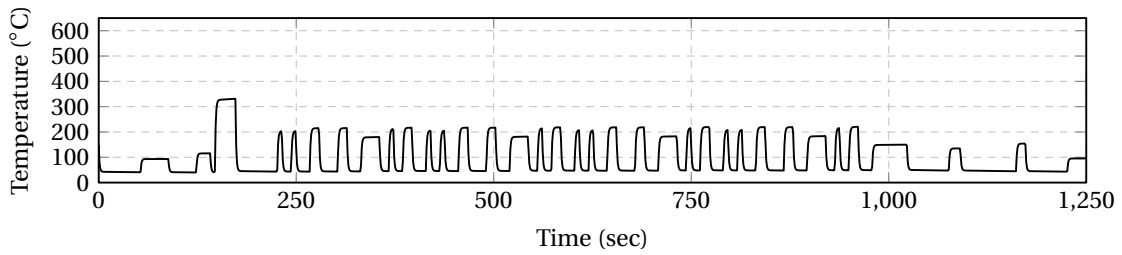
This work improves upon the presently available condition monitoring methods for inverters by utilizing knowledge of the inverter device characteristics. These device characteristics have a nonlinear current and voltage relationship, which is exploited to improve both diagnosis and prognosis of bond wire lift-off faults. The resistance is used as a measure of the number of bond wires which have lifted off. With the ability to characterize the inverter online, the inverter devices are characterized in order to determine the resistance and thus the number of lifted bonds. If only an offline characterization is available, the device characteristics are used to improve the classification using the linear discriminant classifier. Both methods prove to be effective at determining the fault level, and are an improvement upon other published works. Additionally, the mean time to failure estimation is improved upon with knowledge of the effect of bond wire lift-off upon the thermal model. The change in the thermal model under these faulted conditions has not been considered in literature. Knowing the inverter device characteristics, clear improvements are made to the detection and prediction of progression of the bond wire lift-off inverter fault.



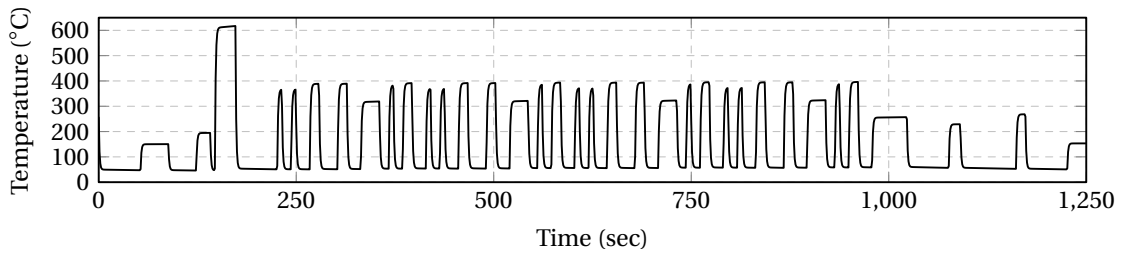
(a) Nominal case temperature profile.



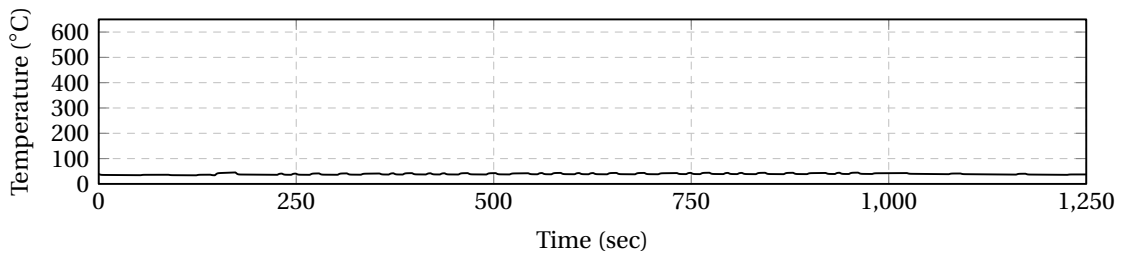
(b) One lifted bond case temperature profile.



(c) Two lifted bonds case temperature profile.



(d) Three lifted bonds case temperature profile.



(e) All lifted bonds case temperature profile.

Figure 4.9: Simulated temperature profile under the ECE 15 + EUDC driving cycle.

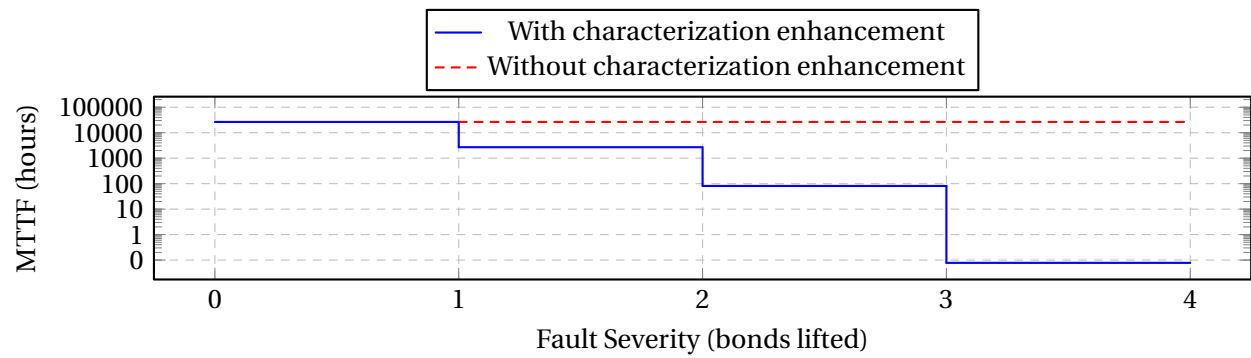


Figure 4.10: The mean time to failure estimation for prognosis improvement is demonstrated by use of the fault diagnostic method.

# Bibliography

- [1] S. Yang, D. Xiang, A. Bryant, P. Mawby, L. Ran, and P. Tavner, "Condition Monitoring for Device Reliability in Power Electronic Converters : A Review," *IEEE Transactions on Power Electronics*, vol. 25, no. 11, pp. 2734–2752, 2010.
- [2] Y. Song and B. Wang, "Survey on Reliability of Power Electronic Systems," *IEEE transactions on Power Electronics*, vol. 28, no. 1, pp. 591–604, 2013.
- [3] Y. Xiong, X. Cheng, Z. J. Shen, C. Mi, H. Wu, and V. K. Garg, "Prognostic and Warning System for Power-Electronic Modules in Electric , Hybrid Electric , and Fuel-Cell Vehicles," *IEEE Transactions on Industrial Electronics*, vol. 55, no. 6, pp. 2268–2276, 2008.
- [4] J. Holtz, J. Quan, "Sensorless vector control of induction motors at very low speed using a nonlinear inverter model and parameter identification," *IEEE Transactions on Industry Applications*, no. 4, pp. 1087–1095, Jul.
- [5] A. R. Weber, B. Rainer, and G. Steiner, "An Accurate Identification and Compensation Method for Nonlinear Inverter Characteristics for AC Motor Drives," *Signal Processing*, 2012.
- [6] K. Liu and Z. Q. Zhu, "Online Estimation of Rotor Flux Linkage and Voltage Source Inverter Nonlinearity in Permanent Magnet Synchronous Machine Drives," *IEEE transactions on Power Electronics*, no. c, pp. 1–9, 2013.
- [7] G. Pellegrino, P. Guglielmi, E. Armando, and R. I. Bojoi, "Self-Commissioning Algorithm for Inverter Nonlinearity Compensation in Sensorless Induction Motor Drives," *IEEE Transactions on Industry Applications*, vol. 46, no. 4, pp. 1416–1424, 2010.
- [8] D. E. Salt, D. Drury, D. Holliday, A. Griffo, P. Sangha, and A. Dinu, "Compensation of Inverter Nonlinear Distortion Effects for Signal-Injection-Based Sensorless Control," *IEEE Transactions on Industry Applications*, no. 5, pp. 2084–2092, Sep.
- [9] R. Raute, C. Caruana, C. S. Staines, J. Cilia, M. Sumner, , and G. M. Asher, "Analysis and Compensation of Inverter Nonlinearity Effect on a Sensorless PMSM Drive at Very Low and Zero Speed Operation," *IEEE Transactions on Industrial Electronics*, vol. 57, no. 12, pp. 4065–4074, 2010.
- [10] S.-K. Choi, Jong-Woo; Sul, "Inverter Output Voltage Synthesis Using," *IEEE Transactions on Power Electronics*, vol. 11, no. 2, 1996.

- [11] Y. Murai, T. Watanabe, and H. Iwasaki, "Waveform Distortion and Correction Circuit for PWM Inverters with Switching Lag-Times," *IEEE Transactions on Industry Applications*, no. 5, pp. 881–886, Sep.
- [12] S.-g. Jeong and M.-h. Park, "The Analysis and Compensation of Dead-Time Effects in PWM Inverters," *IEEE Transactions on Industrial Electronics*, vol. 38, no. 2, 1991.
- [13] J. G. Cintron-rivera, A. S. Babel, E. E. Montalvo-ortiz, S. N. Foster, and E. G. Strangas, "A Simplified Characterization Method Including Saturation Effects for Permanent Magnet Machines," *International Conference on Electrical Machines*, pp. 837–843, 2012.
- [14] I. R. Bojoi, E. Armando, G. Pellegrino, and S. G. Rosu, "Self-commissioning of inverter non-linear effects in AC drives," *Energy Conversion*, pp. 213–218, 2012.
- [15] G. Fedele and D. Frascino, "Spectral analysis of a class of dc ac pwm inverters by kapteyn series," *Power Electronics, IEEE Transactions on*, vol. 25, no. 4, pp. 839–849, 2010.
- [16] A. Leedy, W. Dillard, and R. Nelms, "Harmonic analysis of a two-level sinusoidal pwm inverter using the method of pulse pairs," in *Industrial Electronics Society, 2005. IECON 2005. 31st Annual Conference of IEEE, 2005*, pp. 6 pp.–.
- [17] D. Kostic, Z. Avramovic, and N. Ciric, "A new approach to theoretical analysis of harmonic content of pwm waveforms of single- and multiple-frequency modulators," *Power Electronics, IEEE Transactions on*, vol. 28, no. 10, pp. 4557–4567, 2013.
- [18] Z. Song and D. V. Sarwate, "The frequency spectrum of pulse width modulated signals," *Signal Processing*, vol. 83, no. 10, pp. 2227–2258, 2003.
- [19] W. G. Zanardelli, E. G. Strangas, and S. Aviyente, "Identification of intermittent electrical and mechanical faults in permanent-magnet ac drives based on time–frequency analysis," *Industry Applications, IEEE Transactions on*, vol. 43, no. 4, pp. 971–980, 2007.
- [20] S. Yang, A. Bryant, P. Mawby, D. Xiang, L. Ran, and P. Tavner, "An industry-based survey of reliability in power electronic converters," *Industry Applications, IEEE Transactions on*, vol. 47, no. 3, pp. 1441–1451, 2011.
- [21] D. Diallo, M. Benbouzid, D. Hamad, and X. Pierre, "Fault detection and diagnosis in an induction machine drive: A pattern recognition approach based on concordia stator mean current vector," *Energy Conversion, IEEE Transactions on*, vol. 20, no. 3, pp. 512–519, 2005.
- [22] D. Xiang, L. Ran, P. Tavner, S. Yang, A. Bryant, and P. Mawby, "Condition monitoring power module solder fatigue using inverter harmonic identification," *Power Electronics, IEEE Transactions on*, vol. 27, no. 1, pp. 235–247, 2012.
- [23] J. Estima and A. Marques Cardoso, "A new algorithm for real-time multiple open-circuit fault diagnosis in voltage-fed pwm motor drives by the reference current errors," *Industrial Electronics, IEEE Transactions on*, vol. 60, no. 8, pp. 3496–3505, 2013.

- [24] J. Lehmann, M. Netzel, R. Herzer, and S. Pawel, "Method for electrical detection of bond wire lift-off for power semiconductors," in *Power Semiconductor Devices and ICs, 2003. Proceedings. ISPSD '03. 2003 IEEE 15th International Symposium on*, 2003, pp. 333–336.
- [25] J. Morroni, A. Dolgov, M. Shirazi, R. Zane, and D. Maksimovic, "Online health monitoring in digitally controlled power converters," in *Power Electronics Specialists Conference, 2007. PESC 2007. IEEE, 2007*, pp. 112–118.
- [26] K. Smith, L. Ran, and J. Penman, "Real-time detection of intermittent misfiring in a voltage-fed pwm inverter induction-motor drive," *Industrial Electronics, IEEE Transactions on*, vol. 44, no. 4, pp. 468–476, 1997.
- [27] Q.-T. An, L.-Z. Sun, K. Zhao, and L. Sun, "Switching function model-based fast-diagnostic method of open-switch faults in inverters without sensors," *Power Electronics, IEEE Transactions on*, vol. 26, no. 1, pp. 119–126, 2011.
- [28] A. Ginart, I. Barlas, J. Dorrity, P. Kalgren, and M. Roemer, "Self-healing from a phm perspective," in *Autotestcon, 2006 IEEE, 2006*, pp. 697–703.
- [29] S. Khomfoi and L. Tolbert, "Fault diagnosis and reconfiguration for multilevel inverter drive using ai-based techniques," *Industrial Electronics, IEEE Transactions on*, vol. 54, no. 6, pp. 2954–2968, 2007.
- [30] P. Lezana, R. Aguilera, and J. Rodriguez, "Fault detection on multicell converter based on output voltage frequency analysis," *Industrial Electronics, IEEE Transactions on*, vol. 56, no. 6, pp. 2275–2283, 2009.
- [31] R. Peugeot, S. Courtine, and J.-P. Rognon, "Fault detection and isolation on a pwm inverter by knowledge-based model," *Industry Applications, IEEE Transactions on*, vol. 34, no. 6, pp. 1318–1326, 1998.
- [32] C. Turpin, P. Baudesson, F. Richardeau, F. Forest, and T. Meynard, "Fault management of multicell converters," *Industrial Electronics, IEEE Transactions on*, vol. 49, no. 5, pp. 988–997, 2002.
- [33] F. Richardeau, P. Baudesson, and T. Meynard, "Failures-tolerance and remedial strategies of a pwm multicell inverter," *Power Electronics, IEEE Transactions on*, vol. 17, no. 6, pp. 905–912, 2002.
- [34] D. Mingxing, W. Kexin, L. Jian, and X. Linlin, "Condition monitoring igbt module bond wire lift-off using measurable signals," in *Power Electronics and Motion Control Conference (IPEMC), 2012 7th International*, vol. 2, 2012, pp. 1492–1496.
- [35] P. Paris and F. Erdogan, "A critical analysis of crack propagation laws," *Journal of Basic Engineering*, vol. 85, p. 528, 1963.
- [36] R. Sundararajan, P. McCluskey, and S. Azarm, "Semi analytic model for thermal fatigue failure of die attach in power electronic building blocks," in *High Temperature Electronics Conference, 1998. HITEC. 1998 Fourth International*, 1998, pp. 94–102.

- [37] J. Lutz, *Halbleiter-Leistungsbaulemente*, ser. SpringerLink:Bücher. Springer Vieweg, 2012. [Online]. Available: <http://books.google.at/books?id=g9Ze6Kmh3YUC>
- [38] T. J. Barlow, S. Latham, I. S. McCrae, and P. G. Boulter, "A reference book of driving cycles for use in the measurement of road vehicle emissions," United Kingdom Transport Research Laboratory, Tech. Rep., 2009.