UNIVERSITY
OF APPLIED SCIENCES
UPPER AUSTRIA

Master's degree programme

Automation Engineering

Power Electronic Converter Common-Mode Interference Measurement and Modeling

submitted as a Master Thesis

to obtain the academic degree of

Master of Science in Engineering (MSc)

by

Jürgen Hotz

August 2017

Thesis supervisor

Dipl.-Ing. Dr. Roland Exler

Acknowledgment

The Center for Advanced Power System is a state of the art research institute of the Florida State University. The facility is a multidisciplinary research center organized to perform basic and applied research to advance the field of electric power systems technology and enjoys an excellent reputation.

I had the privilege to work at the Center for Advanced Power Systems for five months. During my stay, I have learned a lot with many challenging experiences throughout the project. This would not have been possible without the help of many people. Therefore, I would like to use this section of my thesis to mention those who helped and supported me with their knowledge and guidance.

First of all I would like to thank Dr. Michael "Mischa" Steurer who gave me the opportunity to be a part of the Power Systems Group. Without him I would not have had the possibility of working on this project and to gain experience in the field of power electronics in an international facility. Furthermore, I would like to thank my supervisor Matthew Bosworth who supported me with his knowledge and experience in this field from the start of the project until its end. Because of his dedication and guidance the work had always a clear direction. I also want to thank Karl Schoder who also supported me with advice and assistance at any time.

I also want to point out my gratitude to my supervisor in Austria, Dr. Roland Exler from the University of Applied Sciences Upper Austria who guided me through the whole project.

A special thanks also goes to the Marshall Plan Foundation, who covered a big part of the financial load of the whole stay.

Finally, I would like to thank my family for their active support during my studies., especially my parents Alexandra and Michael Hotz as well as my sister Corinna. They always kept me motivated and without them it would have been much harder to follow my track.

This work was partially funded by the US Office of Naval Research under Grant N00014-15-1-2250.

Sworn declaration

I hereby declare that I prepared this work independently and without help from third parties, that I did not use sources other than the ones referenced and that I have indicated passages taken from those sources.

This thesis was not previously submitted in identical or similar form to any other examination board, nor was it published.

.....

Jürgen Hotz

Wels, August 2017

Abstract

The research presented in this master thesis was performed at the Center of Advanced Power Systems, a leading electrical power research institute of the Florida State University in 2017. The topic of the research is the modeling and simulation of the common-mode characteristics of a silicon carbide metal-oxide-semiconductor field-effect transistor (SiC MOSFET) H-bridge and the verification of the outcome by taking measurements of the physical switching device by the use of a vector network analyzer.

The main focus of the project lies within the correct replication of the common-mode behavior of the device under test, so the simulation model represents the SiC MOSFET H-bridge and its common-mode behavior. Subsequently, it can be used to present the device in a larger system context, which would lead to a prediction of its effect onto other system components.

In chapter one, a short introduction of the motivation behind this research and an overview of previous performed and related works are given. Furthermore, existing standards related to electromagnetic compatibility are listed. A short introduction of electromagnetic interference and its sources is given in chapter two. In the following section, different modeling approaches of a power electronic building block of the Virginia Tech impedance measurement unit is described, while Chapter 4 presents the measurements of the power electronic device, which contains the SiC MOSFET H-bridge. All measurement results and an introduction of scattering parameters can be found in the appendix of the thesis.

Proper modeling of power electronic device common-mode characteristics is an important step within the design and development of a power system. Since the switching frequency and power density of these devices are constantly rising, modeling the common-mode characteristics of switching components in power electronic circuits is of increased importance. The reason is the root cause of electromagnetic interference, which is a fast rate of change in voltage and current. These rates of changes stimulate oscillations producing current in undesired conductive paths. First, a differential-mode model is presented. This model gets expanded by adding all expected parasitic capacitances to ground, which provides a path for the common-mode currents. After the performance of the mixed-mode model gives a reasonable output a common-mode equivalent circuit is designed, which is then

verified by comparison with the simulation and the performed measurements.

In the last chapter, the conclusions finalize the thesis by presenting the correlation between the created models and the executed measurements. Scattering parameters

Contents

1 Introduction

1.1 Motivation and Background

The Electric Ship Research and Development Consortium (ESRDC) grounding group has been working on developing new approaches for modeling common-mode characteristics of power system components expected to be seen on board of a mega-watt (MW) scale all-electric ship. A motivation for being concerned about common-mode at any stage of ship design is that the adoption of a new enabling power system has the risk of increased electromagnetic interference (EMI). An example of such a power system is one based on power electronic converters.

Leakage current (common-mode current) through bearings and the ship hull can lead to unintended operations of components. This current results in a field that can be coupled to other systems, such as sensors and communication equipment, which consequently can result in disturbances of their signals. Therefore, mitigation is needed. In order to understand common-mode (CM) behavior and achieve mitigation the characterization and measurement of the wide-bandwidth frequency behavior of the systems, including switching-induced electromagnetic fields and the behavior of the system in response to faults is essential for ship designers.

Currently, no standards or guidelines exist for shipboard power systems that describe interface requirements for CM coupling at a system context. The Center of Advanced Power Systems (CAPS), Florida State University, is working towards models validated by experimental results, which can help establishing such interface guidelines in the future. It is known that power electronic switching frequencies are the main source of common-mode interference, due to the high rate of change in voltage and current caused by switching events. Therefore, the following research questions have to be considered. How does one model interference within a power system simulation? Furthermore, how can salient features of CM interactions between components be identified?

To answer these questions, the salient common-mode characteristics of one power electronic building block (PEBB) of the Virginia Tech (VT) impedance measurement unit (IMU) will be determined via computer modeling and simulation using MATLAB®/Simulink and the

additional simulation software package for power electronics PLECS® Blockset as well as PLECS® Standalone. The validation of the model is achieved by taking measurements of the CM current and voltage of the PEBB in an energized and a de-energized state. Moreover, the use of the model in a system level simulation can be verified.

This thesis will gather knowledge about CM interference and its salient characteristics, as well as demonstrate the possibility of modeling the interference caused by power electronic switching events. Furthermore, this work will deliver a CM model of a PEBB, which reproduces its CM behavior over a broad frequency range.

1.2 Literature Review

As a consequence of growing costs and military capabilities the U.S. Navy started to reconsider the design concept of traditional naval ship power distribution systems in the last few years. Therefore, the approach of an all-electric ship (AES) was created as part of an ambitious technology plan for the Navy fleet of the future. The Office of Naval Research (ONR) Electrical Ship Research Development Consortium (ESRDC) is exploring ways to power this kind of ship [1,2]. The concept behind the AES is an integrated power system, i.e. a common power distribution system which allows nearly all shipboard power systems to be driven directly by electric power. This includes propulsion, radar, communication as well as weaponry. The goal of this power distribution is to enable the powering of the ship's loads and the propulsion system from the same electric source, thus avoiding a separate generation system [3], thus a further milestone to achieve a higher efficiency with the use of the on-board power while reducing fuel use and crew size [4]. An example of this new supplying concept is the USS Zumwalt, the first surface combatant with integrated power systems (IPS) that supplies electric power for both propulsion and ship service loads, launched on 29 October 2013 [5,6]. With this IPS, the interest in medium voltage direct current (MVDC) power systems increased for the use in future naval surface vessels. This new energy distribution created new concerns with electromagnetic interference (EMI), especially with leakage currents through the ground plane (i.e. the ship hull), CM currents, as well as voltage stress resulting from high-edge-rate switching. This kind of CM behavior in power systems is related to bearing [7] and insulation failure [8].

The CM phenomena and the effect of parasitic components are observed and analyzed in numerous different works [9–12]. Because of this phenomena and its unwanted effect on a power electronic system, techniques to contain, reduce and mitigate EMI noise increased within the topic of power electronic circuits. These techniques can be associated with different classes. The first group contains filtering techniques, which includes CM-chokes, shielding techniques and filters as proposed in [13–15]. The second class is about cancellation of EMI sources, by the identification of CM voltage sources and driving them

to zero. Hence, the CM-current also is reduced to zero. This can be obtained with cancellation techniques as presented in [16–18], novel circuit designs [19–22] and switching techniques [23–25]. The third group includes techniques to disturb the CM current path, e.g. with different grounding techniques such as grounding of the negative rail or midpoint grounding. The effects were investigated in [2, 26–29]. The last kind of CM mitigation technique involves balancing techniques of a circuit as proposed in [30, 31].

All of these methods involve system penalties. Since CM mitigation also affects the system performance, and the costs can increase due to additional needed components. Because of that reason, it is preferred to reduce CM-voltage (CM-current) just as far as needed to ensure safety and comply with emission standards. To apply any of the mentioned solutions to reduce the CM currents, first one has to understand the noise source and CM current path, i.e. parasitic coupling to ground. One of the main sources of common-mode noise is power electronic switching devices [32]. Because of new technologies, such as Silicone Carbide (SiC) IGBTs and SiC MOSFETS, they have the capability of higher switching frequencies leading to a reduction in size of external components, such as inductors and capacitors. Consequently, the costs are reduced [33]. Nevertheless, a higher switching frequency also has drawbacks. The switching losses rise proportional to the switching frequency and furthermore, it causes higher CM noise, due to the increasing rate of change of voltage over time ($^{dv}/_{dt}$) [34].

From the analytical perspective, modeling showed to support CM design and mitigation. Two different modeling concepts have received the most attention. The first technique is to derive a mixed-mode model, which is created by adding parasitic elements to the differential circuit model. This approach yields a coupled DM/CM behavior [35–40], a mixed-mode model. This concept is shown to be an effective way for single converter or drives, but the computational costs are prohibitive for more complex systems, such as modern ship electrical systems. This is where the second approach becomes preferable. This technique is to derive the CM equivalent circuit for the purpose of analyzing CM voltage and current in large complex power systems. As shown in [7, 14, 18, 21, 41–51], the impact of power electronic switching is represented by CM voltage or current sources, coupled to the parameterized domain, parasitic paths. The computational effort to simulate such equivalent circuits is highly reduced in comparison to the mixed-mode model, due to the number of components and the complexity reduction of the simulation model. Furthermore, the need to identify switching instants throughout a simulation is eliminated. The final advantage of a CM equivalent model is the use of techniques for linear circuit analysis (e.g. Thevenin's theorem), which can be considered hassle-free to apply for a prediction of the CM behavior.

Derivation of CM equivalent circuits is proposed in [41] for a DC-based ship power system.

It defines the CM voltage with respect to an arbitrary reference point, which leads to a straightforward transformation of the mixed-mode model into its CM equivalent as the authors outlined first in [52]. Therefore, [41] will serve as an example for the basic derivation procedure for this thesis, but the focus will lie on modeling the parasitic impact of the included inverter of the device under test (DUT), since the influence of the parasitic coupling to ground of the power electronic switching device over its heat sink is of interest. The impact on the system of the conducted EMI caused by heat sink parasitics are studied and analyzed in [34, 53, 54].

1.3 Standards

Various government bodies defined several standards correlated to the protection of a product against susceptibility to other products emissions. Instituted standards specify limits for the quantities of radiated and conducted noise emission. Compliance is needed in order to sell a product within a country. In Europe these standards are set by the European Economic Consortium (EEC), while the responsible bodies in the United States are the Federal Communications Commission (FCC) and the Department of Defense (DoD). Furthermore there is the International Special Committee on Radio Interference (CISPR), an international body of the International Electrotechnical Commission (IEC), which provides methods and guidance on how to generate appropriate limits for the protection of radio reception, but do not contain any prescribed limits or system related performance specifications. It has to be mentioned that CISPR has no regulatory authority, but its standards can be used as benchmark or goal for suppliers which can be adopted by individual nations in order to achieve facilitation for international trade. In Table 1.1 numerous common standards for EMI regulations are listed [55].

All of these standards include both, conducted and radiated specifications as well as regulations regarding electromagnetic compatibility. The most important difference between the single specifications is the frequency bandwidth which they cover. According to [56] and [57], for purposes of the FCC's exposure guidelines, the frequency range of interest is between 300 kHz and 100 GHz. The most important limits for this thesis occur in the frequency range of 450 kHz to 30 MHz. Conducted emissions have to be controlled in this domain in the FCC standards. While the CISPR as well as the IEC regulations exhibits the same end frequency of 30 MHz, both specify the start of the conducted emission frequency bandwidth at 150 kHz [58].

Standard	Description
EN 50065-1	Signalling on low voltage electrical installations in the frequency range 3 kHz to 148,5 kHz - Part 1: General requirements, frequency bands and electromagnetic disturbances
EN 55011 \ CISPR 11	Industrial, scientific and medical (ISM) radio-frequency equipment – Electromagnetic disturbance characteristics – Limits and methods of measurement.
EN 55013	Sound and television broadcast receivers and associated equipment - Radio disturbance characteristics - Limits and methods of measurement
EN 55014	Electromagnetic compatibility - Requirements for household appliances, electric tools and similar apparatus
EN 55015	Limits and methods of measurement of radio disturbance characteristics of electrical lighting and similar equipment
EN 55022:2010 \ CISPR 22	Information technology equipment - Radio sisturbance characteristics - Limits and methods of measurement
IEC 61000-3-2	Electromagnetic compatibility (EMC) - Part 3-2: Limits - Limits for harmonic current emissions (equipment input current $\leq$ 16 A per phase)
IEC 61000-3-3	Electromagnetic compatibility (EMC) – Part 3-3: Limits – Limitation of voltage changes, voltage fluctuations and flicker in public low voltage supply systems, for equipment with rated current $\leq$ 16 A per phase and not subject to conditional connection
IEC 61000-3-11	Electromagnetic compatibility (EMC) - Part 3-11: Limits - Limitation of voltage changes, voltage fluctuations and flicker in public low voltage supply systems - Equipment with rated current $\leq$ 75 A and subject to conditional connection
IEC 61000-3-12	Electromagnetic compatibility (EMC) - Part 3-12: Limits - Limits for harmonic currents produced by equipment connected to public low voltage systems with input current $>$ 16 A and $\leq$ 75 A per phase
IEC 61000-4-3	Electromagnetic compatibility (EMC) - Part 4-3: Testing and measurement techniques - Radiated, radio-frequency, electromagnetic field immunity test
FCC Part 15	Radio Frequency Devices
FCC Part 18	Industrial, scientific and medical equipment
MIL-STD-461G	Department of Defense Interface Standard – Requirements for the Control of Electromagnetic Interference Characteristics of Subsystems and Equipment

Table 1.1: List of common electromagnetic interference regulations

2 Common-Mode Interference

To provide a basis for deriving of a common-mode equivalent circuit, a short review of common-mode interference and the methodology is provided [41, 52].

2.1 Review and Definition

First of all, one has to define electromagnetic interference (EMI), definitions and sources in order to understand common-mode interference. EMI is a phenomenon where one electromagnetic field interferes with another, resulting in a distortion of both fields. This distortion is an unwanted effect of electromagnetic noise which interferes with other signals of interest and can yield in an unexpected systems behavior. In other words, it is any unwanted electric or electronic disturbance, which causes an undesirable response, thus creating a malfunction or degradation in the performance of electrical or electronic equipment. Generally speaking, the effect of EMI is detrimental and just about any electrical or electronic device has the potential to generate EMI.

EMI can be distinguished in two types of interference, radiated and conducted. Conducted emissions are electromagnetic emissions propagated along a power or signal conductor, while radiated emission is the electromagnetic energy propagated through space. Moreover, conducted electromagnetic interference can be broken down into two modes of circuit operation: differential-mode (DM) and common-mode (CM). The differential-mode is the desired operation of the circuit, while the common-mode, also called asymmetrical interference, is an undesired operation of a system. CM is often a result of interference, imbalances in the switching circuitry, transmission path or load, asymmetrical design or parasitic coupling. Parasitic coupling will play a major part in this thesis. As a result, noise appears in all phases with equal amplitudes. The definition of CM voltage v_{cm} and CM current i_{cm} as well as DM voltage v_{dm} and DM current i_{dm} is shown in Fig. 2.1.

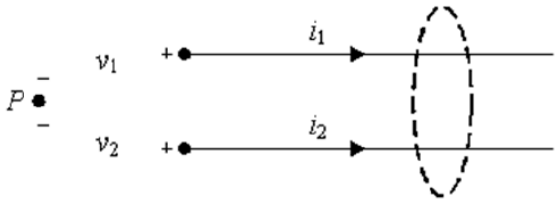


Fig. 2.1: Differential and Common-Mode Definition [41]

As described in previous works, the DM and CM currents are defined for the set of wires by:

$$i_{dm} = \frac{1}{2}(i_1 - i_2) \tag{2.1}$$

$$i_{cm} = i_1 + i_2 \tag{2.2}$$

According to this definition, the CM current is zero, if a current I is flowing through line one and returning on line two ($i_1 = -i_2$), while the DM current results in I in this case. In the same way the DM and CM voltages are defined herein with respect to an arbitrary point P by:

$$v_{dm} = v_{1P} - v_{2P} \tag{2.3}$$

$$v_{cm} = \frac{1}{2}(v_{1P} + v_{2P}) \tag{2.4}$$

If both voltages v_{1P} and v_{2P} are balanced with respect to the chosen point P, the CM voltage between the two wires is zero while the DM voltage is simply the difference between v_{1p} and v_{2p}. Equation 2.4 also shows that the voltage with respect to ground is not the same as the CM voltage, since the reference point P can be chosen arbitrarily. Further generalizing this definition of CM current and voltage, [52] and [41] propose the following formula for the CM quantities for a number of K lines,

$$i_{cm} = \sum_{k=1}^{K}(i_k) \tag{2.5}$$

$$v_{cm} = \frac{1}{K}\sum_{k=1}^{K}(v_{kP}) \quad \text{with} \quad k \in 1 \dots K \tag{2.6}$$

where the CM voltage is defined with respect to a fully arbitrary point P. In this way a piecewise construction of a CM equivalent model for arbitrary large power systems is possible. The defined CM voltage represents the average voltage looking into or out of a set of electrical ports [41, 52].

Power inverters convert electrical power of one voltage or frequency to another power of different voltage or frequency. Most inverters employ pulse-width modulation (PWM)

schemes that rely on frequently switching signals with very fast rise and fall times, especially with SiC based switching devices. These signals have significant energy at frequencies far beyond the fundamental switching frequency. Imbalances in the switching circuitry, transmission path or load drive a portion of the power from the DM currents through CM current pathways, which can interfere with other electric or electronic devices. The higher the switching frequency the higher the influence, due to the increasing rate of change of voltage over time $\left(\frac{\mathrm{d}v}{\mathrm{d}t}\right)$.

2.2 Sources of Electromagnetic Interference

With increasing density of the electromagnetic environment, the concern about the effects of EMI producing sources is of importance. Since the interference has an impact on the system performance, one has to consider possible EMI sources within the circuit of interest and occurring parasitics of the device under test. Under the term parasitics one understands unavoidable and unwanted parasitic elements such as capacitances and inductances, which occur between the components of the circuit or between a component and its environment. The main focus lies in the identification of parasitic capacitances, since these elements provide a path for the CM current.

2.2.1 Passive Components

Passive components such as resistors, capacitors, inductors and transformers as well as connection cables with considerable length need to be seen as source of interference, especially with increasing frequency. While these components behave as expected in the lower frequency domain, their performance changes with rising frequency, due to parasitic capacitances and inductances. Therefore, passive components can influence EMI.

2.2.2 Active Components

Active components are one of the sources of noise in a system, due to inherent parasitics in the device packaging. In the case of the PEBB the parasitic coupling to ground of each SiC MOSFET over its heat sink has to be taken into consideration. The occurring CM voltage waveform interacts with the parasitic capacitance between the MOSFET and heat sink. Hence, it provides a pathway for CM current to ground and it serves as a source of CM noise. If the heat sink is floating, the noise will be reduced, but in power electronic applications this parasitic coupling cannot be fully eliminated. This thesis will focus on the identification and influence of these parasitics.

Besides the parasitic capacitances, the switching devices will also exhibit parasitic inductances from the package leads, which causes high frequency ringing in the voltage waveform

across the MOSFET. These effects serves in turn as DM noise current source due to the interaction between the Miller capacitance (gate-to-drain capacitance) of the switching device and the high frequency voltage component [59,60]. These parasitic impedances and other additional parasitic effects such as the diode reverse recovery are out of scope of this research and will not be discussed.

3 Modeling

As a first step, a DM model is created of the electric circuit of the PEBB shown in Fig. 3.1. In order to simulate the coupled DM/CM circuit, parasitics of the device are considered and added to the model. This approach causes issues. The most important problem is the rising number of components, which are necessary to set up the mixed-mode (MM) simulation model. This results in a numerical expenditure, since the system of interest becomes more complex and the computation time rises significantly. In order to predict the CM interference caused by the device, a CM equivalent circuit is modeled. This modeling approach reduces the needed components of the circuit of interest. The decreasing number of components also reduce the computational burden.

By using the definitions of CM voltage and current shown in Chapter 2, the authors in [52] and [41] propose a formalized process to create a common-mode equivalent circuit from the DM model. The procedure is described below:

1. Add parasitic capacitances to the DM component model
2. Transform the DM components into a CM equivalent circuit by using the definitions of CM voltage and current
3. Characterize the CM voltage source(s)
4. Build the CM system model and
5. Perform circuit analysis by using standard circuit analysis (time or frequency domain)

These steps are governed by two essential assumptions. First, the circuit or system of interest must be symmetrical with relation to a common potential, e.g. ground. In other words, all terminals of the DUT must have the same impedance. If the system of interest does not fulfill this assumption and presents unequal impedance at its terminals, CM/DM coupling will occur and the definitions in Fig. 2.1 become invalid. This includes line-ground fault scenarios, unbalanced AC phase operation, etc.

The second assumption is a negligible CM/DM coupling. In real systems, common- and differential-modes exist simultaneously and result in an inherent coupling between both modes (i.e. an intrinsic mixed-mode operation). In order to separate and understand the CM impact throughout the system, the coupling between the two modes needs to be negligible. This assumption may not be valid for all possible operation conditions. Literature

in the field of EMI and radio frequency applications provide insight into simulation and measurement approaches of the mixed-mode (MM) operation [61–66]. Furthermore, the parasitic capacitances of the MOSFETs are dependent on its voltage, which would cause them to change while switching the semiconductors on or off. It is assumed, that this change is negligible in comparison with the parasitic capacitances presented by the rest of the system.

In order to keep the system of interest symmetric, it was decided to use a DC voltage source to power the device and to use the PEBB as DC/AC converter with a pure resistive load. Details of the hardware and the operation mode are described in Chapter 4.

3.1 Differential-Mode Model

A differential-mode model of the IMU PEBB was built in MATLAB®/Simulink with the additional simulation software package for power electronics, PLECS®. An existing model was used as base, which was provided by the Center for Power Electronics (CPES) at Virginia Tech (VT).

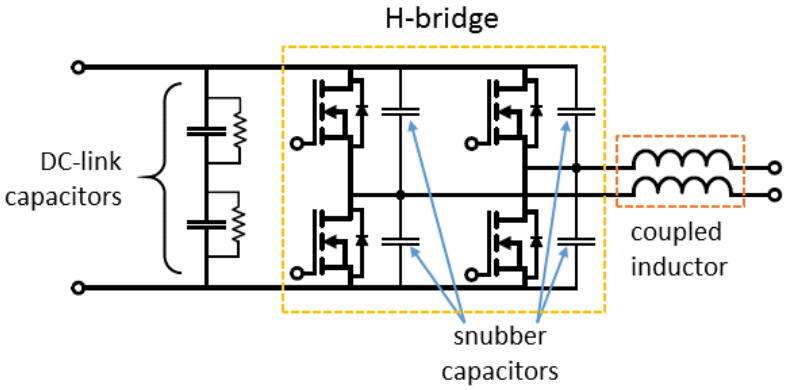


Fig. 3.1: Simplified circuit schematic of the PEBB

Fig. 3.1 shows a simplified version of the modeled circuit. The previously built model used the PEBB as AC/DC converter and comprised a modulation index calculation, which used a current and voltage control loop to readjust the index in order to stabilize the output. This calculation was removed and replaced by a fixed modulation index signal, since both the current and voltage control were disconnected and not used in the performed measurements. The reason lies within the fact that the focus is on common mode quantities. Therefore, there is no need for an optimized output and a sine-wave with 60 Hz and a modulation magnitude of 0.9 was applied directly to the input of the sinusoidal pulse width modulation (SPWM) was used. The value of the amplitude was chosen in a way, to avoid

over-modulation and the PWM used a dead time of 2.5 μs. Furthermore, the provided model used a triangular carrier signal with 10 kHz and 50% duty cycle as carrier signal, which was maintained in the new model. The resulting pulse generator control diagram is shown in Fig. 3.2.

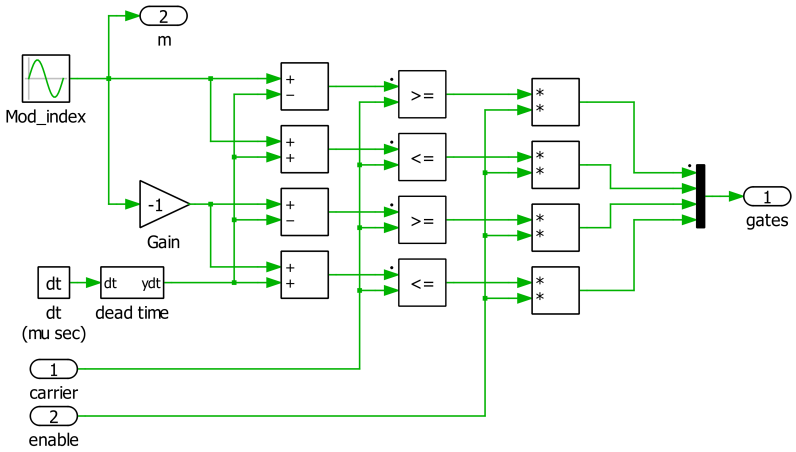


Fig. 3.2: Sinusoidal pulse width modulation

The dead time calculation is included, which is computed over the rise time of the carrier signal,

$$\Delta y = \frac{y}{t_y} \cdot \Delta t \tag{3.1}$$

where Δy represents the required shift of the modulation index, in order to achieve a dead time of Δt. The amplitude of the carrier is described by y and its rise time by t_y. Since these calculated delay is applied to all four switching signals, Δy has to be halved to achieve the wanted dead time. It should be mentioned that there is also a preexisting PLECS block, which can be used to achieve a dead time, but when it was used instead of the calculation, it caused an error at the start of the simulation and therefore, was not used. The modeling of the DM equivalent circuit of the PEBB and its MOSFET H-bridge was a straight forward process, by rebuilding the system in MATLAB®/Simulink/PLECS Blockset. The simulation model circuit is shown in Fig. 3.3.

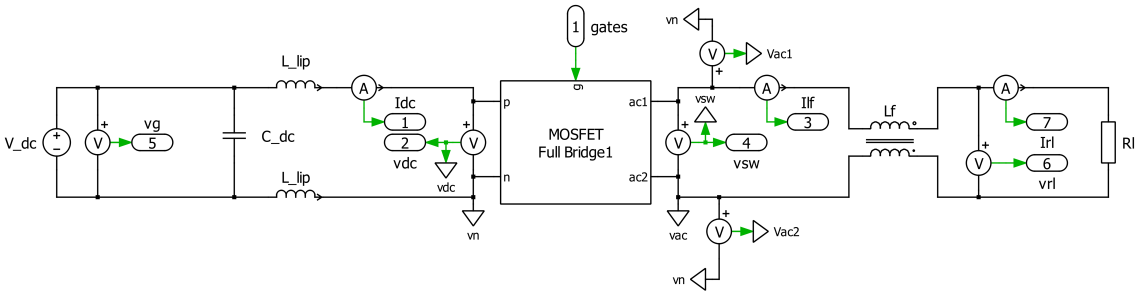


Fig. 3.3: DM model of the PEBB

The model provided by CPES did not include the snubber capacitors in parallel to each MOSFET. These were added to the model in PLECS in order to represent the power electronic switching devices behavior as accurate as possible. The circuit of the H-bridge can be seen in Fig. 3.4.

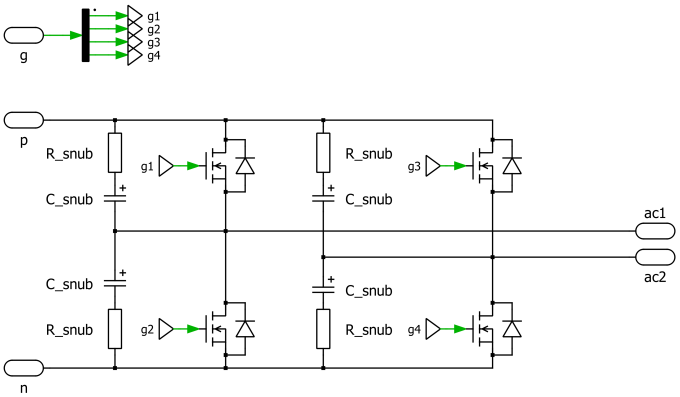


Fig. 3.4: DM model of the H-bridge

The values of all components included in the simulation model are listed in Table 3.1. It should be noted that the DC-link capacitor includes its parasitic serial inductance and resistance. This is to recreate the real frequency behavior of the component within the simulation and details are given in Section 3.4.2. The effect of the DC-link capacitor on the system is expected to be rather low, since the simulation is performed with an ideal power source.

The parameters for the non-ideal MOSFETs were estimated as data sheets were not available. The blocking voltage is the rated voltage of the device. For a first assessment of the continuous drain current, rise time and fall time, the requirements for SiC switching devices used in a dual half-bridge power MOSFET module mentioned in [67] were used. It was decided to use the maximum rise time of 100 ns, due to snubber capacitors effect. The fall time was set to 80 ns, since it is common for MOSFETs to show a lower fall than rise time as described in [68]. The on-resistance from the original CPES model of $30m\Omega$ is used. The off-resistance was set to 1 MΩ. The stray inductance of the device was set to a value of 1 μH, based on simulation assessment. A 1 Ω resistor was added into the snubber capacitor path to damp unreasonably large ripples observed within the H-bridge output when no resistor is present. In the real circuit, other damping mechanism must be present as no such large ripples were observed by measurements.

The tolerance of the snubber capacitors is $\pm 10\%$. This was neglected in the simulation, but this possible deviation from the nominal value can cause a disruption of the systems symmetry. A measurement of each snubber capacitor was not possible, since they

Sys. comp.	Description		Symbol	Value
Source side	DC voltage source		V_{dc}	max. 160 V
	DC-link capacitor	Capacitance	C_{dc}	635 μF
		Parasitic resistance	R_p	8.3 mΩ
		Parasitic inductance	L_p	1.6 μH
	Low inductive plate		L_{lip}	100 nH
Inverter	SiC MOSFET	Blocking voltage	V_{ds}	10 kV
		Continuous drain current	I_d	100 A
		Rise time	t_r	100 ns
		Fall time	t_f	80 ns
		Stray inductance	L_{sig}	1 μH
		On-resistance	R_{on}	30 mΩ
		Off-resistance	R_{off}	1 MΩ
	Free wheeling diode	Diode voltage	V_d	2 V
		On-resistance	R_d	30 mΩ
	Snubber capacitor	Capacitance	C_{snub}	700 nF
		Resistance	R_{snub}	1 Ω
Load side	Coupled inductor	Inductance per coil	L_f	440 μH
		Mutual inductance	L_m	330 μH
		Resistance	R_d	150 mΩ
	Load resistor		R_l	100 Ω

Table 3.1: Values of components included in the DM model simulation

were connected directly between the low inductive plate and the inverter, which is why a disconnection of the system was not possible.

3.2 Mixed-Mode Model

The DM model represents the PEBB and its supposed behavior, but it does not properly represent the real system. To correctly model the physical aspects the occurring parasitics must be added. In this manner a model is created, which includes both, the differential- and common-mode behavior of the system. To accomplish a correct expansion of the DM model to MM model, knowledge of possible sources of parasitic coupling needs to be defined.

3.2.1 Parasitic Capacitances

Previously performed measurements and analysis of PEBB components are presented in [69]. These measurements were performed in 2015. In the report the capacitive parasitic coupling to ground of the DC-link capacitors, the IGBT-module[1] and the coupled inductor are estimated by using a method with least square error (LSE) and multiple measurement setups of each component. Therefore, the document gives a first look into the expected parasitic capacitances to ground, which will have an impact on the CM behavior of the PEBB. To verify or correct the outcome all measurements were repeated with the same configuration.

3.2.1.1 DC-link Capacitor

To determine the parasitics of one disconnected and de-energized pair of the DC-link capacitors, three different measurement locations, all in respect to ground were chosen: positive rail, negative rail, and midpoint connection point. This is shown in Fig. 3.5a.

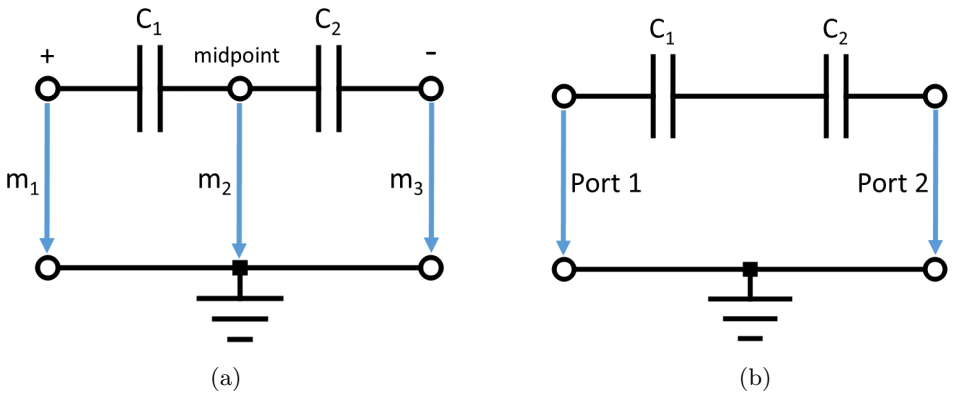
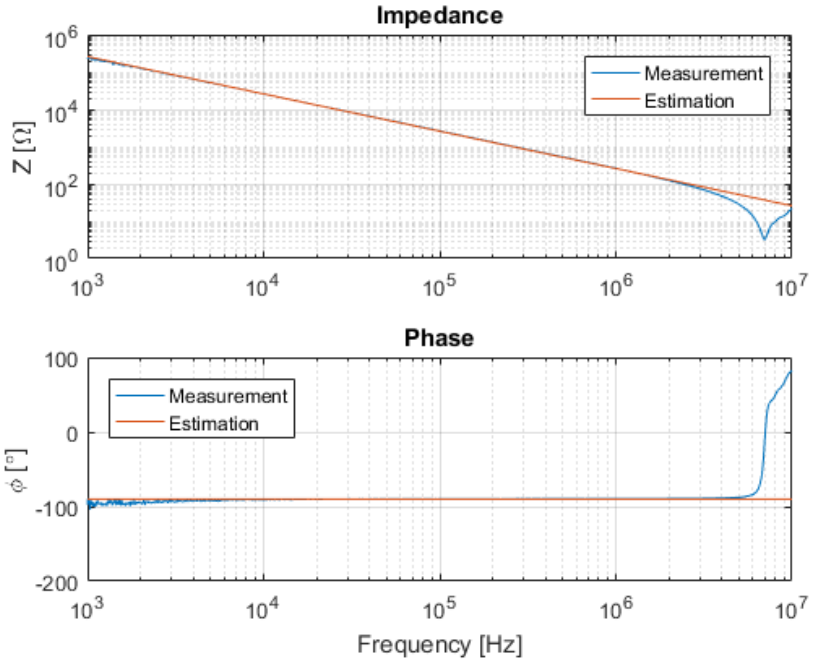


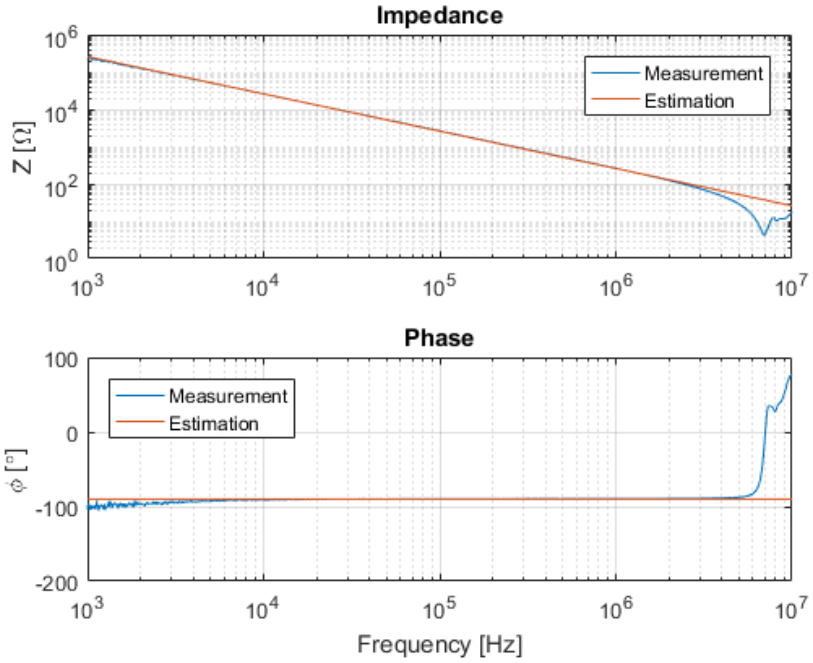
Fig. 3.5: Various performed measurements of one pair of the DC-link capacitors to estimate the parasitic capacitance to ground: (a) Measurement of three different points against ground, (b) S-parameter measurement of the DC-link capacitors

The described measurements as depicted in Fig. 3.5a were repeated in order to verify the values of the parasitic capacitances. The outcome of both measurement configurations and an estimation of the caused parasitic capacitances to ground are shown in Fig. 3.6 and Fig. 3.7.

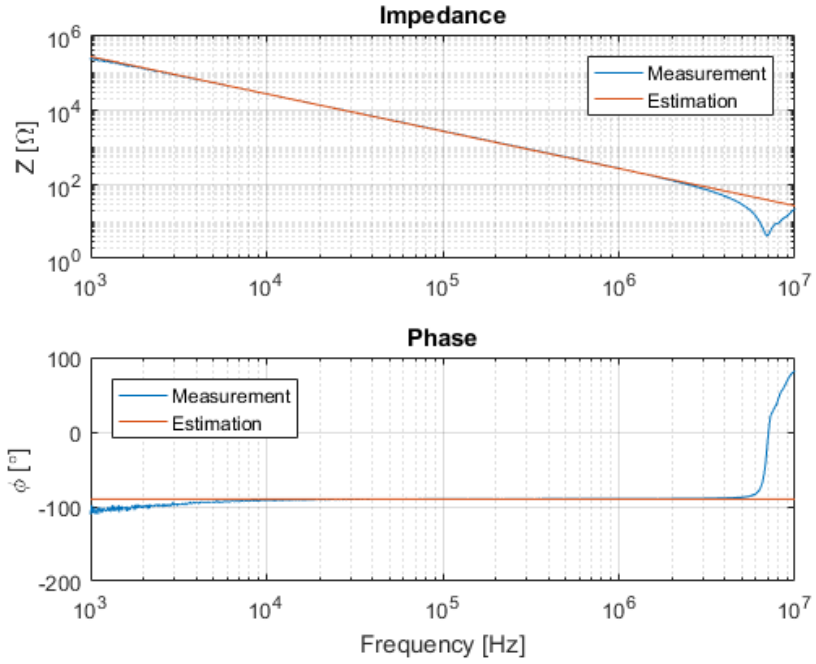
[1]The IGBT-module was removed for the performed tests. Therefore, its parasitics are irrelevant and are not discussed herein.



(a) Positive rail to ground



(b) Midpoint to ground



(c) Negative rail to ground

Fig. 3.6: Measurement of the DC-link capacitor performed in configuration as shown in Fig. 3.5a and comparison with an estimation of the parasitic capacitance to ground caused by the DC-link capacitor: (a) Measurement point m_1: positive rail to ground, (b) Measurement point m_2: midpoint to ground, (c) Measurement point m_3: negative rail to ground

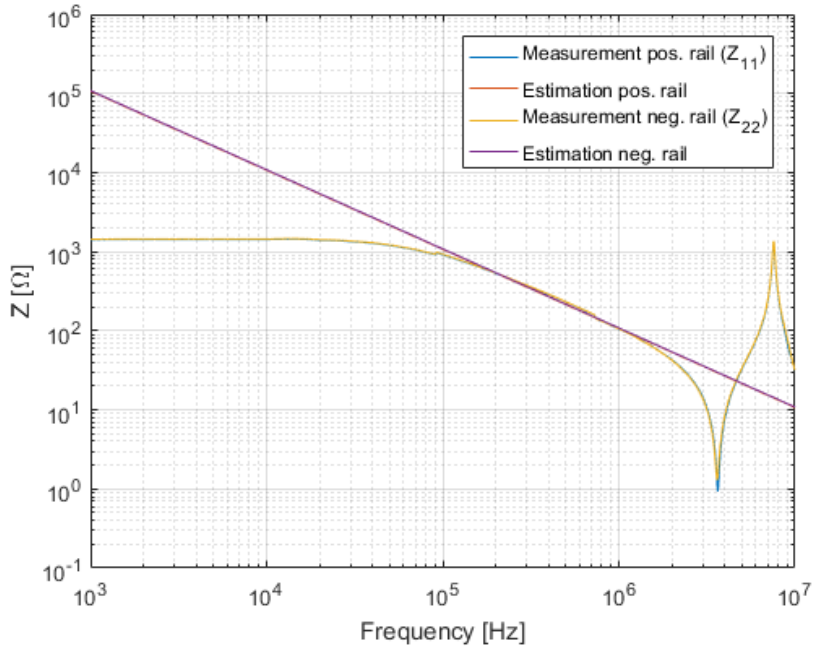


Fig. 3.7: Two-port S-parameter measurement of the DC-link capacitor performed in configuration as shown in Fig. 3.5b

It can be seen that the performed measurements provide good insight into the parasitic coupling to ground, in order to determine its size. Furthermore, an accurate estimation of its value is possible since to the DC-link capacitor shows a linear behavior over a wide frequency range. Therefore, a good match was achieved for frequencies up to 2 MHz. The estimated parasitic capacitances based on these measurements of the DC-link capacitor of Fig. 3.6 are listed in Table 3.2.

Measurement point	**Parasitic capacitance**	
	previous [pF]	**new [pF]**
positive rail (m_1)	723	615
midpoint (m_2)	861	613
negative rail (m_3)	983	615

Table 3.2: Comparison of previous and actual estimated parasitic capacitances of the DC-link capacitor against ground for three different measurement points shown in Fig. 3.5a

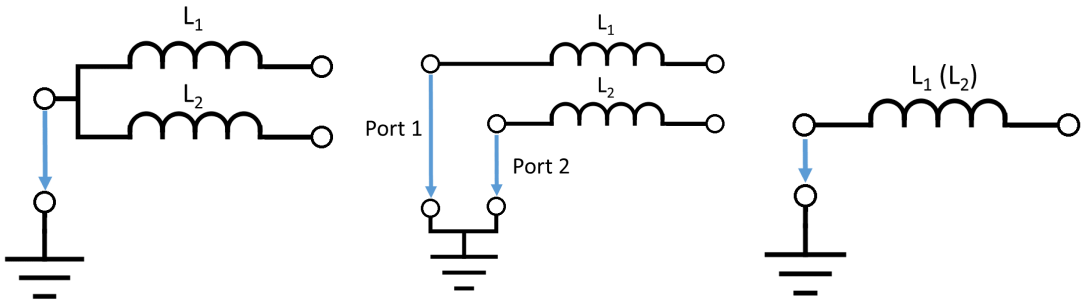
As can be seen, the latest measurements differ from the previous. Furthermore, the new estimated parasitics show only little deviation in comparison to each other, while the previous measurements show more than 25% difference between measurements. This could have been caused by the grounding conditions of the system or the chosen connection point to ground for the measurement. Thus it is assumed that the newly performed measurement results to be more accurate. This is due to the fact that the low differences between all three examined points meet the expectation that each of them shows the same parasitic capacitance. These values serve as the parasitic capacitances of the DC-link capacitor in the mixed-mode simulation model.

As a second approach to identify the parasitic coupling of the component, a 2-port S-parameter measurement was performed as shown in Fig. 3.5b. This was not executed before. The captured data shown in Fig. 3.7 defines the DC-link capacitors frequency behavior in great detail and represents the parasitic coupling seen from both ports of the device. The resulting estimated parasitic capacitances are 1.48 nF seen at port 1 and 1.47 nF seen at port 2. In comparison with the prior results, the values are significantly higher. Therefore, they specify the upper limit of the added parasitics in the mixed-mode model, while the first measurement provides the lower limits. A simulation showed that a change within a range of 1.8 nF to 3 nF in the overall parasitic capacitance of the DC-link capacitor has a very little effect on the CM behavior. In fact, the average amplitude of the resulting CM voltage evinced a change between 0.0022% and 0.16% depending on the supply voltage, which was varied between 10 V and 160 V. For this reason, the effect is

considered as negligible and the value for the parasitic capacitance is set to 2 nF for the DC-link capacitor in the MM model.

3.2.1.2 Coupled Inductor

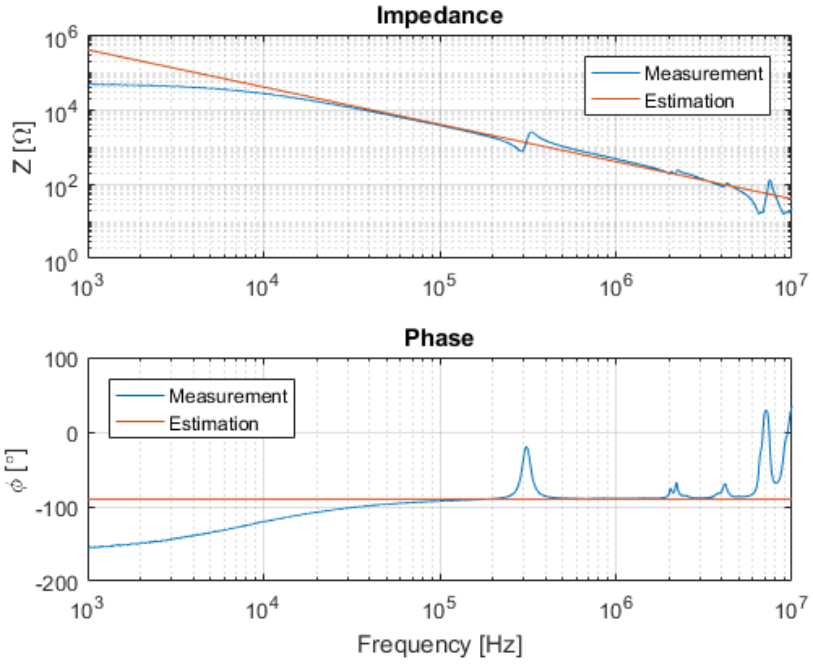
For the measurements of the parasitic capacitances presented by the coupled inductor different configurations of the hardware were used, shown in Fig. 3.8. All measurements were performed under disconnected and de-energized conditions.



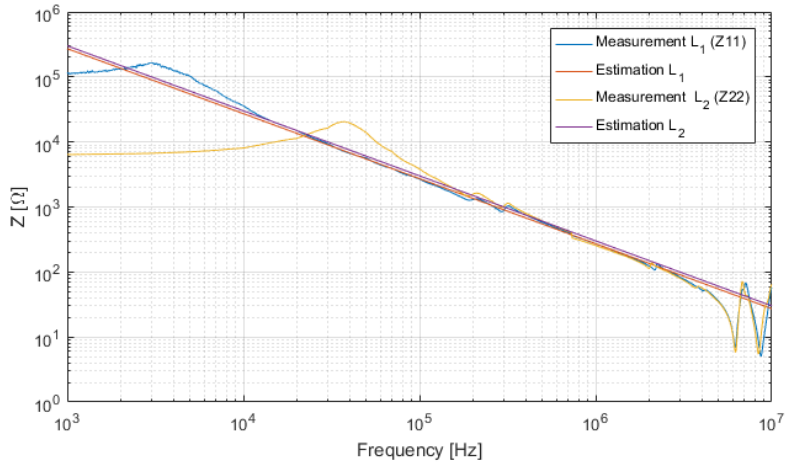
(a) Shorted (b) Open (c) Separated

Fig. 3.8: Various performed measurements of the coupled inductor: (a) One terminal of both inductors were tied together and a one-port measurement against ground was performed. (b) The inductors were separated from each other by disconnecting the short added for measurement (a) and a two-port measurement was performed. (c) Each inductor was individually measured against ground.

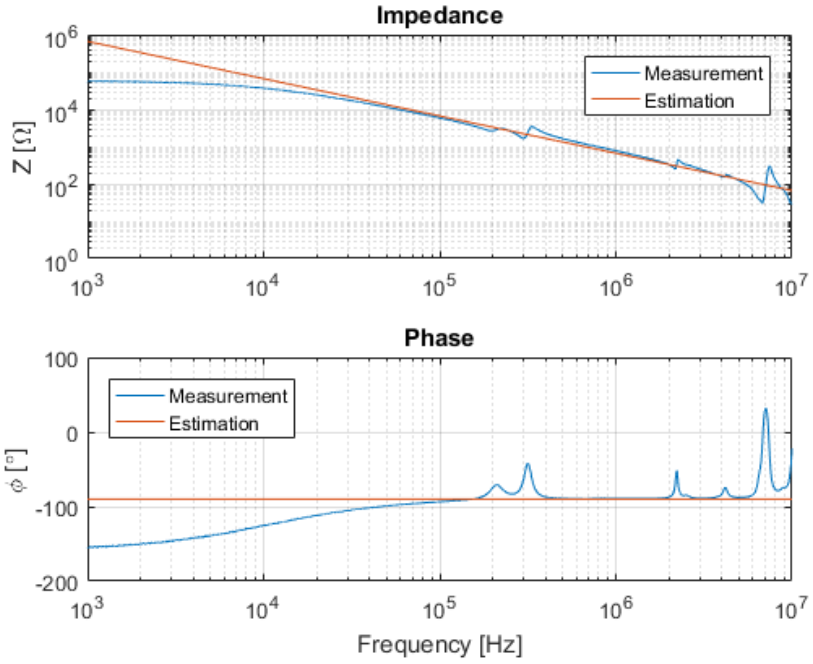
The measurement configuration shown in Fig. 3.8a was taken from the switch side in respect to ground, which demonstrates the total capacitance seen from the filter side. The second setup depicted in Fig. 3.8b describes a 2-port S-parameter measurement. It results in an S-parameter matrix, which contains all data of the device of interest and has to be processed. The details can be read in Chapter 11. This measurement was performed to represent the interactions between the two windings of the coupled inductor. It also includes the same data as obtained by the third measurement structure of Fig. 3.8c. The last measurement configuration represents an impedance measurement of each coil against ground. In sum, four measurements were taken. The tied configuration, the two-port S-parameter measurement and an impedance measurement for each coil. To validate the values of the previously estimated parasitic capacitances of the coupled inductor, the measurements as in [69] were repeated in the same three presented configurations. The impedance behavior for each setup can be seen in Fig. 3.9.



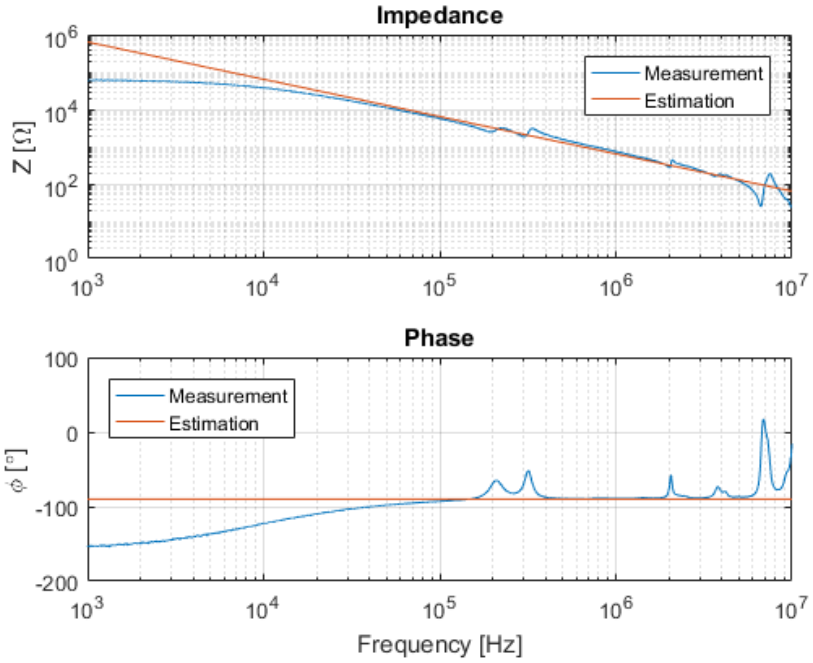
(a) Both coils tied



(b) Two-port S-parameter measurement



(c) Impedance measurement of first inductor



(d) Impedance measurement of second inductor

Fig. 3.9: Measurement of the coupled inductor performed in configuration as shown in Fig. 3.8 and comparison with the estimation of the parasitic capacitance to ground: (a) Measurement configuration shown in Fig. 3.8a, (b) Measurement configuration shown in Fig. 3.8b, (c) Measurement configuration shown in Fig. 3.8c for the first inductor, (d) Measurement configuration shown in Fig. 3.8c for the second inductor

The outcome for the estimated parasitic capacitance to ground of the presented measurement setups are given in Table 3.3 for the execution performed in 2015 and the new performed measurements.

Measurement method	**Parasitic capacitance**	
	previous [pF]	**actual [pF]**
Configuration 3.8a	426	403
Configuration 3.8b, first coil	282	240
Configuration 3.8b, second coil	253	249
Configuration 3.8c, first coil	311	585
Configuration 3.8c, second coil	336	529

Table 3.3: Comparison of previous and actual estimated parasitic capacitances of the coupled inductor against ground for the different measurement configurations shown in Fig. 3.8

In comparison, it can be seen that the outcome of the first two measurement setups show similar values. The deviation of a maximum of 42 pF which can be caused by differently chosen ground points. It is assumed that the divergences between the measurements of the third configuration are caused by the system setup, since grounding of the frame can have a significant impact.

3.2.1.3 Connection Cable

The connection cable between the coupled inductor and the load was also considered to have a parasitic coupling to ground. The cable is of the type XLPE with three phases (two in use) and a length of ten meters. Its parasitics can be modeled in different ways, but the most common simulation model of a cable is a Π-section model as shown in Fig. 3.10. It also represents the most accurate model of the high frequency response of a cable, where the number of Π-sections can be adjusted. The greater the number of Π-sections, the better the match. The parasitic elements (i.e. parasitic capacitance to ground, series inductance and series resistance), have to be specified per unit of length and calculated based on number of Π-sections used.

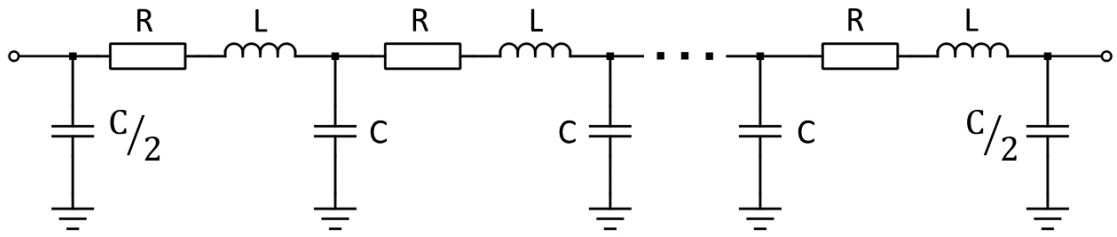


Fig. 3.10: Representative Π-section model of a cable

Copper has a conductivity of $\kappa = 56\ \frac{m}{\Omega \text{mm}^2}$, which mainly defines the induced parasitic serial resistance of the cable without considering its connection points. For the first estimation of the serial resistance for low frequencies follows:

$$R_c = \varrho \cdot \frac{l}{A} = \frac{1}{\kappa} \cdot \frac{l}{r^2\pi} = \frac{1}{56\ \frac{\text{m}}{\Omega\,\text{mm}^2}} \cdot \frac{10\ \text{m}}{1\ \text{mm}^2 \cdot \pi} = 56.8\ \text{m}\Omega \tag{3.2}$$

This does not include the additional resistance of the connections. The parasitic capacitance to ground was determined by an impedance measurement similar to the configuration of the coupled inductor as shown in 3.8b. The outcome for the impedance measurement can be seen in Fig. 3.11.

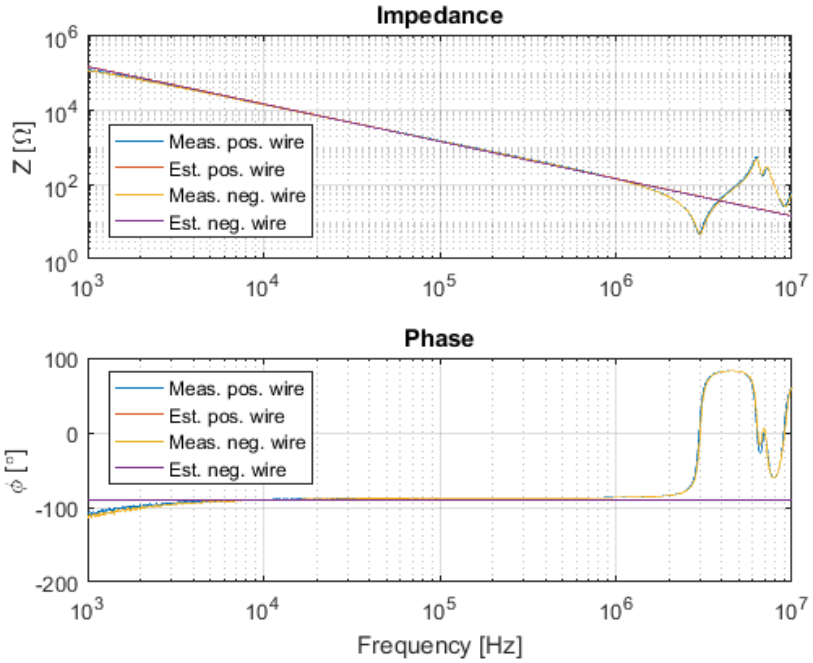


Fig. 3.11: Parasitic capacitive coupling to ground of the cable

The measurement shows that both wires show a similar behavior as expected. The first wire exhibits a parasitic capacitance of 1.11 nF to ground while the second wires shows a value of 1.25 nF. To determine the serial resistance and provided serial inductance of

the connection cable an impedance measurement was performed. As measurement points both terminals (i.e. ends) of the cable were used. The result is shown in Fig. 3.12

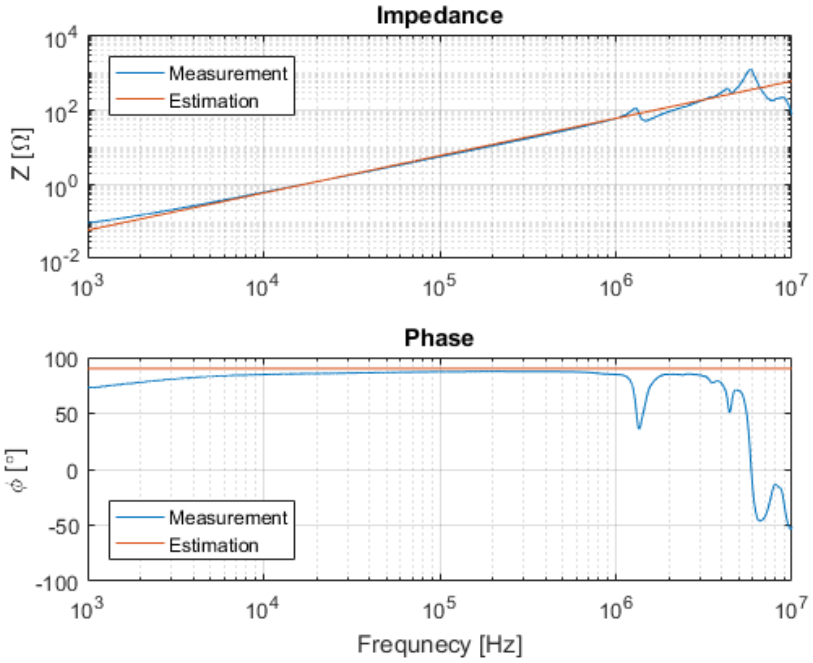


Fig. 3.12: Bode-plot of the connection cable to evaluate the induced serial resistance and inductance

The induced serial resistance is approximately 80 mΩ, which is a valid value considering the additional resistance induced by the connections of the cable and deviation caused by the measurement itself. The estimated parasitic inductance is 9.11 nH. Since the serial resistance of the cable is much smaller than the load resistance of 100 Ω and its inductance is also far lower than the impedance provided by the coupled inductor (1.1 mH) the effect of both parasitic elements can be neglected. Furthermore, the impact of the parasitic capacitance of the cable on the CM behavior of the PEBB is considered negligible since the CM currents circulate within the shortest provided path back to its source, which is the inverter. This hypothesis proved to be correct since the outcome of the simulation of the CM quantities were only slightly affected by the additional parasitic coupling of the cable to ground.

3.2.1.4 Inverter

In [41] the authors extended the DM model to the MM model and determined the switching elements as source of the CM voltage of the investigated system, without considering any parasitic coupling effects of the inverter or rectifier. In comparison to that approach, this thesis includes the parasitic coupling of each MOSFET from its heat sink to ground,

which was studied in [34, 53, 54]. To determine the parasitic coupling to ground of the switching devices, impedance measurements or S-parameter measurements would have to be performed of each MOSFET to ground. This was not possible due to the hardware setup, since the MOSFETs are included in a half-bridge module without the possibility of access to a single device. Therefore, the information of a former analysis of the half-bridges [70] was used to estimate the expected inherent parasitic capacitances. In this analysis it is mentioned that a comparison of different modules illustrates that the module baseplate capacitance appears to be more closely correlated to the module current rating than to the module voltage rating. Values between 0.26 nF and 1 nF are listed for different SiC MOSFET modules. For the mixed-mode model the measured maximum of 1 nF was used.

The included snubber capacitors parallel to each SiC MOSFET were also considered to have an additional impact on the parasitics. Measurements to achieve an insight into their frequency behavior and parasitic properties as performed for the DC-link capacitors or the coupled inductor could not be performed, since those capacitors are directly between two half-bridge modules and the low inductive plate, which connects the DC-link capacitors with the H-bridge. Therefore, a disconnection of these circuit elements was not possible.

3.2.1.5 Power Source

A last source of parasitics is the DC power supply. In this case, it was barely possible to find any sources, which mention the impact of the power source on parasitic coupling to ground. Furthermore, parasitic coupling to ground strongly depends on the type of power source used.. Based on previous knowledge and practical experience of workers at CAPS, a value of 10 nF for the parasitic capacitance was used.

The resulting MM circuit can be seen in detail in Fig. 3.13 and Fig. 3.14. In this simulation model all previously discussed and considered parasitics are included.

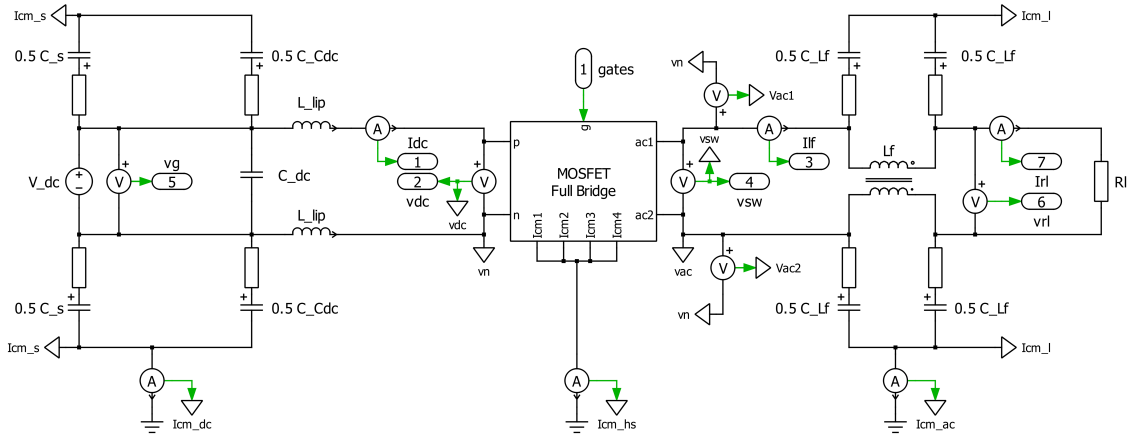


Fig. 3.13: Detailed MM model of the PEBB which includes parasitic capacitances to ground

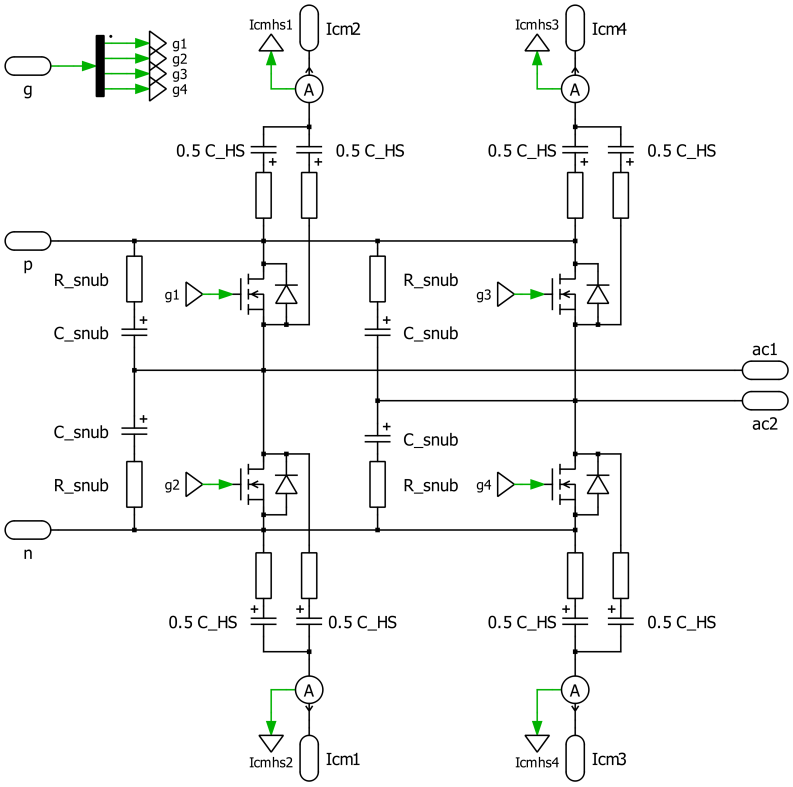


Fig. 3.14: H-bridge model of the mixed-mode model

During the simulation process, the impact of the low inductive plate is not negligible, since the linear inductance of the plate has a direct impact on the occurring CM current peaks. Therefore, an additional serial inductance was added between the DC-link capacitor and the input of the H-bridge for both rails as shown in Fig. 3.13 with L_{lip}.

All used values of the components for the simulation of the MM model are the same as for

the DM model and are shown in Table 3.1. The values of the added parasitic capacitances to ground are listed in Table 3.4.

System component	Description	Indication	Value
Source side	DC voltage source	C_s	10 nF
	DC-link capacitor	C_{Cdc}	2 nF
Inverter	SiC MOSFET	C_{HS}	1 nF
Load side	Coupled inductor	C_{Lf}	400 pF

Table 3.4: Values of the components parasitic capacitance to ground of the MM model

3.2.2 Solver Settings

In order to obtain correct simulation data, one has to consider the solver settings. The underlying computation engine of MATLAB®/Simulink/PLECS Blockset is a variable step ordinary differential equation (ode) solver. The numerical accuracy of the performed simulations showed a strong dependency on the solver settings. Furthermore, they also affect the simulation time. The most important options are: type, minimum and maximum time step size, solver reset type and tolerance. An improper adjustment of these settings can lead to a wrong signal output or can significantly slow down the speed of the simulation. An optimal adjustment of the solver is correlated to advanced skills and experience using MATLAB®. It can take several trials to find a suitable configuration, since it is often a trade-off between simulation speed and accuracy. For the performed simulations the ode15s variable step stiff solver showed the best results and was used in [27] with success, but the minimum time step size had to be set to a value of 0.1 ps in order to solve the simulation, because of the values of the parasitic capacitances. An increase of this value lead to numerical problems and a termination of the simulation as the nonlinear iteration would not converge. Hence, this limitation substantially increased the duration of the simulation. However, PLECS® Standalone offers other solvers, like the RADAU solver, which is also a variable-step solver for stiff systems using a fifth-order accurate fully-implicit three-stage Runge-Kutta formula [71], which results in higher values of the minimum time step. The used settings are listed in Table 3.5.

Setting option	**MATLAB®/Simulink/ PLECS Blockset**	**PLECS Standalone**
Type	variable step	variable step
Solver	ode15s (stiff/NDF)	RADAU (stiff)
Min. step size	1e-13	–
Max. step size	auto	1e-3
Initial step size	auto	200e-9
Relative tolerance	1e-4	1e-4
Solver reset method	Fast	–

Table 3.5: Solver settings for performed simulations in MATLAB®/Simulink/PLECS Blockset and PLECS® Standalone

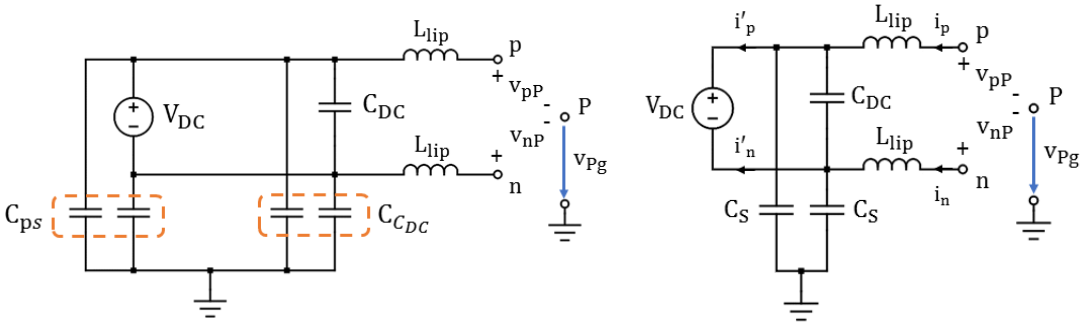
It has to be mentioned that both solvers resulted in different outcomes, due to the lower time steps used by the ode solver. The further data processing was more efficient by the use of MATLAB®/Simulink in combination with PLECS® Blockset, due to the possibility of saving the data directly into the workspace after the simulation. This resulted in an increased speed of the simulation, since the data had not to be written into a file after each time step. Therefore, is was decided to use MATLAB®/Simulink/PLECS Blockset software configuration and the ode15s solver.

3.3 Common-Mode Model

As described in [41], the first step to model a CM equivalent circuit is to split the model into different parts, generate its CM equivalent circuit and attach them together to form the CM equivalent system model. Therefore, the DM model gets split into three sections: the source side, the inverter and the load side. The source side includes the power source and the DC-link capacitor. It is known that the inverter is a source of CM voltage. Therefore, it will be replaced by a controlled voltage source in the CM equivalent model, which will provide the circuit with the inherent CM voltage. The parasitic capacitances of the MOSFETs heat sink to ground are split into two equal parts and symmetrically placed on both sides of the CM voltage source. The load side includes all elements on the AC side of the circuit. This comprises the coupled inductor and its parasitics along with the resistor.

3.3.1 Common-Mode Circuit

In order to transform the DM model into its CM equivalent, one must determine the phase voltage with respect to an arbitrary reference point P as shown in Fig. 3.15a.



(a) (b)

Fig. 3.15: Source model with parasitic capacitances to ground: (a) detailed, (b) remodeled and simplified

In this figures p and n represent the positive and negative rail of the DC side of the system. The application of Kirchhoff's voltage law (KVL) results in the following loop equation for each of the two phases:

$$v_{pP} + v_{Pg} = \frac{1}{C_s} \int (i_p - i'_p)dt + L_{lip} \cdot \frac{di_p}{dt} \tag{3.3}$$

$$v_{nP} + v_{Pg} = \frac{1}{C_s} \int (i_n - i'_n)dt + L_{lip} \cdot \frac{di_n}{dt} \tag{3.4}$$

Starting from connection p the first loop goes from P to ground over the parasitic capacitance C_S and over the inductance L_{lip} back to its origin. In the same manner the second loop is formed for the negative rail with its start point at connection n. The two loop equations are summed up and the equation can be rewritten.

$$2v_{Pg} + (v_{pP} + v_{nP}) = \frac{1}{C_s} \int [(i_p + i_n) - (i'_p + i'_n)]dt + L_{lip} \cdot \frac{d}{dt}(i_p + i_n) \tag{3.5}$$

$$v_{Pg} = -\frac{1}{2}(v_{pP} + v_{nP}) + \frac{1}{2C_s} \int [(i_p + i_n) - (i'_p + i'_n)]dt + \frac{1}{2}L_{lip} \cdot \frac{d}{dt}(i_p + i_n) \tag{3.6}$$

By applying Kirchhoff's current law (KCL) it follows that

$$i'_p + i'_n = 0 \tag{3.7}$$

Furthermore, the CM definition provides

$$i_{CM} = i_p + i_n \tag{3.8}$$

$$v_{CM} = \frac{1}{2}(v_{pP} + v_{nP}) \tag{3.9}$$

One obtains a suggestion for a CM equivalent model for the circuit part shown in Fig. 3.15b, by implementing the three resulting Equations 3.7, 3.8 and 3.9 into equation 3.6. This yields in

$$v_{Pg} = -v_{CM,s} + \frac{1}{2C_s}\int i_{CM}dt + \frac{1}{2}L_{lip} \cdot \frac{di_{CM}}{dt} \tag{3.10}$$

where $v_{CM,s}$ is the CM voltage produced by the source. The DC power supply CM voltage is neglected in this thesis, because the CM influence on the system is unknown. Therefore it is removed from the equation and the resulting CM equivalent model of the source can be seen in Fig. 3.20 circled in blue. To derive the CM equivalent model of the load side the same procedure is used. The load side is depicted in Fig. 3.16.

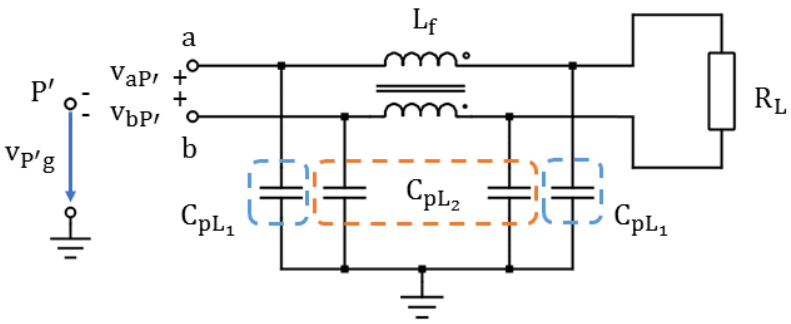
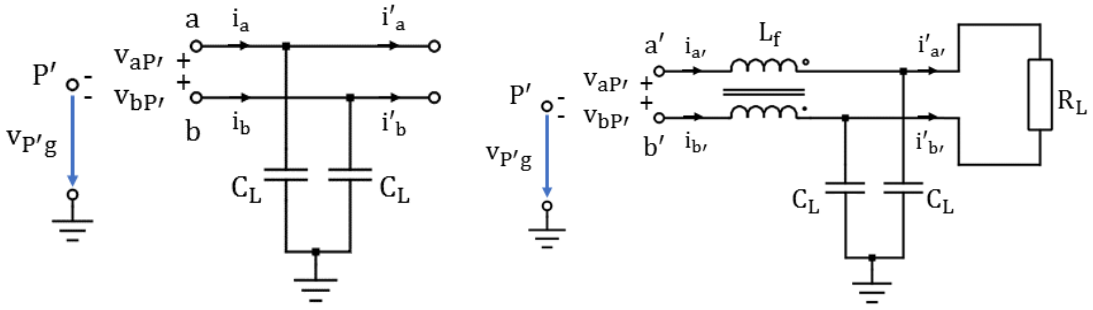


Fig. 3.16: Load model with parasitic capacitances to ground

For an easier understanding the circuit can be split in two different parts as shown in Fig. 3.17.



(a) Parasitics in front of the coupled inductor

(b) Coupled inductor, following parasitics and load resistance

Fig. 3.17: Load model with parasitic capacitances to ground

For each circuit shown in Fig. 3.17 two different loops exist to apply KVL. The two loops for the circuit depicted in Fig. 3.17a results in

$$v_{P'g} + v_{aP'} = \frac{1}{C_L} \int (i_a - i'_a) dt \tag{3.11}$$

$$v_{P'g} + v_{bP'} = \frac{1}{C_L} \int (i_b - i'_b) dt \tag{3.12}$$

The following two equations describe the two loops over the parasitic grounding in Fig. 3.17b.

$$v_{P'g} + v_{aP'} = L\frac{di_{a'}}{dt} + \frac{1}{C_L} \int (i_{a'} - i'_{a'}) dt \tag{3.13}$$

$$v_{P'g} + v_{bP'} = L\frac{di_{b'}}{dt} + \frac{1}{C_L} \int (i_{b'} - i'_{b'}) dt \tag{3.14}$$

The summation and transformation of Equation 3.11 and 3.12 in the same manner as for the previous calculation yields

$$v_{P'g} = -v_{CM,l_1} + \frac{1}{2C_L} \int (i_{CM} - i'_{CM}) dt \tag{3.15}$$

while the same procedure for Equation 3.13 and 3.14 results in

$$v_{P'g} = -v_{CM,l_2} + L\frac{di'_{CM}}{dt} + \frac{1}{2C_L} \int (i'_{CM}) dt \tag{3.16}$$

where v_{CM,l_1} and v_{CM,l_2} are the CM voltages produced by each part of the load side. Both are equal to zero and can be removed from the equation. The voltage from point a to ground and the voltage from point a' to ground are equal. Same goes for the voltages of point b and b' to ground. Since there is no change of voltage between the connection parts of the two parts, the suggested CM equivalent models can be connected in series. The resulting circuit is shown in Fig. 3.20 circled in orange.

The last remaining part to discuss is the inverter itself shown in Fig. 3.18. This part of the system contains the CM voltage source. Therefore, it will induce CM current for the whole CM equivalent model.

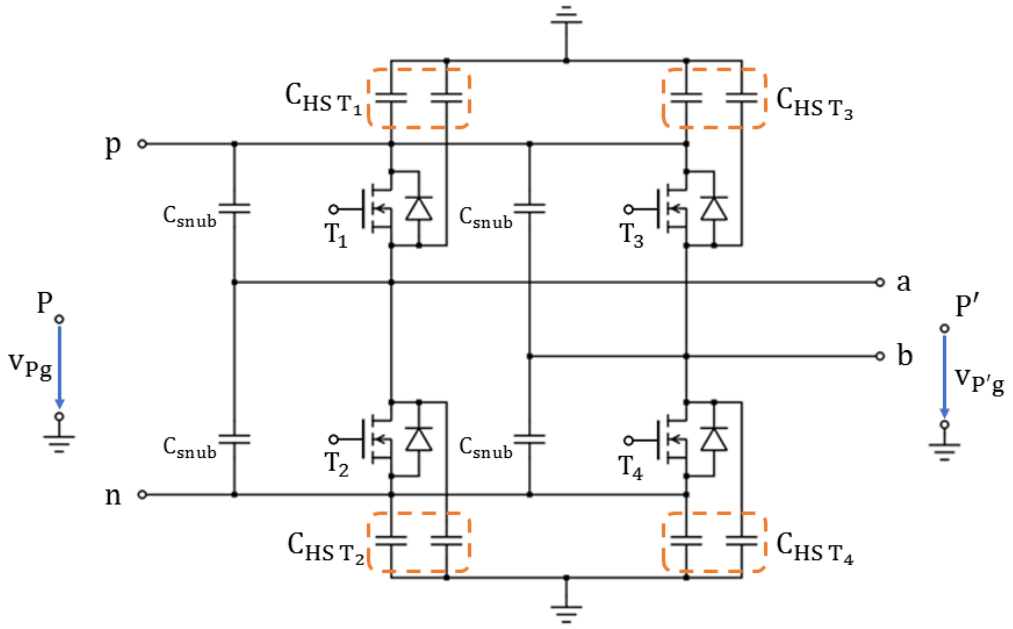


Fig. 3.18: Inverter model with included parasitics to ground

The parasitic capacitances can be seen in a different way. Both parasitics from the positive rail to ground (one part of C_{HST_1} and C_{HST_3}) an the negative rail to ground (one part of C_{HST_2} and C_{HST_4}) can be fused into one capacitor, respectively. In the same manner this can be done for the parasitics from each wire (a and b) of the AC side to ground. This configuration yields the circuit shown in Fig. 3.19.

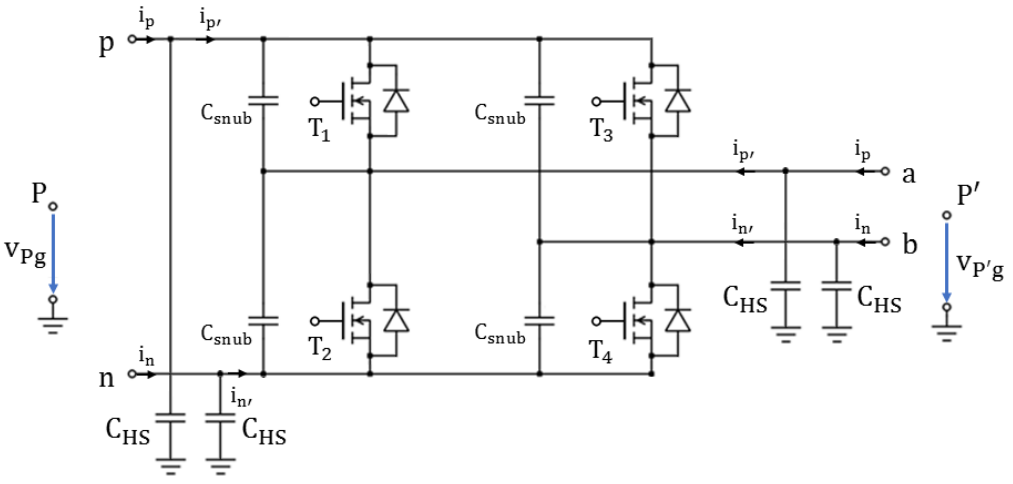


Fig. 3.19: Inverter model with reordered and fused parasitic coupling

All parasitic capacitors of the heat sink to ground are assumed to show an equal value and therefore labeled with the same name C_{HS}. By applying KVL for the DC side the

following two equations are derived:

$$v_{Pg} + v_{pP} = \frac{1}{C_{HS}} \int i_p - i'_p \tag{3.17}$$

$$v_{Pg} + v_{nP} = \frac{1}{C_{HS}} \int i_n - i'_n \tag{3.18}$$

As in the calculations before, the equations can be summed up and rewritten to yield in:

$$v_{Pg} = -v_{CM,DC} + \frac{1}{2C_{HS}} \int i_{CM} - i'_{CM} \tag{3.19}$$

For the AC side the same procedure yields

$$v_{P'g} + v_{aP'} = \frac{1}{C_{HS}} \int i_a - i'_a \tag{3.20}$$

$$v_{P'g} + v_{bP'} = \frac{1}{C_{HS}} \int i_b - i'_b \tag{3.21}$$

By repeating the above process, the result is similar to the DC side

$$v_{P'g} = -v_{CM,AC} + \frac{1}{2C_{HS}} \int i_{CM} - i'_{CM} \tag{3.22}$$

These equations suggest a CM equivalent model of the inverter with two different CM voltage sources: one for the DC side and one for the AC side. These two sources can be combined into one, but it has to be considered, where the source is placed and how the inverter model is constructed. For the simulation it was decided to place the CM voltage source between the occurring parasitics of the inverter, in order to keep the circuit simple and symmetric. The polarity of the source was chosen, due to the CM voltage as calculated by the simulation results with the negative rail of the DC side between the inductance of the low inductive plate and the inverter as arbitrary point. This means, all other connection points of the inverter (both rails of the AC side and the positive rail of the DC side) were measured against this point. The result can be seen in Fig. 3.20 circled in green.

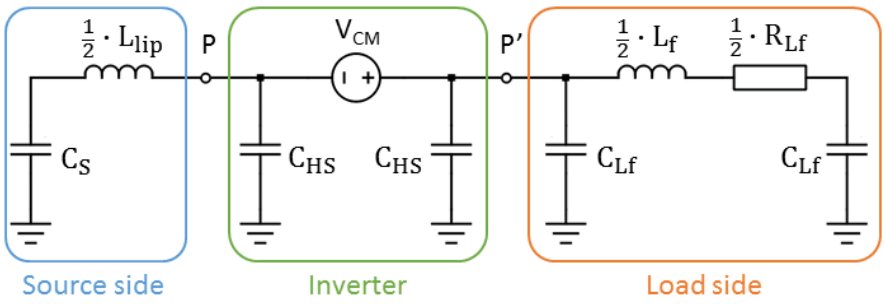


Fig. 3.20: Simplified circuit of the CM equivalent model

Fig. 3.20 shows all derived and built CM subsystems parts (source, inverter and load)

connected together.

3.3.2 Common-Mode Voltage Source

The CM voltage can be obtained in several different ways. It can be derived analytically, it can be calculated with captured simulation data and it can be measured. The analytical approach is only possible, if there is great knowledge of the switching pattern and switching control a priori. In the case of the PEBB, a PWM was used with a sinusoidal modulation index $m = m_i \cdot sin(2\pi f)$ with an amplitude $m_i = 0.9$ and its frequency $f_{AC} = 60\,Hz$. The switching frequency of the inverter was 10 kHz and measurements of the master control output showed a dead time of 2.5 μs for each switch. One carrier signal is used for each half-bridge to generate the gate signals. With this knowledge it would be possible to derive the CM voltage analytically, but this method was not used in extent of this work. In order to keep any occurring oscillation and noise within the captured CM voltage signal by using a simulation model, it was decided to use a controlled voltage source within the CM model and transfer the saved data of the a previous performed simulations directly by the use of a lookup table. As mentioned before, the CM voltage of the simulation is derived by measuring the positive rail of the DC side and both rails of the AC side in reference to the negative rail of the DC side. Afterwards, both captured voltages get summed and averaged. This represents the CM voltage on the AC side.

$$V_{cm,AC} = \frac{V_{an} + V_{bn}}{2} \tag{3.23}$$

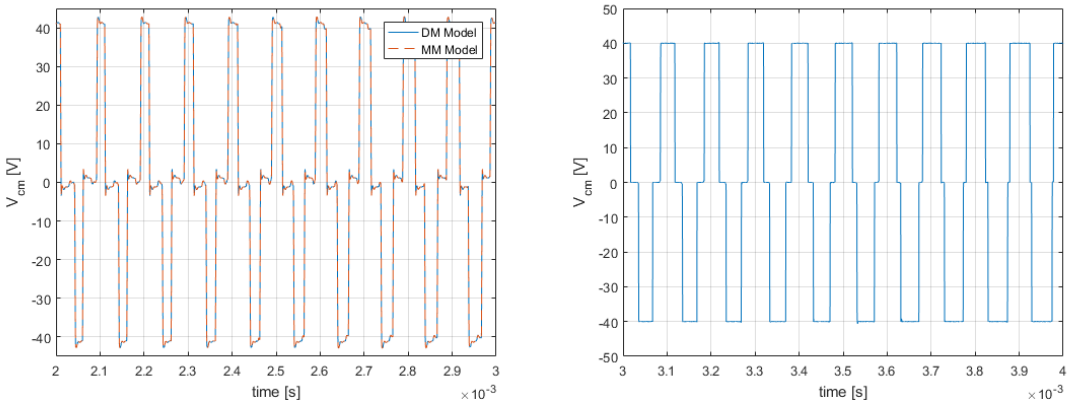
The CM voltage of the DC side is half of the supply voltage.

$$V_{cm,DC} = \frac{V_{DC}}{2} \tag{3.24}$$

The overall CM voltage for the controlled source in the CM equivalent is the difference between both voltages.

$$V_{cm} = V_{cm,AC} - V_{cm,DC} \tag{3.25}$$

A simulation of the DM model and the MM model showed that the resulting CM voltages of both models are congruent. This can be seen in Fig. 3.21a for a supply voltage of 80 V. Therefore, both datasets can be used as source for the lookup table in the CM model.



(a) CM voltage of the DM and the MM model

(b) CM voltage under use of ideal MOSFETs and without low inductive plate

Fig. 3.21: CM voltage with ideal and non-ideal MOSFETs for 80 V supply voltage

The peaks and waves of the signal have several causes. The use of non-ideal MOSFETs, free-wheeling diodes and the inductances provided by the low inductive plate have a major influence of CM voltage behavior. The result of a simulation with ideal switching devices and neglection of the low inductive plate can be seen in Fig. 3.21b.

By using the outcome of the simulations directly in a lookup table within the CM equivalent circuit, it is ensured that any effect on the CM voltage of the whole system represented with the MM model is also included in the CM model. These effects would be lost if the analytical approach would have been used, since it does not take the influences of other system components into account. Furthermore, a measurement was performed of the CM voltage on the physical device. This is described in detail in Section 4.4.3.

3.4 Frequency Dependent Simulation Components

To reproduce the behavior of the DUT as accurate as possible, it is important to take the frequency behavior of each included component of the device into consideration. It is well known that all passive devices behavior changes with rising frequency.. Real components have many parasitic circuit elements (i.e parasitic inductance, capacitance and resistance), which become relevant at high frequencies. For example, real inductors and capacitors always will show a self-resonance at a certain frequency, because of their non-ideal behavior. Also resistors can exhibit a self-resonance, but for this component it depends on its physical structure and material. Therefore, equivalent models for real resistors, capacitors and inductors are created, which possess the capability to match the frequency response of their real complement in the range of 1 kHz to 5 MHz, the focused frequency range of interest. Subsequently, this leads to a more detailed and precise modeling approach of

the PEBB. All components of the equivalent circuits with the suffix p represent parasitic elements of the actual device.

3.4.1 Resistor

To reproduce the frequency response of a component, first one has to understand which parasitics occur and in which frequency band they will dominate. An equivalent circuit for a resistor is depicted in Fig. 3.22 as presented in [72]. L_p represents the parasitic inductance induced by the external connection of the resistor and its physical structure (e.g. number of windings), which has typical values in the range of tenth of nH, while C_p represents the parasitic capacitance between the windings or end-to-end of the resistor with typical values of several pF.

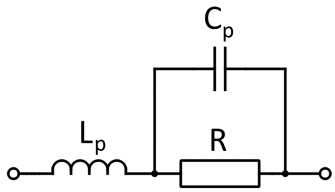


Fig. 3.22: Equivalent model of a real resistor

For low frequencies the impedance of the series parasitic inductance is rather low and the impedance of the parasitic capacitance is significantly larger in comparison to the resistor. Therefore, the resistor will dominate the magnitude of the impedance. With rising frequency the impedance associated with the parasitic capacitance decreases and the model shows a capacitive behavior. At a certain frequency its impedance is equal to the value of the intrinsic resistor, which means

$$R = \frac{1}{j\omega C_p} \tag{3.26}$$

When the frequency exceeds that point, more current will start to flow through the conducting path provided by the parasitic capacitance. The parasitic inductance still exhibits only a very low impact on the overall impedance, which subsequently will further decrease until it reaches its minimum at the self resonant frequency of the replication of the physical resistor .

$$\omega_0 = \frac{1}{\sqrt{L_p C_p}} \tag{3.27}$$

with $\omega_0 = 2\pi f_0$. After surpassing this frequency the impedance gets dominated by the parasitic inductance and the frequency response of the model equals the behavior of an inductor. An example of the described frequency behavior of a resistors impedance Z is shown in Fig. 3.23. For the simulation a resistor with 1 kΩ, a parasitic capacitance of 1 pF

and a parasitic inductance of 10 nF was used.

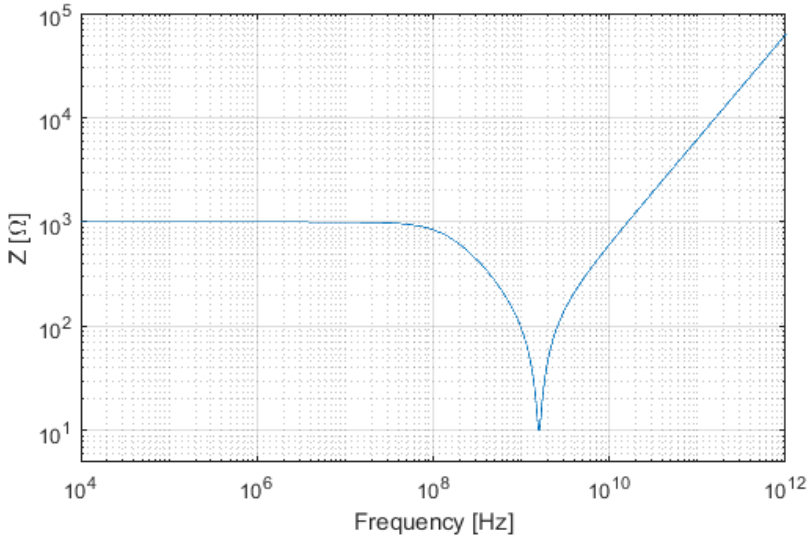


Fig. 3.23: Frequency response of the equivalent model of a resistor

The frequency behavior of a resistor strongly depends on its material and physical structure. An impedance measurement of a 100 Ω power resistor which is used as load for the energized measurements showed a capacitive behavior for higher frequencies, which does not correlate with the proposed wide frequency bandwidth model. Its behavior is depicted in Fig. 3.24.

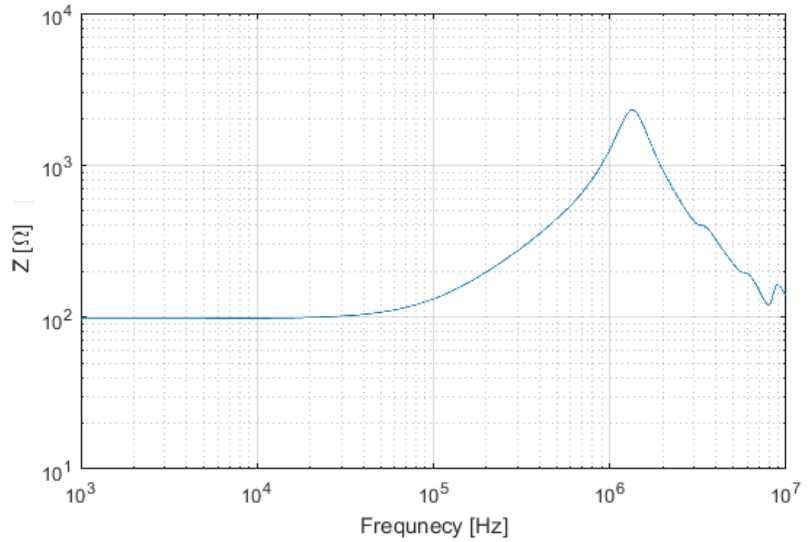


Fig. 3.24: Frequency response of a 100 Ω power resistor

As it can be seen, its frequency response shows an inductive behavior at first and after the

resonance frequency the resistors behavior is similar to a capacitor. Therefore, the model should not be used as a component for the power resistor in the simulation model, because it would cause higher deviations than a standard provided resistor model. This is the reason, why it is not used in the detailed model for the frequency domain representation of the DUT.

3.4.2 Capacitor

The parasitics of a capacitor are a combination of parasitic inductance (L_p), capacitance (C_p) and resistance R_p. L_p is induced by the components leads and/or by a magnetic field generated by the capacitor, which in turn leads to inductance in the structure. This parasitic component is seen as serial inductance to the main capacitance C. On the one hand, a parasitic resistance is introduced by the resistance of the dielectric layer between the capacitor plates in parallel to the ideal capacitor, which is also known as an effect of dielectric absorption. On the other hand an additional resistance R_p is caused by the capacitors plates itself, due to their finite conductivity. In literature and data sheets this parasitic resistance is often referred to as effective series resistance (ESR) [73]. The parasitic shunt resistance between the plates is very large and since it is seen in parallel to C, it can be modeled as open circuit and is neglected. Furthermore, a parasitic capacitance (C_p)is present, which is also induced by the leads, but in comparison to the device's ideal bulk capacitance, this parasitic effect can be also neglected. As proposed in [72], the resulting equivalent circuit is a serial oscillation circuit as shown in Fig. 3.25.

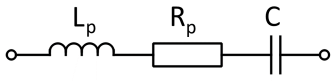


Fig. 3.25: Equivalent model of a real capacitor

L_p exhibits typical values in the range of several nH, while R_p contributes a resistance of tenth of mΩ. The capacitor's nominal value is represented by C. As for the resistor, the capacitors structure has an impact on the components parasitics.

For low frequencies the capacitor of the equivalent circuit dominates the inductance. Consequently, it will decrease like an ideal capacitor with increasing frequency up to the resonance frequency of

$$\omega_0 = \frac{1}{\sqrt{L_p C}} \tag{3.28}$$

which is inevitable for any real capacitor. At this frequency the equivalent circuit is in self-resonance and its impedance reaches the minimum, which is purely real and defines the parasitic resistance R_p of the capacitor. When the frequency exceeds the components resonance, the parasitic inductance will dominate the impedance. Hence, it will increase

with rising frequency and the frequency response of the equivalent model will evince + inductive behavior.

The described behavior with rising frequency is shown in Fig. 3.26. It can be seen that a good correlation was accomplished between the measured and the simulated frequency response in the frequency range of interest.

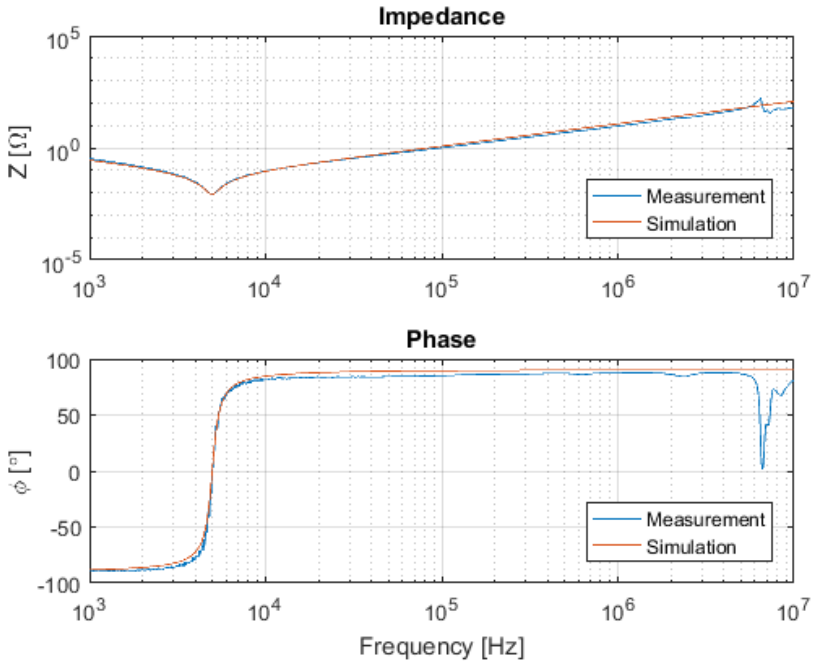


Fig. 3.26: Bode diagram of a real capacitor and the equivalent simulation model

The simulation model was fed with values derived by the impedance measurement of the DC-link capacitor of the PEBB. The parasitic serial resistance is equal to the minimum value of the impedance. This resulted in a value of $R_p = 8.4$ mΩ. The capacitance of the measured component was calculated by the mean of three points within the linear behavior for frequencies below 4 kHz. This lead to a value of $C = 634.97$ μF. In the same manner the value of the inductance was determined. The inductance was calculated for five points between 20 kHz and 2 MHz and the results were averaged which lead to a total parasitic inductance of $L_p = 1.61$ μH. This values result in a resonance frequency of $f_0 = 4.98$ kHz. The reached accuracy is shown in Fig. 3.27.

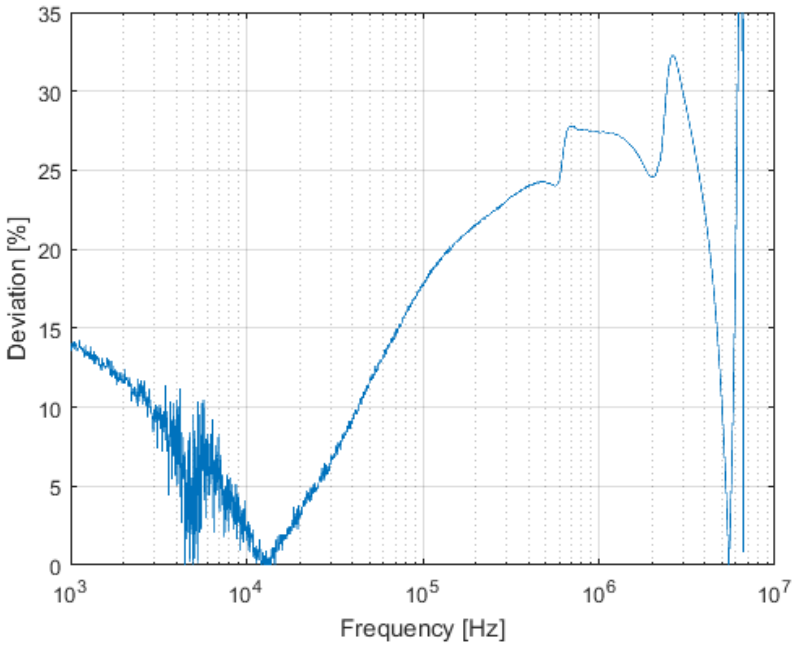


Fig. 3.27: Derivation between the simulation of the equivalent capacitor model and the measurement

The smallest deviation was reached in a frequency range around the resonance frequency. For higher frequencies the deviation rises, until the measured impedance starts to fluctuate at 5 MHz. At the one hand, this could be caused by additional parasitics, which are not taken into account with the simulation model, but on the other hand, this could be a result of the fixture, which was used for the measurement, since its impact on the resulting impedance increases with higher frequencies. Its frequency behavior is described in Section 3.4.4 in more detail. The precision of the equivalent circuit to the performed real life measurement is considered as good enough to implement to reproduce the behavior of the PEBB in greater detail.

3.4.3 Inductor

For a equivalent model of an inductor, parasitics not only have to be taken into account, but also the magnetic saturation. The windings contribute a serial resistance R_p (R_{ps}) as well as a parasitic capacitance between each winding as depicted in Fig. 3.28.

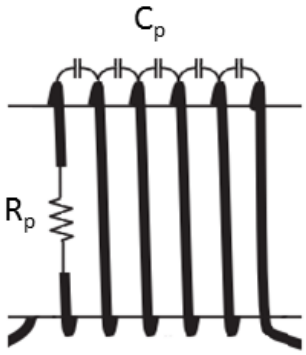


Fig. 3.28: High frequency inductor geometry

For inductors with small magnetic losses, the mentioned parasitics yield in the equivalent model shown in Fig. 3.29 [72, 74]. However, as soon as the magnetic losses reach considerable dimensions, an additional parasitic component has be added to the model.

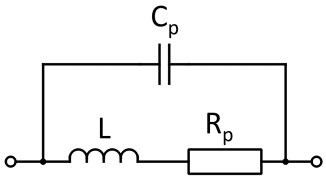


Fig. 3.29: Equivalent model of a real inductor with small magnetic losses

The magnetic losses can be modeled as a parallel resistor R_{pp} across the nominal inductance L and its serial resistance R_{ps}. The extended equivalent circuit, which takes the magnetic losses into consideration is shown in Fig. 3.30 [74].

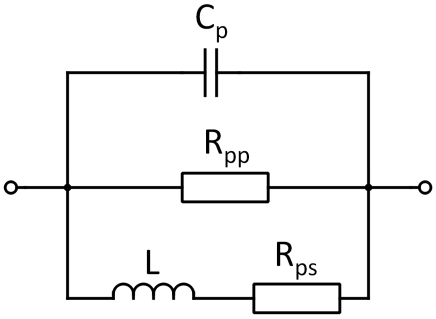


Fig. 3.30: Equivalent model of a real inductor with large magnetic losses

The value of this additional parasitic element can be calculated by using the quality factor

Q, which can be mostly gained from the data sheet of the corresponding inductor [74].

$$Q = \frac{R_{pp}}{\omega_0 L} \tag{3.29}$$

Both presented models are dominated by the serial resistance R_{ps} for very low frequencies. With rising frequency the impedance is specified by the inductance and shows a linear behavior up that point, where the device's self-resonance occurs

$$\omega_0 = \frac{1}{\sqrt{LC_p}} \tag{3.30}$$

and the impedance of the inductor reaches its maximum. For frequencies beyond the resonance, the parasitic capacitance C_p dominates the overall impedance, which in turn decreases with increasing frequency. The result of the measurement and both simulation models can be seen in Fig. 3.31.

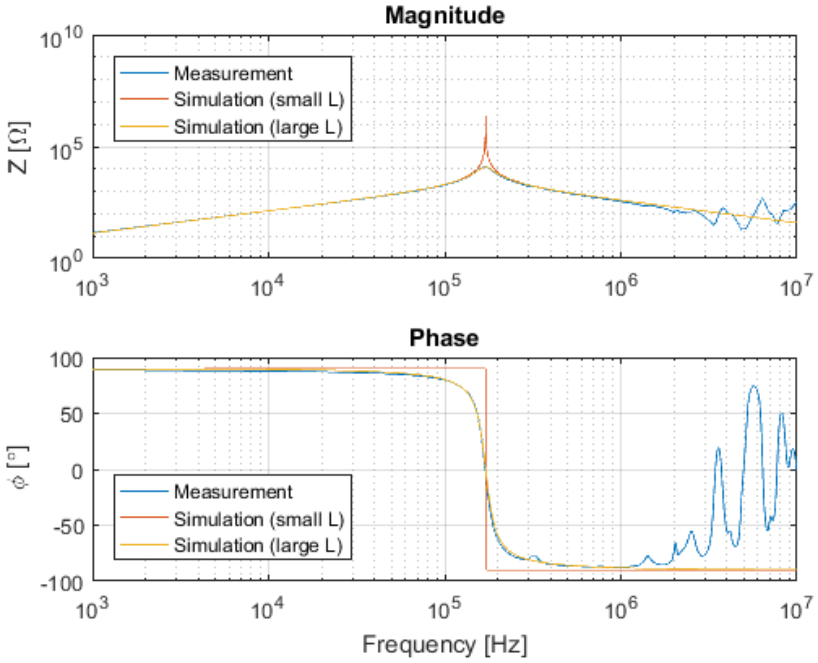


Fig. 3.31: Bode diagram of a real inductor and the equivalent simulation model

In the case of the PEBB, the inductor does not have a data sheet. Therefore, the value of R_{pp} was progressively determined empirically. This resulted in a value of 12 kΩ. The serial parasitic resistance R_{ps} was estimated by the offset between the measurement and simulation at the lowest captured frequency points, 148 mΩ. The inductance L and the parasitic capacitance C_p were calculated in the same way as for the capacitor before. The averaged value of different points in the linear sections gave a value of 2.1 mH for the inductance L and a value of 404.2 pF for the inductor's parasitic capacitance C_p. These

values result in a resonance frequency of 170.85 kHz, which shows a deviation of 1.1 kHz in comparison to the measurement.

As it can be seen in Fig. 3.31, the equivalent inductor model for negligible magnetic losses results in a sharp transition from inductive to capacitive behavior in comparison to the extended model and the impedance measurement of the real component itself. It can also be gathered that the magnetic losses have only a significant impact on the impedance for frequencies near the resonance point. Therefore, both models achieve similar results for low and high frequencies relating to the impedance and accuracy. The deviation of both models in relation to the measured outcome is depicted in Fig. 3.32

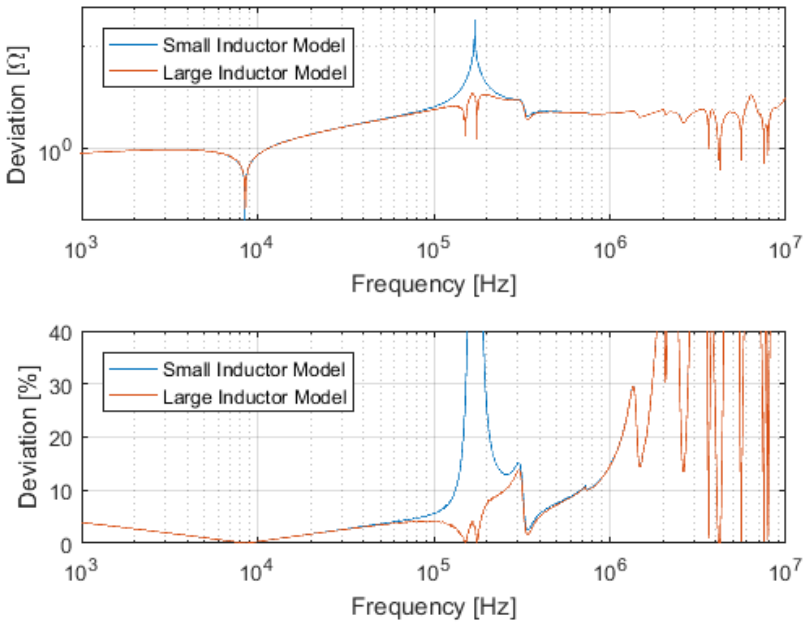


Fig. 3.32: Derivation between the simulation of the equivalent inductor model and the measurement

It can be seen that accuracy was achieve, especially for frequencies below the self-resonance of the inductor. For higher frequencies the deviation rises again, similar to the result of the capacitor. Again, this could be caused by additional parasitics, which are not taken into account with the simulation model or by the fixture used during measurement.

3.4.4 Fixture

The effect of the fixture used for the performed measurements had a major influence on the resulting impedance at higher frequencies. Its impact limits the accuracy of the presented equivalent circuits, since the fixture exhibits additional parasitics and shows an inductive

behavior for high frequencies as shown by Fig. 3.33. This can cause additive resonance for frequencies above 3 MHz.

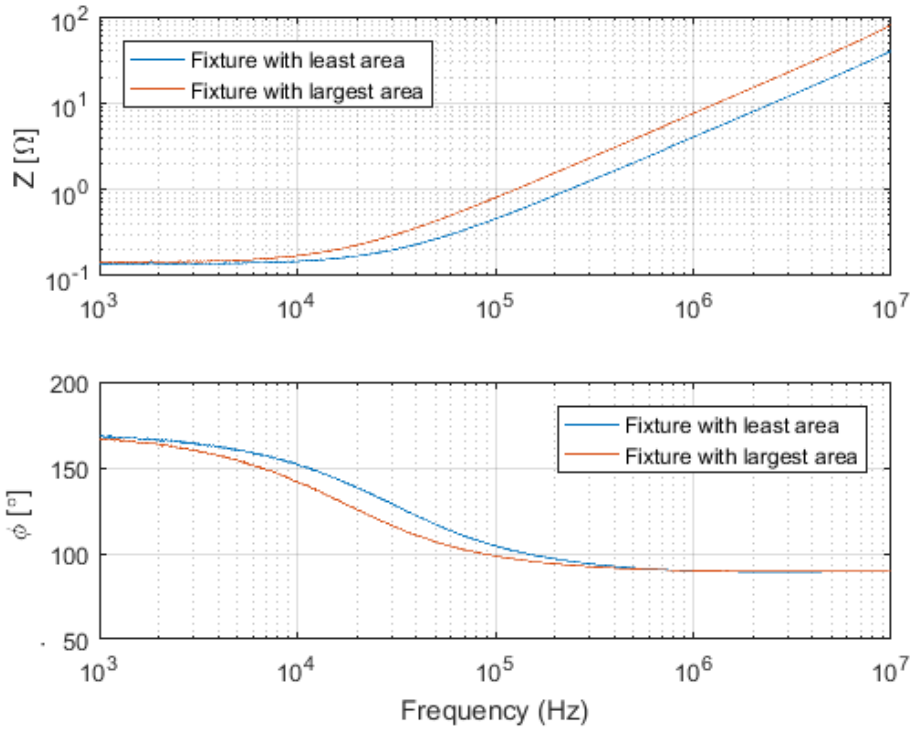
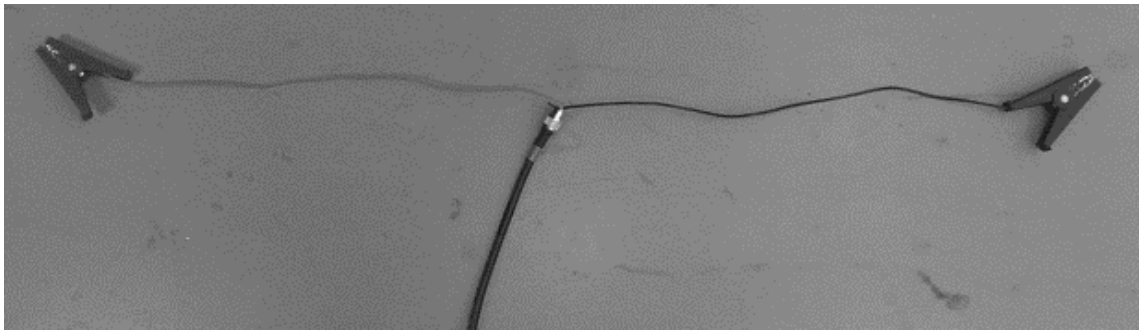


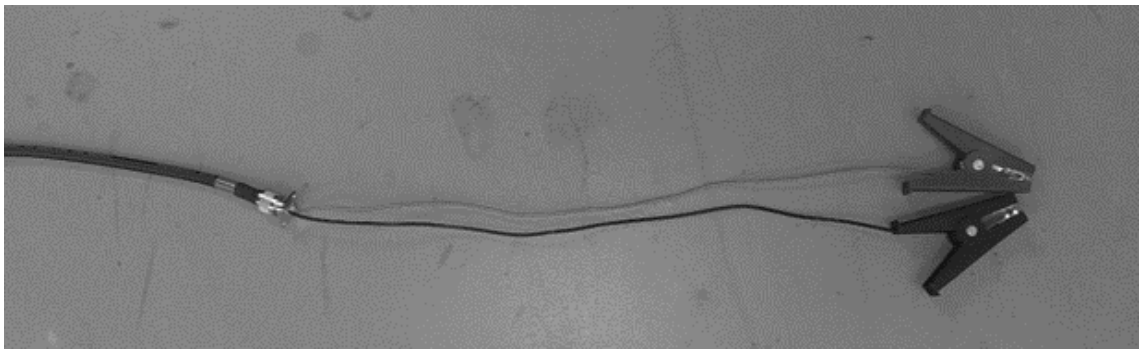
Fig. 3.33: Dependency of the impedance of the fixture on its position

Each measurement was performed for both wires separately as shown in Fig. 3.34. The first wire is measured from connection 1 to clamp 1 and the second one is measured from connection 2 to clamp 2. The orange line is the result of the impedance measurement for the fixture configured as depicted in Fig. 3.35a for one wire and the blue line represents the outcome for the position shown in Fig. 3.35b for the same wire. Both cables show the same behavior. Therefore, only one of them is shown in Fig. 3.33.

Fig. 3.34: Representation of the fixure hardware and its measurement points



(a)



(b)

Fig. 3.35: Two extreme positions of the fixture [75]: (a) Clamps of the fixture distant as far as possible, (b) Clamps of the fixture located as close as possible

The resulting impedance changes for both depict physical positions of the connection clamps as proposed in [75]. The author of [69] describes the impact of the fixture on the impedance of a DUT as a root cause of the occurring resonance frequencies above 5 MHz. This is one feature of the presented bode plots of the coupled inductor and the capacitor in Chapter 4. In other words, this feature is due to the inductance exhibited by the fixture that was used to connect the VNA to the measurement points of the examined power system components. The measurements of the fixture leads to the additional serial inductance of the fixture, which is between 630 nH and 1.2 μH depending on the configuration of its wires. The rising deviation between the equivalent circuits of included components and the performed measurements at frequencies over 1 MHz is also likely to be caused by the increasing impact of the fixtures inductance and consequently no effect of the examined components characteristics.

A further reason, why the fixtures influence is significant in a high frequency spectrum is that its impedance increases considerably. At 1 MHz the fixture shows an impedance between 4 Ω and 7.6 Ω depending on its position, while it increased to 40 Ω or 80 Ω at a frequency of 10 MHz respectively. Furthermore, its effect can not be predicted in an accurate way, because it depends on the physical setup of the fixture as described in [76].

4 Measurements of the Power Electronic Building Block

4.1 Power Electronic Building Block

The PEBB is one of three parts of a medium voltage impedance measurement unit (IMU) designed by the Center for Power Electronics (CPES) at Virginia Tech (VT). The concept enables great scalability and modularity, which allows numerous power conversion topologies. The unit is shown in Fig. 4.1 and its topology with the rated nominal input and output voltage is depicted in Fig. 4.2. The PEBB used in the IMU includes two 10 kV, 120 A SiC MOSFET phase-leg modules in H-bridge configuration [77,78], gate drives, four times two DC-link capacitors in parallel rated for 5 kV with a value of 900 μF each, 700 nF snubber capacitors parallel to each SiC MOSFET and a 2.4 mH coupled inductor. The unit comprises a high-speed digital controller, an uninterruptible power supply and liquid cooling for the H-bridge and a protection IGBT. Each leg of the SiC H-bridge operates at a switching frequency of 10 kHz.

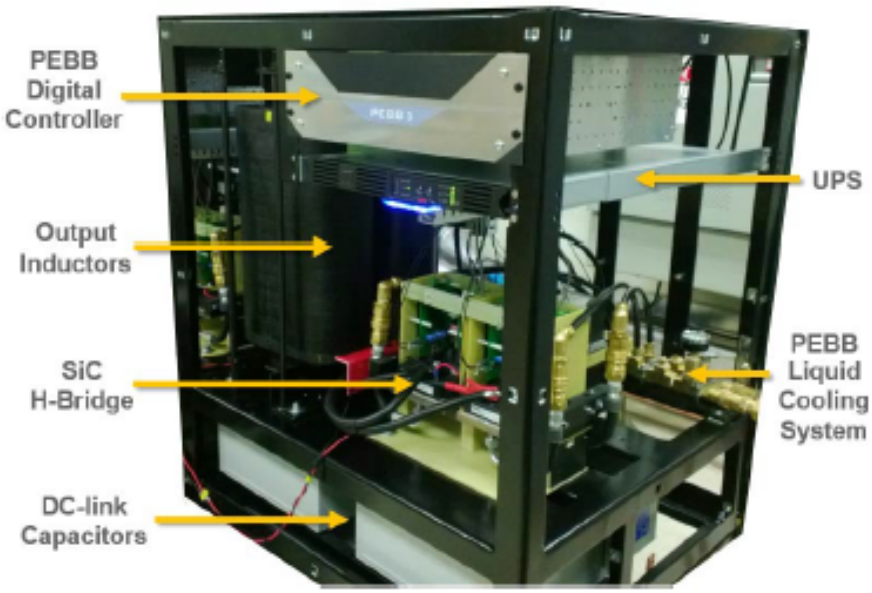


Fig. 4.1: Hardware Implementation of the PEBB [79]

For the performed measurements the IGBT was removed from the system, due to the

voltage range of the tests was considered safe for all implied devices. Apart from that, all but two DC-link capacitors were disconnected, which resulted in a capacitance of 450 μF at the input side. The removal of these parts served to reduce the involved components of the circuit, to gain a more accurate idea of how the inverter impacts the CM behavior.

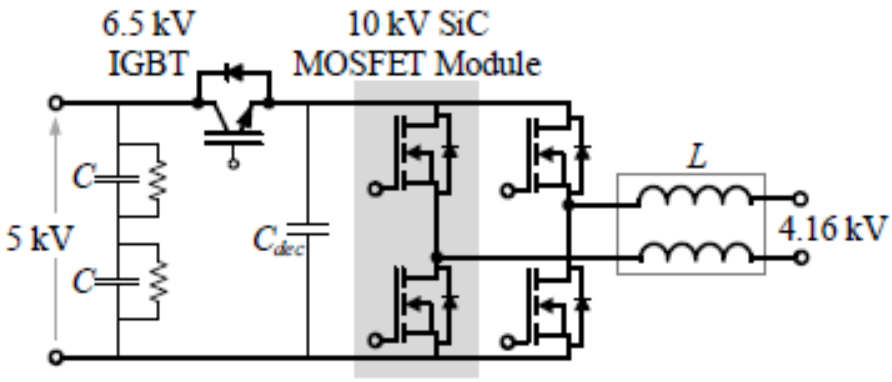


Fig. 4.2: Structure and Topology of the PEBB [79]

The physical structure of the H-bridge can be seen in Fig. 4.3.

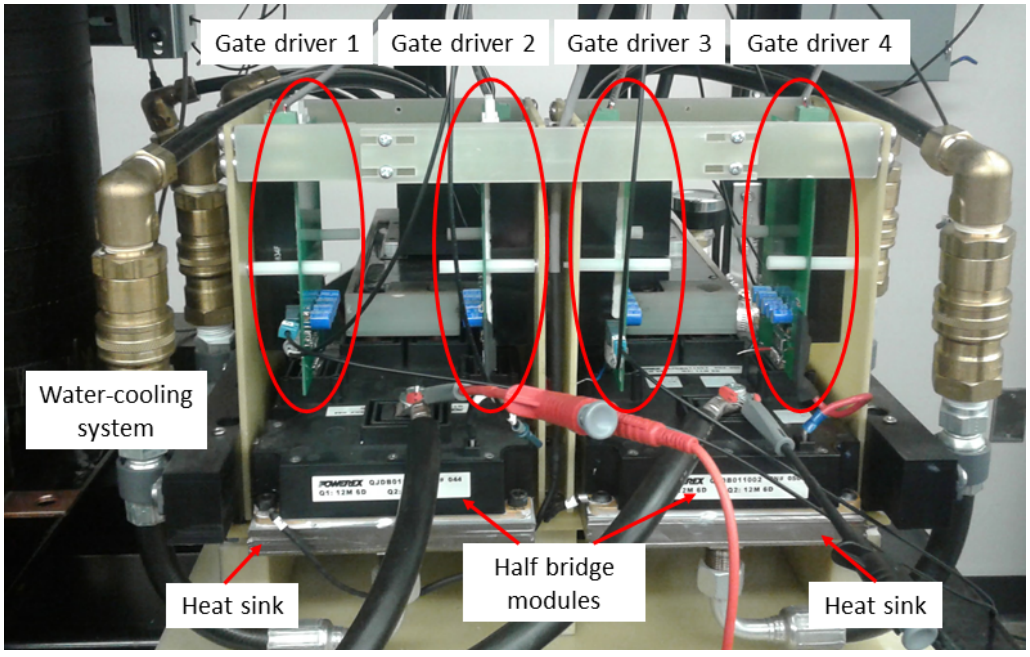


Fig. 4.3: H-bridge hardware setting

In the following sections, the given parameters of the components are validated by impedance and scattering-parameter (S-parameter) measurements. Both were performed with a vector network analyzer (VNA), an Agilent E5061B.

4.2 Circuit and Components

The device of interest involves two DC-link capacitors at the DC side and a serial parasitic inductance caused by the low inductive plate, which connects the capacitors with the H-bridge. The tested inverter includes two SiC MOSFET half bridge modules and a parallel snubber capacitor to each switching device. The inverter includes a free wheeling diode for each MOSFET. The AC side of the circuit contains a coupled inductor, shown in Fig. 4.2. For active measurements of the PEBB, a pure resistive load with 100 Ω was connected to the AC side. A DC power source, two BK Precision (power source brand) in series connection in master-slave configuration, was connected to the DC side. The series connection of the two sources was necessary, due to one of these devices is limited to a maximum voltage output of 80 V. The values of each of these components are the same as used for the simulation as shown in Table 3.1.

4.2.1 Preparation of the Circuit

For the de-energized measurements, all components had to be separated form each other. Therefore, the DC-link capacitors were disconnected and shortened. The connection cables between the SiC MOSFET half bridges and the coupled inductor were removed. When it comes to energized measurements, the PEBB will be powered with low voltage between 10 V and 160 V. For this voltage domain, which is considered save for all involved components, the IGBT was also removed, which was used as protection for the transistors, plus it would represent an additional source of CM noise and would add parasitic elements to the circuit. Its connection points on the low inductive glass plate were shortened with a copper strip. Moreover, each MOSFET receives its switching signal directly from the master control unit in order to prevent any influence of the included control unit of the PEBB. The whole hardware setup can be seen in Fig. 4.4, which shows the energized measurement of the CM voltage of the PEBB, described in detail in Section 4.4.3.

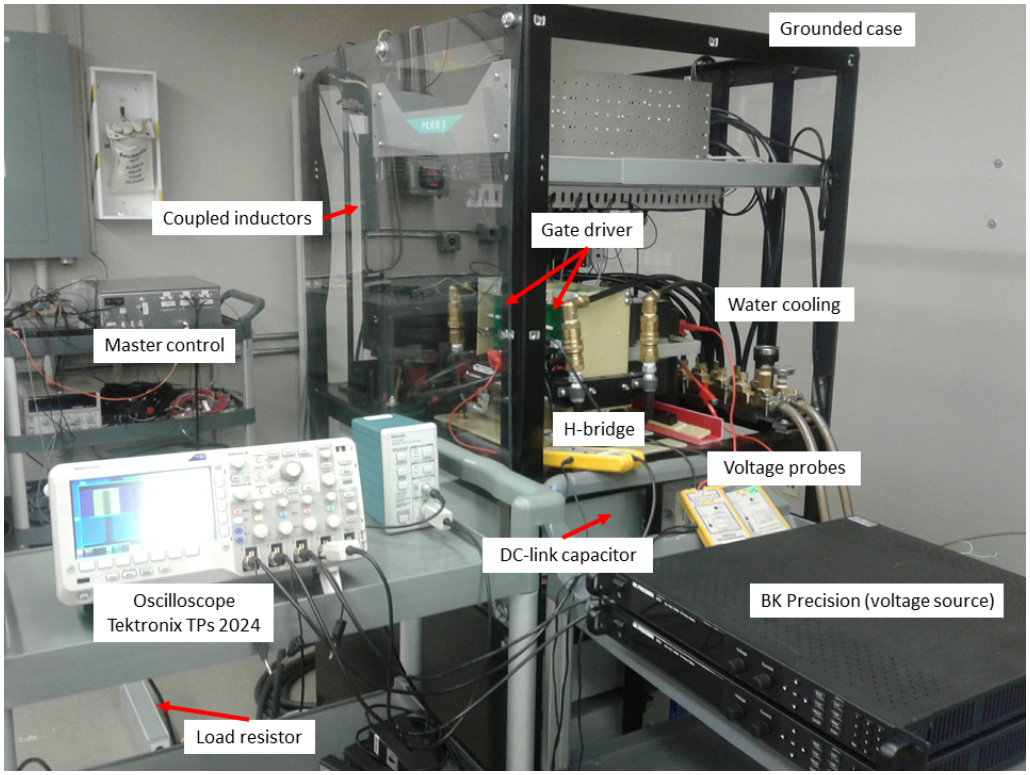


Fig. 4.4: Hardware setting

4.3 De-Energized Measurements

Most of the de-energized measurements were already presented earlier in this thesis in Section 3.2.1 and Section 3.4. Only a few more details will be discussed in this section, such as the mutual inductance of the coupled inductor, the snubber capacitors and the SiC MOSFETs.

4.3.1 Coupled Inductor

The measurements of the parasitic capacitance to ground of the coupled inductor (Section 3.2.1) and an impedance measurement if its overall inductance (Section 3.4) was already presented. A further measurement with was performed to gain more information of the component, an impedance measurement of each coil. In combination with the impedance measurement of the coupled inductor with tied ends, it is also possible to calculate the mutual inductance. The measurement can be seen in Fig. 4.5.

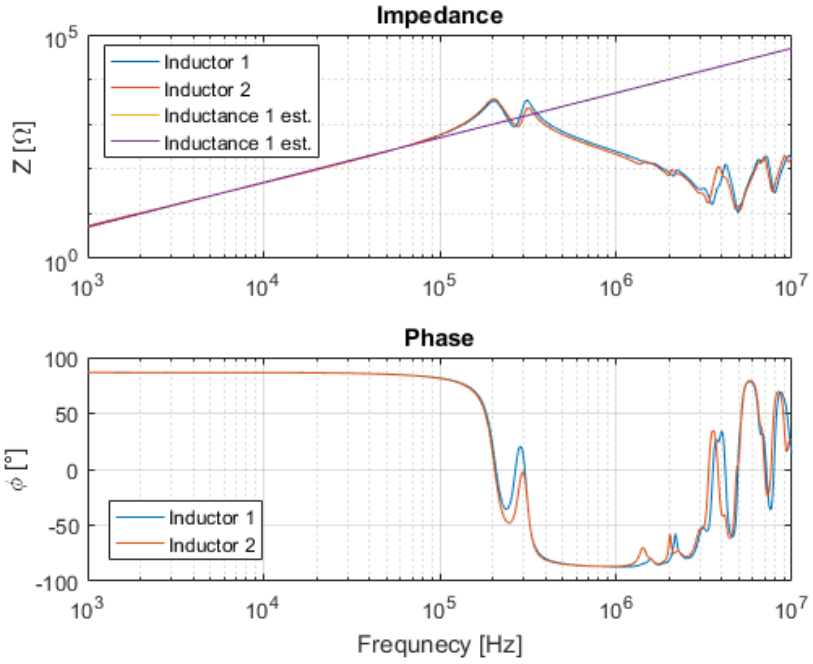


Fig. 4.5: Impedance measurement for each coil of the coupled inductor and estimated inductance

The resulting inductances for each coil and included mutual inductance are $L_a = 768.3\ \mu$H and $L_b = 768.2\ \mu$H. The estimated total inductance of the device is 2201.5 μH. With the following equation for couped inductors, it is possible to calculate the mutual inductance [80].

$$L_{tot} = L_1 + L_2 + 4L_m \tag{4.1}$$

This equation is valid for two coupled inductances measured in series. Furthermore, to calculate the inductance of each coil (i.e. L_1 and L_2) and the mutual inductance L_m, the following equations are needed.

$$L_a = L_1 + L_m \tag{4.2}$$

$$L_b = L_2 + L_m \tag{4.3}$$

From Equation 4.2 follows

$$L_m = L_a - L_1 \tag{4.4}$$

By inserting this result into Equation 4.3 one obtains for L_2

$$L_b = L_2 + (L_a - L_1) \longrightarrow L_2 = L_b - L_a + L_1 \tag{4.5}$$

but since the measurement result for L_a is roughly the same as for L_b, the approximation

$L_2 = L_1$ is used. For Equation 4.1 follows:

$$L_{tot} = L_1 + L_1 + 4(L_a - L_1) = 4L_a - 2L_1 \tag{4.6}$$

By rearranging this formula, the inductance L_1 can be calculated.

$$L_1 = \frac{1}{2}\big(4L_a - L_{tot}\big) = \frac{1}{2}\big(4 \cdot 768\ \mu\text{H} - 2201\ \mu\text{H}\big) = 435\ \mu\text{H} \tag{4.7}$$

The impedance L_2 also results in 435 μH and the mutual inductance $L_m = 332\ \mu$H. This values for L_1, L_2 and L_m were used in the simulation. The equivalent circuit is shown in Fig. 4.6.

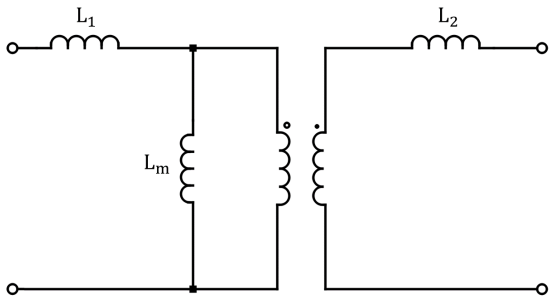


Fig. 4.6: Equivalent circuit of the coupled inductor

The two coils in the middle of the circuit represents the 1:1 coupling between both inductors.

4.3.2 Snubber Capacitors

The value of each snubber capacitor of 700 nF is known due to available information of the PEBB. To confirm their size, take any deviations into consideration and to determine any parasitic coupling to ground, measurements of these capacitors would have been necessary. This was not possible, due to the hardware setup, since the snubber capacitors are directly connected between the low inductive plate and the two half-bridges. It was assumed that the impact of these devices can be neglected, because of the much larger DC-link capacitor values.

4.3.3 Silicon Carbide MOSFETs

A measurement of the impedance or an S-parameter measurement could not be performed on the SiC MOSFETs, because of the hardware setup. Therefore, the determined parasitic capacitances of the switching devices over its heat sink to ground of previous performed

measurements was used as described in Section 3.2.1.

For an S-parameter measurement of the H-bridge one would have to disconnect the low inductive plate at the DC-side of the system and the XPLE connection cables to the coupled inductor. By doing so each half-bridge would be separated from the PEBB and an two-port S-parameter measurement against ground could be performed for the input and for the output side. To avoid any influence of the system one should also disconnect the gate drivers. This measurement could provide a better insight into the inverters parasitic coupling effects.

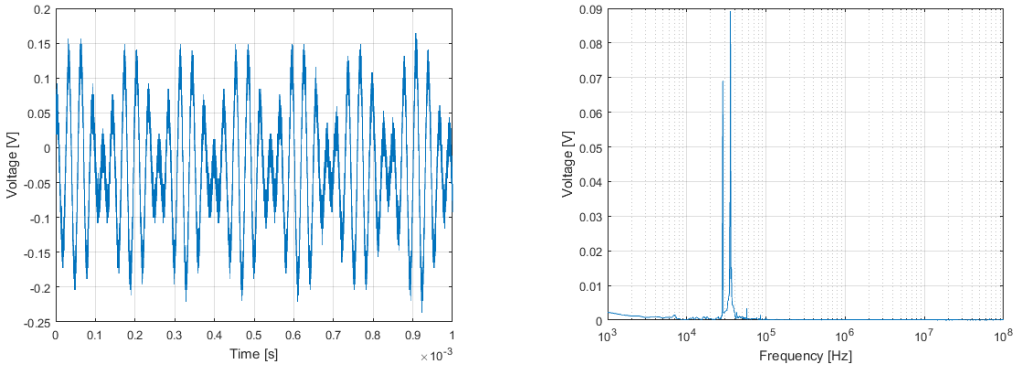
4.4 Energized Measurements

For the energized measurements the following voltages were used as DC supply voltage: 10 V, 50 V, 80 V, 120 V and 160 V. For each of these voltages the CM voltage and the CM current was measured. The input and output voltage and current was measured up to a supply voltage of 80 V.

4.4.1 Power Source

For the first scrutiny measurements the AE Techron TEC3622 was used and directly connected to the H-bridge. The four gates of the inverter were powered by the PEBB power supply. The activation of the switching pattern was controlled by the master controller through fiber, operated over an Ethernet connection and the provisioned control software of the IMU. The output of the two half-bridges was captured with the Tektronix DPO 2014B oscilloscope and a voltage probe. During these measurements there was nothing connected to the load side of the inverter (i.e. coupled inductor and resistive load).

When the gates of the MOSFETs were powered, the switching algorithm was turned off and the power source was in standby (i.e. no voltage output), a 200 mV noise signal was observed at the AC side of the bridge with two dominant frequencies 28.5 kHz and at 35 kHz. Different grounding methods of the source were tested, in order to reduce or eliminate this noise, e.g grounding of the negative rail and grounding the chassis of the source, but the noise persisted. It was assumed that the source itself was the cause of this disturbance, possibly creating a resonance within the circuit. Therefore, another power supply of the same type was tested with the same result. The captured noise measurement and its frequency analysis are shown in Fig. 4.7a and Fig. 4.7b.



(a) Noise signal on the AC side of the inverter (b) Frequency analysis of the noise signal

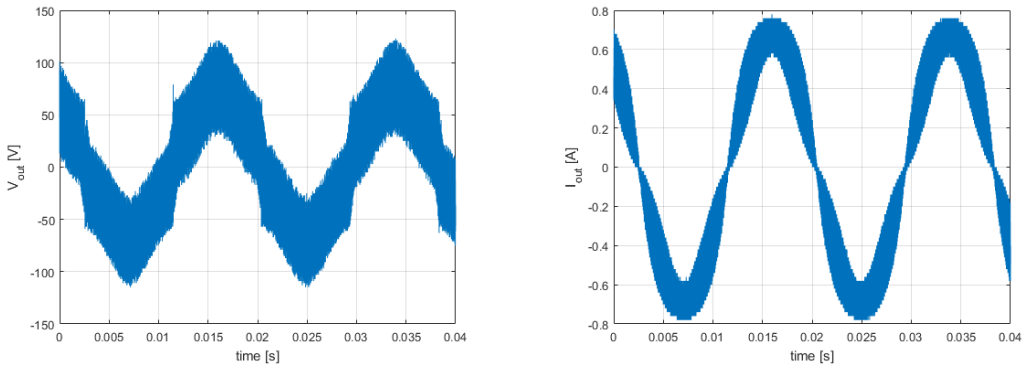
Fig. 4.7: Noise signal cause by the power source AE Techron TEC3622

After this test the power source was switched to a BK Precision. Using this device the noise signal was eliminated and therefore this change confirmed the assumption that the AE Techron TEC3622 itself causes the observed noise signal. For this purpose all further studies were performed using a BK Precision for voltages below 80 V and two BK Precision power sources in series in master-slave configuration for higher voltages. The series connection was needed, due to one of these devices has a output limitation of 80 V.

It is assumed, that the observed signal outcome while using the AE Techron is a cause of the capacitive load (i.e. DC-link capacitor) of the power supply. This is because the possibility that the implemented control circuit of the source cannot handle the high capacitance, especially during open circuit operations.

4.4.2 Input and Output Quantities

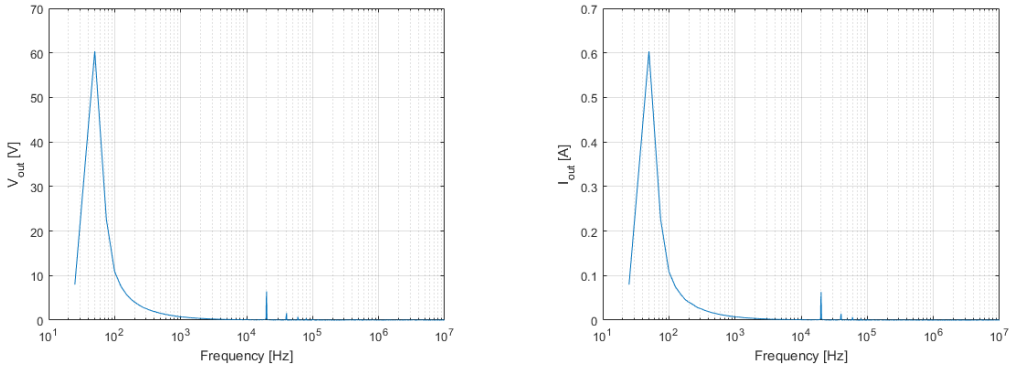
Both, the input and output quantities were measured for a supply voltage of 10 V, 50 V and 80 V, but the focus lies on the measurement and identification of the CM behavior. Therefore, only one example of these quantities for an input voltage of 80 V will be shown. For this supply an input current of $I_{in} = 350$ mA was measured. The output quantities are shown in Fig. 4.8.



(a) Output voltage V_{out} (b) Output current I_{out}

Fig. 4.8: Output quantities for 80 V supply voltage

As can be seen, both, the output voltage and output current exhibit multiple higher order frequencies. An FFT of the captured signals shows that the main intensity is at 60 Hz, which is the wanted output frequency and further low intensity peaks at 20 kHz and its multiples. This can be seen in Fig. 4.9.



(a) Frequency analysis of the output voltage V_{out} (b) Frequency analysis of the output current I_{out}

Fig. 4.9: Frequency analysis of the output quantities for 80 V supply voltage

The peaks at 20 kHz are seen since each half bridge is controlled by its own carrier. The two carrier signals are shifted by 180 degrees. In earlier measurements which were performed before this project, it was already observed that 20 kHz occur in the output signal of the PEBB. This measurement was only performed as a control measure and optimal output quantities are not required in order to measure and characterize the CM behavior of the inverter. Therefore, no further investigations or optimizations were performed.

4.4.3 Common-Mode Voltage

The CM voltage was identified by capturing the voltage of the positive and the negative rail of the DC side (point p and n in Fig. 4.10) in front of the inverter against rail b of the AC side between the inverter and the coupled inductor. Moreover, the voltage between both rails (point a and b in Fig. 4.10) of the AC side was measured. In other words, rail b was chosen as the arbitrary reference point to obtain all needed voltages to calculate the resulting CM voltage of the switching device.

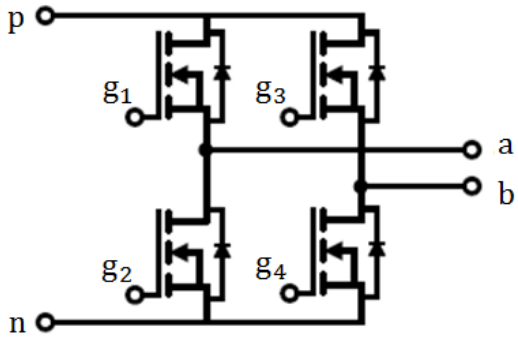
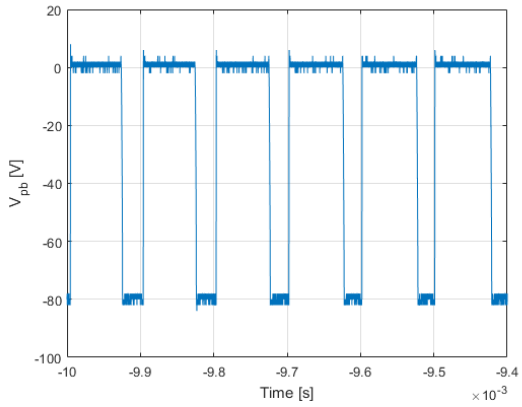


Fig. 4.10: Voltage measurement points of the inverter

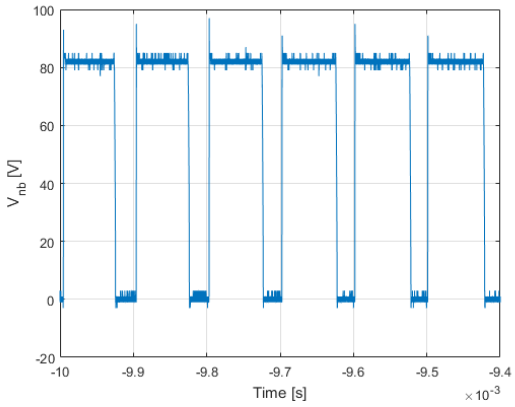
The following equation was used to calculate the CM voltage of the system with the captured voltages:

$$V_{CM} = \frac{V_{pb} + V_{nb}}{2} - \frac{V_{ab}}{2} \tag{4.8}$$

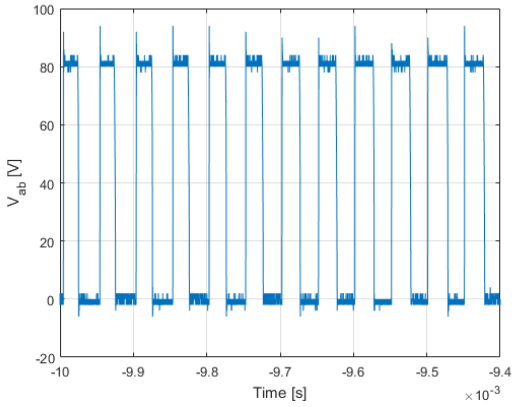
This conforms to the definition of the CM voltage given in Chapter 2. As an example, each of the captured voltages can be seen in Fig. 4.11 for a supply voltage of 80 V. The resulting CM voltage is shown in Fig. 4.12.



(a) V_{pb}

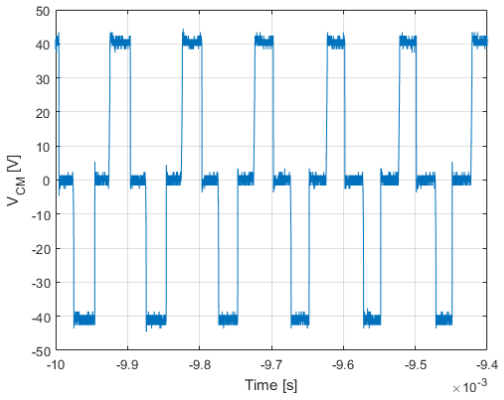


(b) V_{nb}

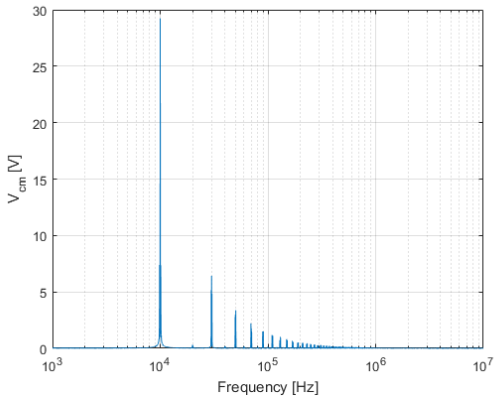


(c) V_{ab}

Fig. 4.11: Measurements of all voltages included in the CM voltage calculation: (a) Voltage between the positive rail and rail b, (b) Voltage between the negative rail and rail b, (c) Voltage between the rail a and rail b



(a)

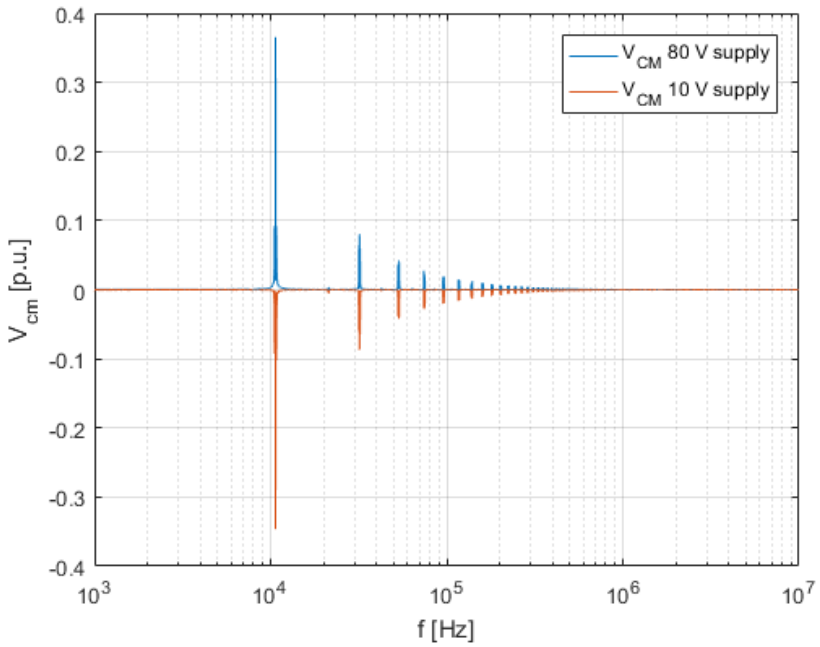


(b)

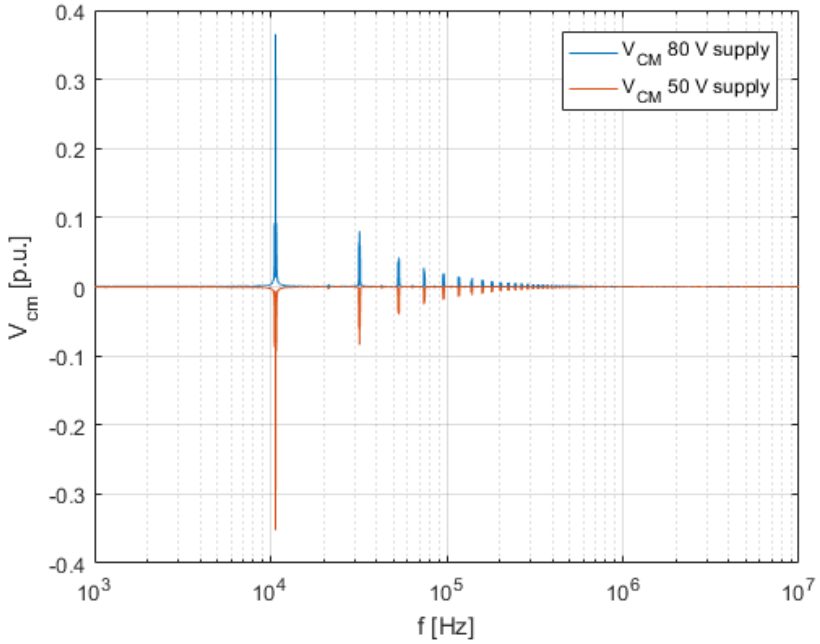
Fig. 4.12: CM voltage for 80 V supply voltage: (a) time domain plot of the CM voltage, (b) frequency analysis of the CM voltage

It was assumed that the resulting time domain maxima of the CM voltage will be in the range of half the applied voltage. As can be seen, this conjecture is valid for the outcome of the processed measurements and also confirms the correctness of the calculation. Furthermore, the frequency analysis illustrated in Fig. 4.12b shows the CM voltage intensity peaks at the switching frequency of the MOSFETs of 10 kHz and its odd harmonics. There are also very small peaks at 20 kHz and its multiples. This is caused, due to each half bridge controlled by its own carrier signal shifted by 180 degrees. The measurements taken at other supply voltages are shown in Chapter 12.

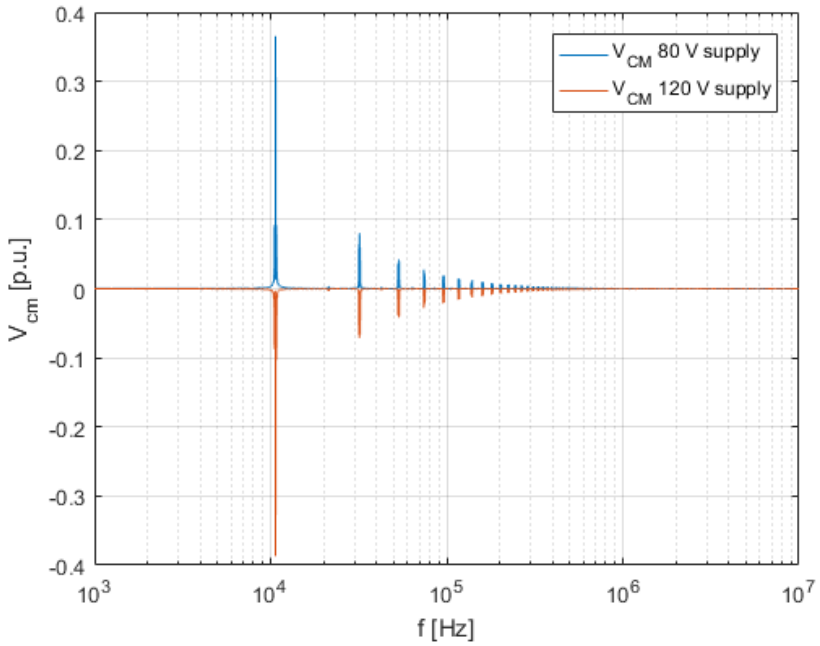
An FFT of the normalized CM voltage for all five different supply voltages can be seen in Fig. 4.13. All measurements were compared to the outcome with 80 V.



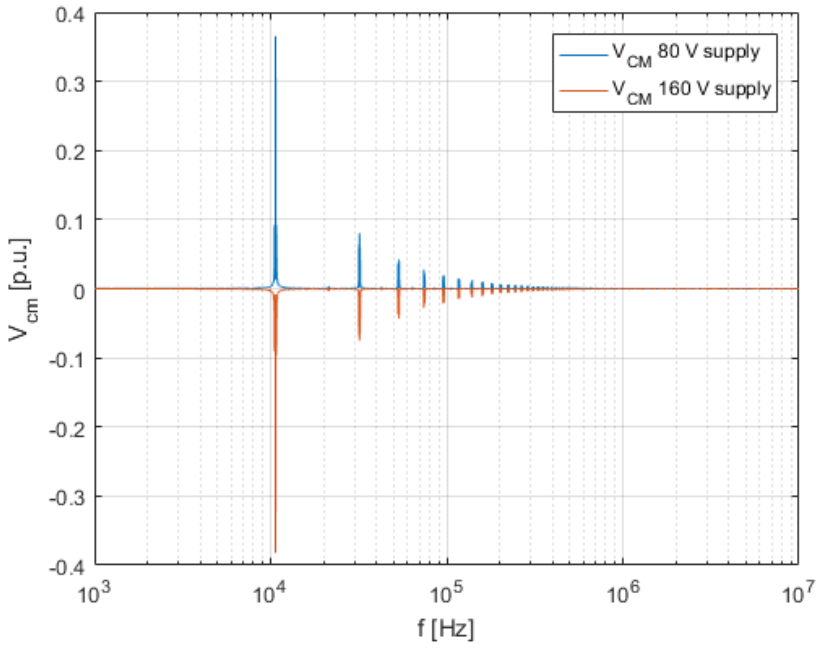
(a) Comparison of 10 V with 80 V supply voltage



(b) Comparison of 50 V with 80 V supply voltage



(c) Comparison of 120 V with 80 V supply voltage



(d) Comparison of 160 V with 80 V supply voltage

Fig. 4.13: Comparison of the frequency analysis of the measured and normalized CM voltage for different supply voltages with the result of 80 V supply voltage as reference: (a) Comparison of 10 V against 80 V with voltage, (b) Comparison of 50 V with 80 V supply voltage, (c) Comparison of 120 V with 80 V supply voltage, (d) Comparison of 160 V with 80 V supply voltage

By analyzing these five measurements, one characteristic of the CM voltage could be confirmed. It is linear dependent on the supply voltage. This can be seen in Fig. 4.14.

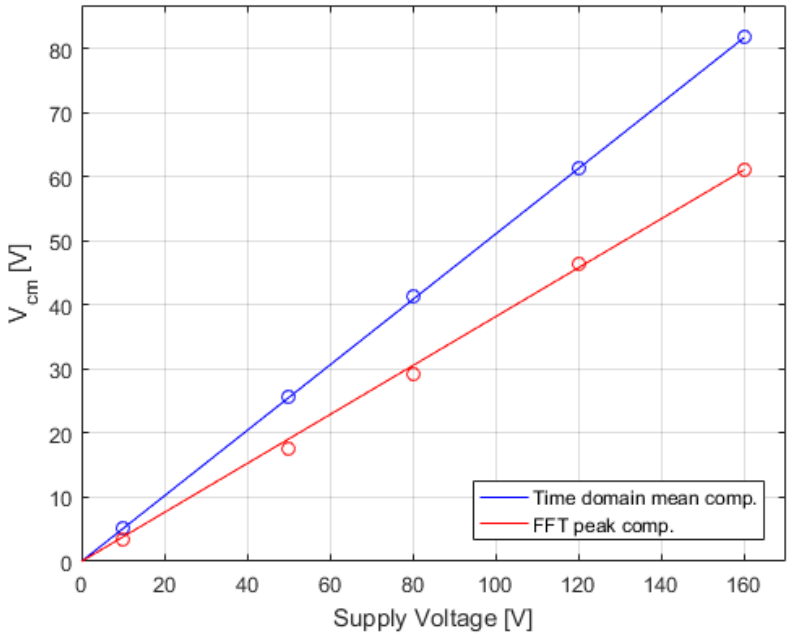


Fig. 4.14: Dependency of the CM voltage on the supply voltage

Two different methods were used to analyze the CM voltage for its linearity. The first one was to calculate the mean of all occurring maxima in the time domain signal for each measurement (blue line). The second method was to compare the intensity peak at 10 kHz (amplitude of the 10 kHz component) of the frequency analysis (red line). As can be seen, in both cases the dependency of the CM voltage on the applied voltage can be considered linear.

4.5 Common-Mode Current

It is possible to measure the CM current of the inverter directly, by measuring both, the current of the positive and the negative rail of the DC side to the bridge and both rails of the AC side in front of the coupled inductor, which follows the definition of CM current from Chapter 2. The measurement on the DC side in front of the two half-bridges of the PEBB could not be performed, due to the hardware structure. A current measurement at that side was not possible, because of the low inductive plate, which directly connects the DC-link capacitors to the input of the H-bridge. Therefore, a correct measurement of the common-mode current on the DC side could not be performed and the CM current of the H-bridge could not be measured directly. If the current measurements could have been performed on both sides of the inverter, a combination of the currents would have lead to the parasitic current, which uses the parasitic capacitance of the MOSFETs heat sink to ground as path.

However, the measurement of at the AC side could be performed. Two different measurement setups were used. First of all, the original XPLE connection cables between each half-bridge and the coupled inductor were used. In this case, two separate high current bandwidth probes had to be used to measure the current of each rail, since the combination of the two wires exceeded the gauge limitation of the current probe. Both probes were Tektronix TCP303 AC/DC high bandwidth current probes, and the Tektronix TCPA300 probe amplifier. The hardware is shown in Fig. 4.15. If the CM currents are measured with two separate probes, one has to take care that both are measured in the same direction, because the resulting signal data requires an additional processing, since the CM current is the sum of all currents through the connected wires as shown in the definition in Fig. 2.1.

Fig. 4.15: Tektronix high current bandwidth probe

For the second setup the XPLE cables were replaced with a common copper wire with two mm in diameter. In this way, it was possible to measure the CM current directly with one current probe. An extract of both time domain signal results can be seen in Fig. 4.16.

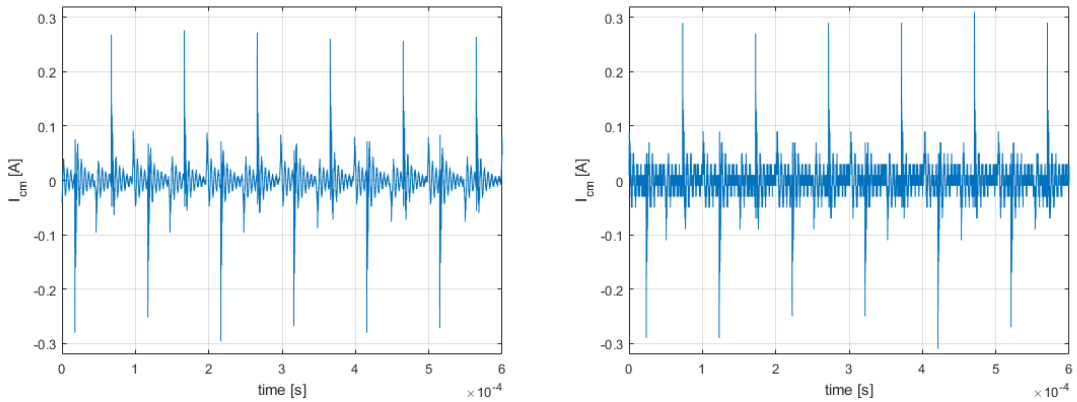


Fig. 4.16: Time domain comparison of the measured CM current: (a) Measurements with copper cable, (b) Measurement with XPLE cable

For a better analysis and a direct comparison the frequency domain plot of both, the measurement setup with the XPLE cables and with the copper cables, can be seen in Fig. 4.17. The for the FFT used time domain signals had a length of 40 ms and a time resolution of 10 ns.

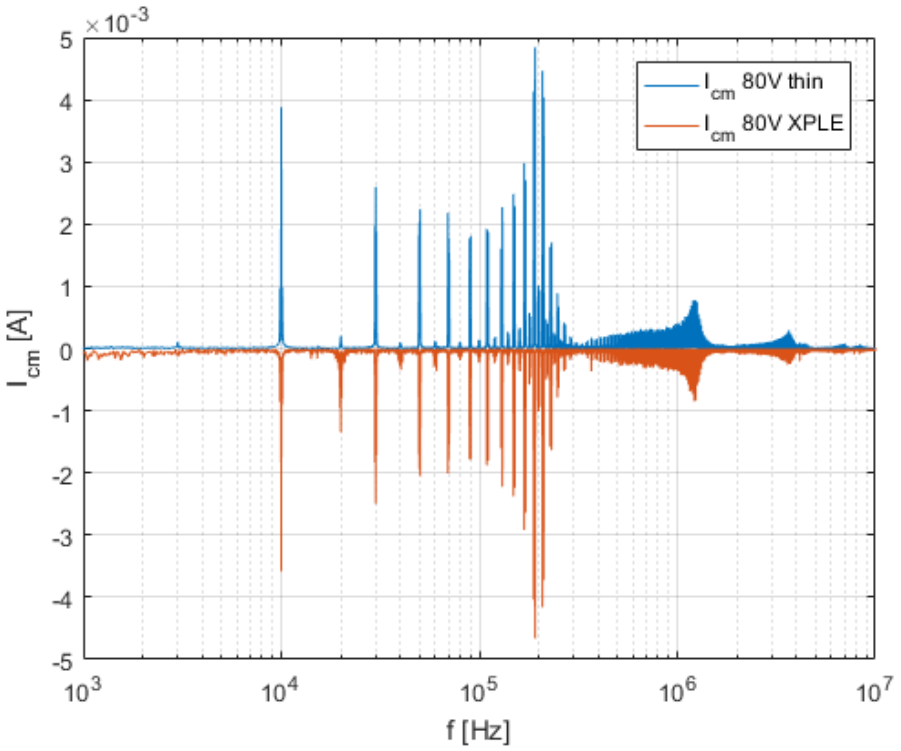


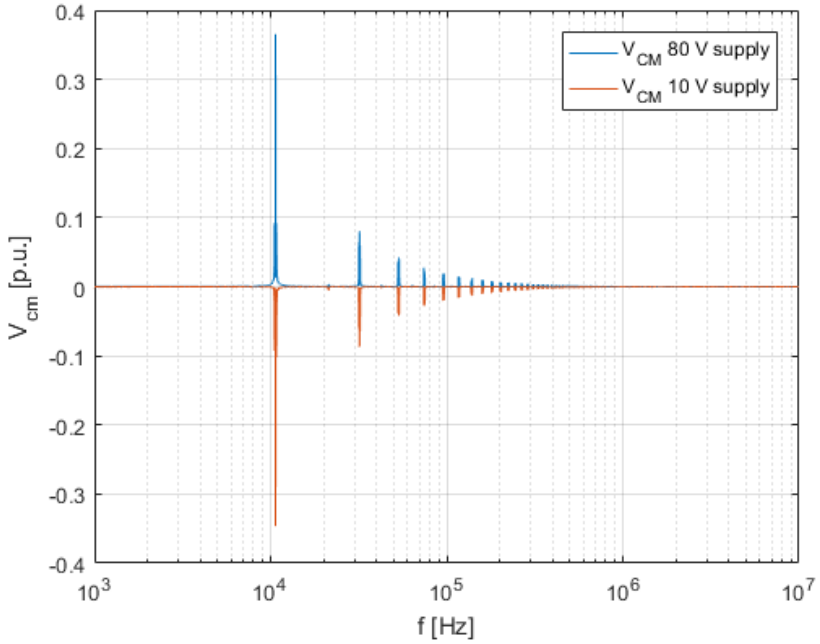
Fig. 4.17: Comparison of the CM current of both cable setups for 80 V supply voltage

As can be seen, the measurement with the XPLE cables shows higher intensity peaks at 20 kHz and its harmonics in comparison with the measurement with the common copper wires, which also results in a divergence in the intensity peaks. It is assumed that this was caused by the process of data saving and processing, since this can result in numerical differences. This effect can be seen, when the time domain plots in Fig. 4.16 are compared. While the CM current for the measurement with the copper cable setup shows a clear waveform, the result of the measurement with the XPLE cable setup presents more harmonic content. If the CM voltage is taken into consideration, it suggests that the measurement with the thin copper cables is more accurate, because the captured CM voltage shows only very low intensity peaks at 20 kHz and its multiples. However, both measurements show similar peaks at the switching frequency of 10 kHz and its odd harmonics and both exhibit the main intensity peak at a frequency of 191 kHz. Everything above 320 kHz is considered as noise.

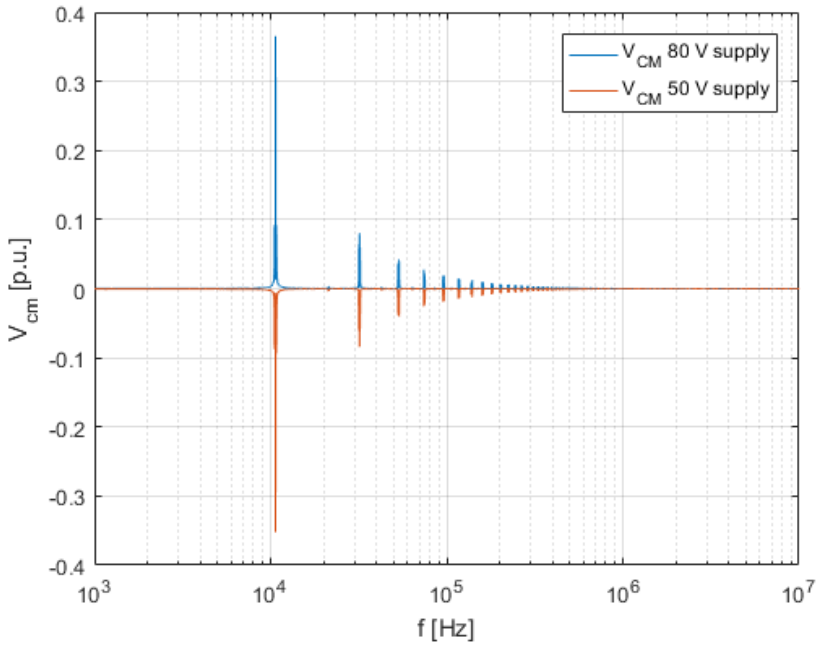
The resulting CM current for all five applied supply voltages between 10 V and 160 V for the measurements under use of the copper cables can be seen in Fig. 4.18, while Fig. 4.19 depicts the captured CM current for the measurement configuration with XPLE cables. All currents are normalized. For the normalization the measured input current was used. These values are listed in table **??**

Supply voltage [V]	10	50	80	120	160
Input current [mA]	45	220	350	500	700

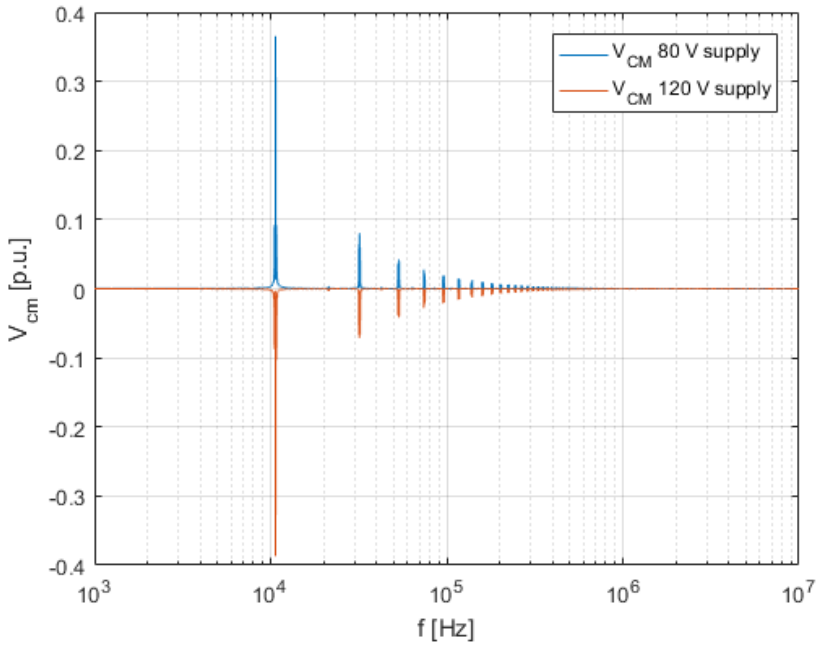
Table 4.1: Measured input currents for each supply voltage



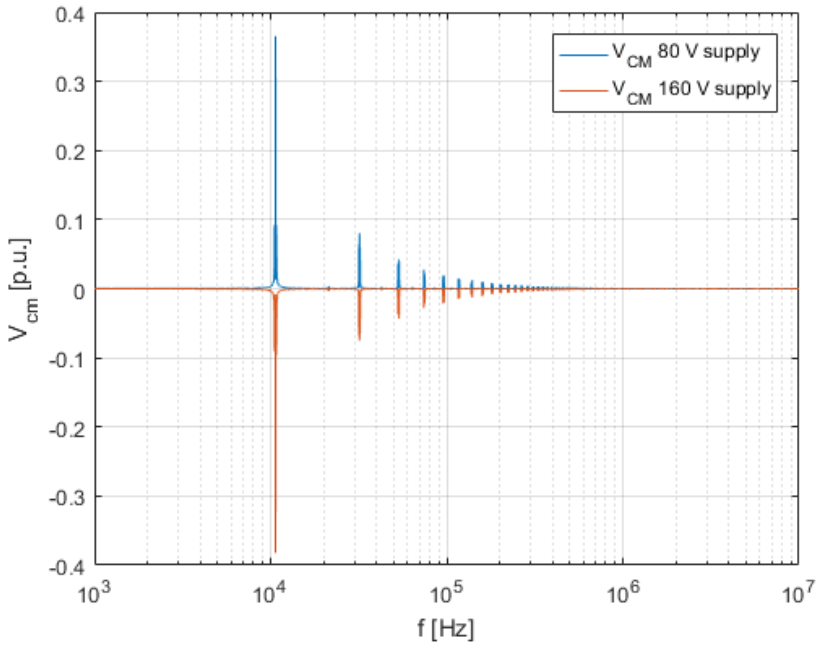
(a) Comparison of 10 V with 80 V supply voltage



(b) Comparison of 50 V with 80 V supply voltage

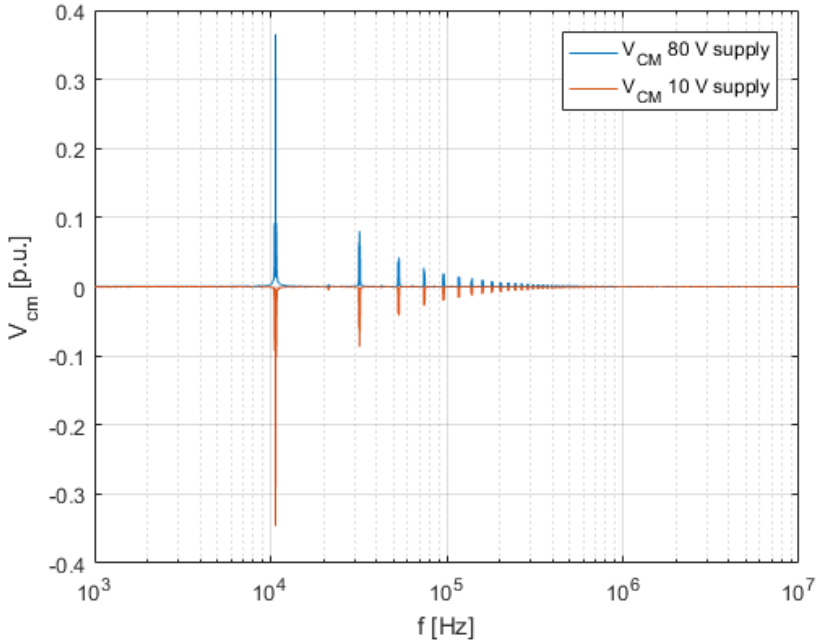


(c) Comparison of 120 V with 80 V supply voltage

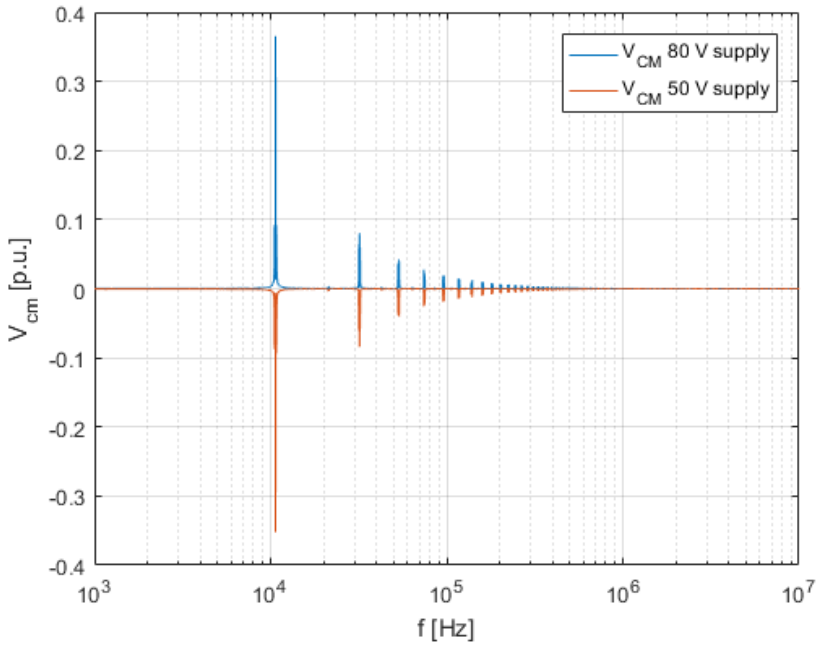


(d) Comparison of 160 V with 80 V supply voltage

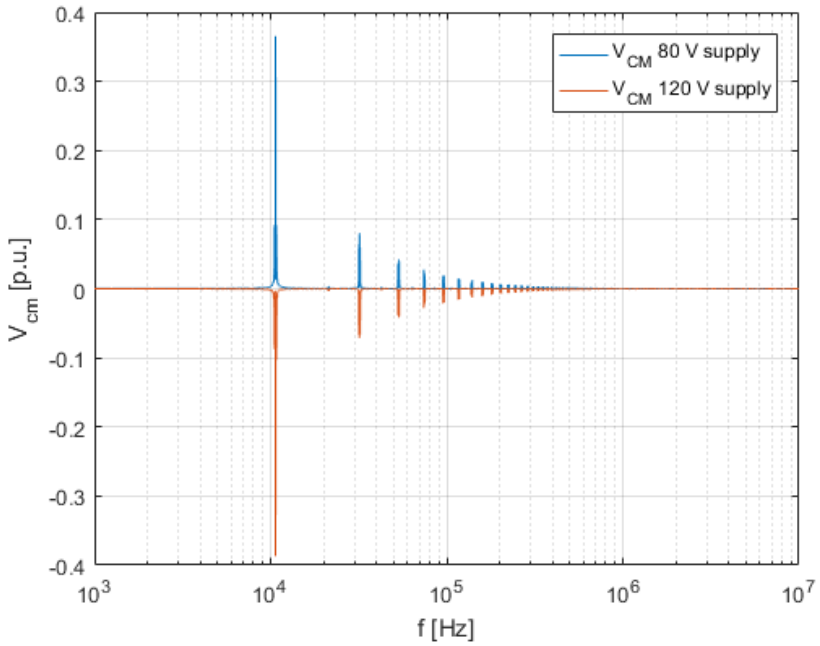
Fig. 4.18: Comparison of the frequency analysis of the measured and normalized CM current with copper cable setup for different supply voltages with the result of 80 V supply voltage as reference: (a) Comparison of 10 V against 80 V with voltage, (b) Comparison of 50 V with 80 V supply voltage, (c) Comparison of 120 V with 80 V supply voltage, (d) Comparison of 160 V with 80 V supply voltage



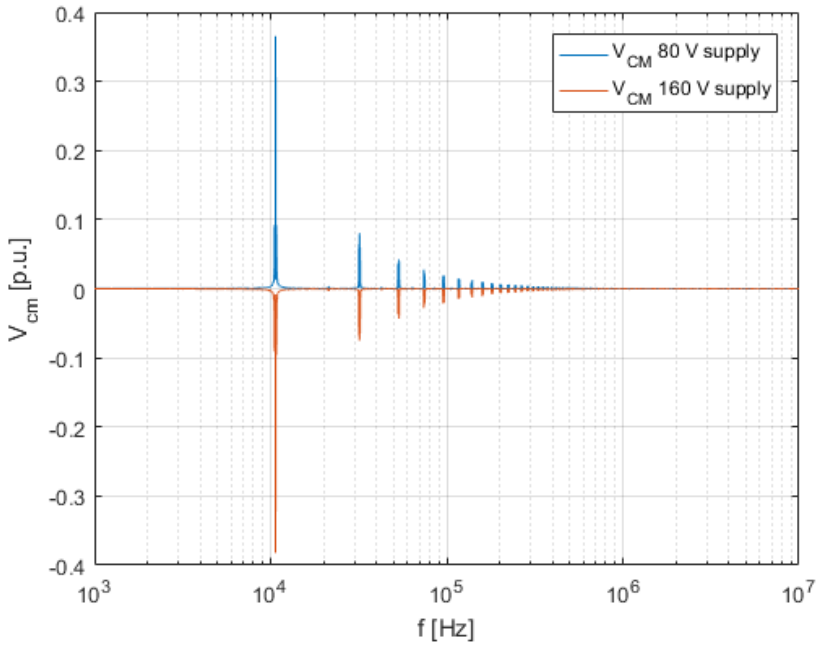
(a) Comparison of 10 V with 80 V supply voltage



(b) Comparison of 50 V with 80 V supply voltage



(c) Comparison of 120 V with 80 V supply voltage



(d) Comparison of 160 V with 80 V supply voltage

Fig. 4.19: Comparison of the frequency analysis of the measured and normalized CM current with XPLE cable setup for different supply voltages with the result of 80 V supply voltage as reference: (a) Comparison of 10 V against 80 V with voltage, (b) Comparison of 50 V with 80 V supply voltage, (c) Comparison of 120 V with 80 V supply voltage, (d) Comparison of 160 V with 80 V supply voltage

To investigate the dependency of the parasitic current on the applied voltage, the main intensity peak at 191 kHz was captured for each performed measurement. The result for both measurement setups can be seen in Fig. 4.20. For the proof of linearity of the two configurations, which is shown in that figure, the intensity peak at 10 kHz of each measurement (amplitude of the 10 kHz component) was used.

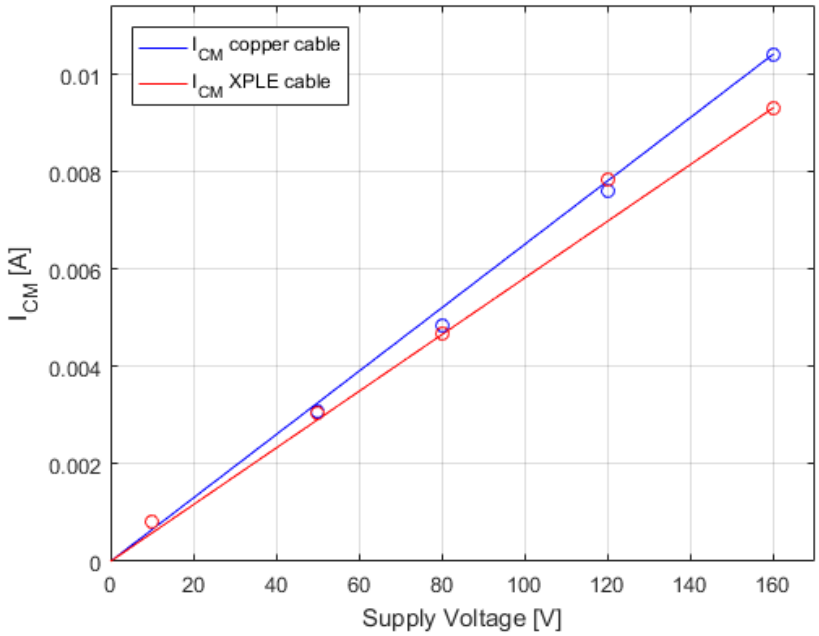


Fig. 4.20: Dependency of the CM current for different supply voltages

The reason that the measurements for setup with XPLE cables exhibit a lower intensity has already been explained. As can be seen, the CM current can be seen as linear similar to the dependency of the CM voltage. It is not clear why there is an outlier for the measurement with XPLE cables at a supply voltage of 120 V, but it is assumed that a repetition of the measurement would result in a better match and less deviation to the expected linear increasing value.

5 Validation

The following chapter provides validation of both, the MM and the CM model, comparing the simulation and measurement results.

5.1 Mixed-Mode Model

First of all the MM model is evaluated, since its CM voltage was used as source for the CM model. Thus, the CM behavior of the simulation model is compared to the outcome of the measurements. A direct comparison of the resulting CM voltage for a supply voltage of 80 V is shown in Fig. 5.1.

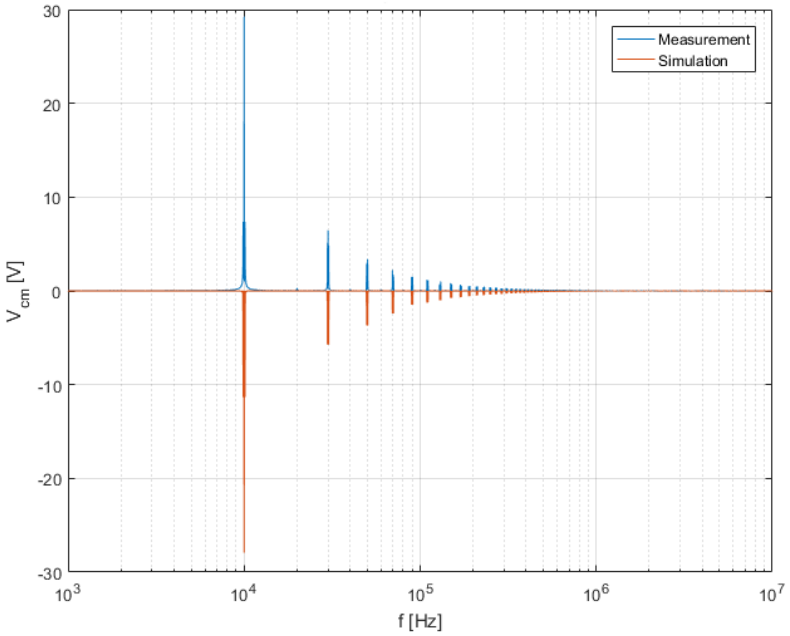


Fig. 5.1: Comparison of the frequency analysis of the CM voltage of simulation and measurement

As can be seen, the simulation model shows the same behavior as the physical device and a good match was achieved. The peak at 10 kHz is 29.24 V for the measurement and 28.53

V for the simulation, which is a difference of 2.43 %. The deviation between the 10 kHz peaks for each supply voltage can be seen in Fig. 5.2

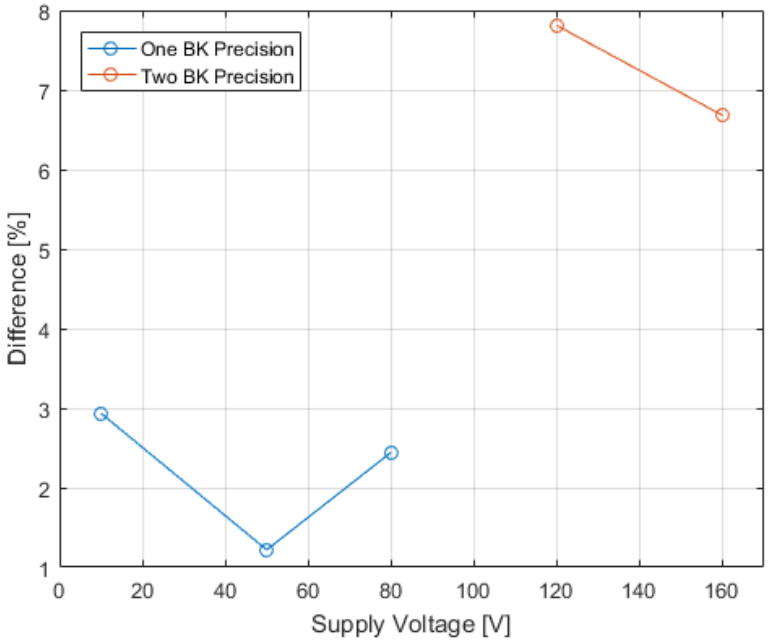


Fig. 5.2: Deviation of the CM voltage between simulation and measurement for the 10 kHz peak

For applied voltages below 80 V only one BK Precision was used as source and for a supply voltage of 120 V and 160 V two of them in master-slave configuration powered the system. As Fig. 5.2 shows, the highest accuracy was achieved at a supply voltage of 50 V. Furthermore, it can be seen that the result of the MM simulation model exhibit an overall better compliance with the measurements performed with just one voltage source. Therefore, it can be assumed that the two voltage sources in series result in a possible change of the parasitic coupling effect on the source side. Consequently, the variance increased with the change of the circuit setup. This could be proofed, by repeating the measurements for 10 V, 50 V and 80 V with the serial connection of the two power sources as used for the two performed measurements with higher voltages, but this test was not executed. It also was observed that the deviation of 2.93% for a supply voltage of 10 V was caused by the free wheeling diodes, which resulted in a voltage jump of approximately 1 V, as it can be seen in Fig. 5.3 circled in red.

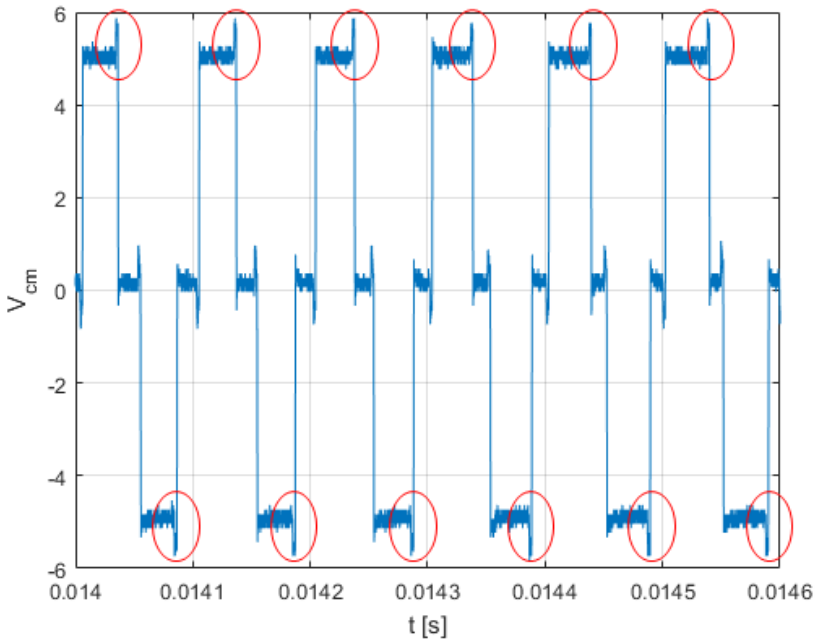


Fig. 5.3: Measured common-mode voltage for 10 V supply voltage

A comparison of the mean peaks occurred within the time domain signal as it was performed in Chapter 4 for the CM voltage and CM current can be seen in Fig. 5.4. It was surprising that the highest deviation occurred at the same supply voltage, where the comparison of the FFT showed the best match and the measurement setup with two serial voltage sources show a very low deviation of 0.24%. The comparison of the mean time domain peak shows an overall accuracy of over 99%.

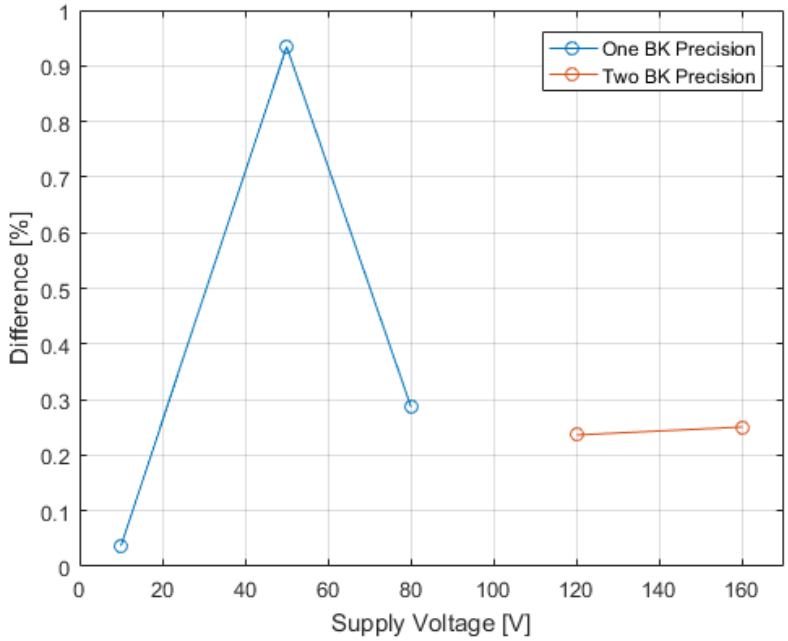


Fig. 5.4: Deviation of the CM voltage between simulation and measurement for mean peaks in time domain signal

Both, the comparison of the 10 kHz peak of the FFT and the comparison of the mean peak in the time domain, leads to the conclusion that the simulation of mixed-mode model results in an accurate replication of the physical devices common-mode voltage.

As a further step to validate the model, the result of the measured CM current is compared with the outcome of the simulation. This comparison can be seen in Fig. 5.5.

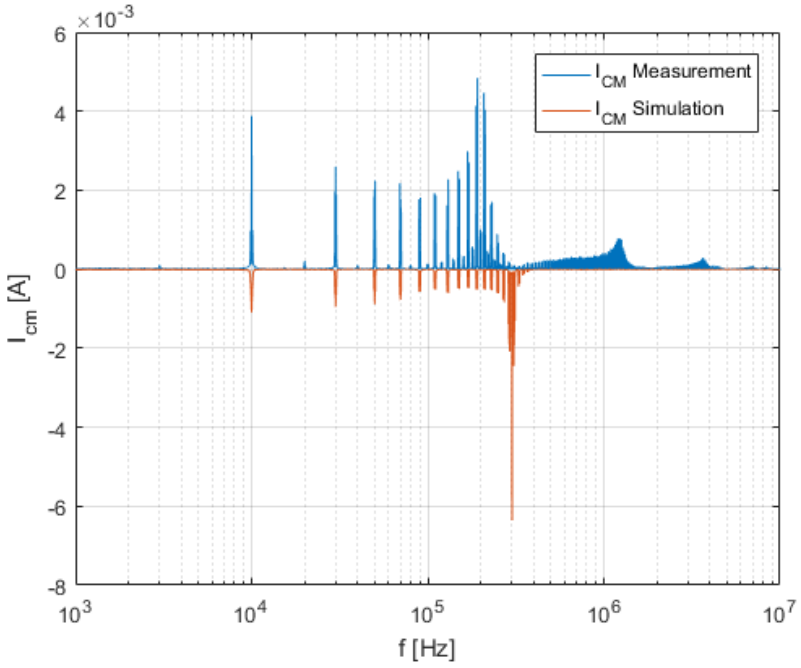


Fig. 5.5: Comparison of the frequency analysis of the CM current of the mixed mode simulation model and the measurement for 80 V supply voltage

The comparison of the two signals shows that the main intensity peak is shifted to a higher frequency from 191 kHz in the measurement to 301 kHz in the simulation. These root of these high frequency peaks is the resonance caused by the presented parasitic elements of the system (capacitances and inductances). The intensity peaks for frequencies below that peak are lower. In contrast to the CM voltage the currents exhibit bigger differences. This could be caused by several different reasons. For example, the values of the parasitic coupling of the MOSFETs to ground is based on earlier measurements. Therefore, the exact capacitive coupling is unknown, since an evaluation by own performed measurements was not possible. The values of the properties of the non-ideal switching devices were estimated based on literature and simulation experiments, which represents another possible failure source. Both of these possible error sources could have an impact on the outcome. The result of the CM current under neglection of the parasitic path through the MOSFETs heat sink to ground can be seen in Fig. 5.6.

It can be seen that a complete neglection of the heat sinks parasitics results in a better match of the simulation with the performed measurement. This leads to the assumption that the chosen parasitics are to high. Moreover, it could be possible that the CM current flowing over the heat sink is so small that it could be neglected without bigger affects on the simulation accuracy. This could be one reason how the authors of [41] were able achieve such a high accuracy with the CM model approach.

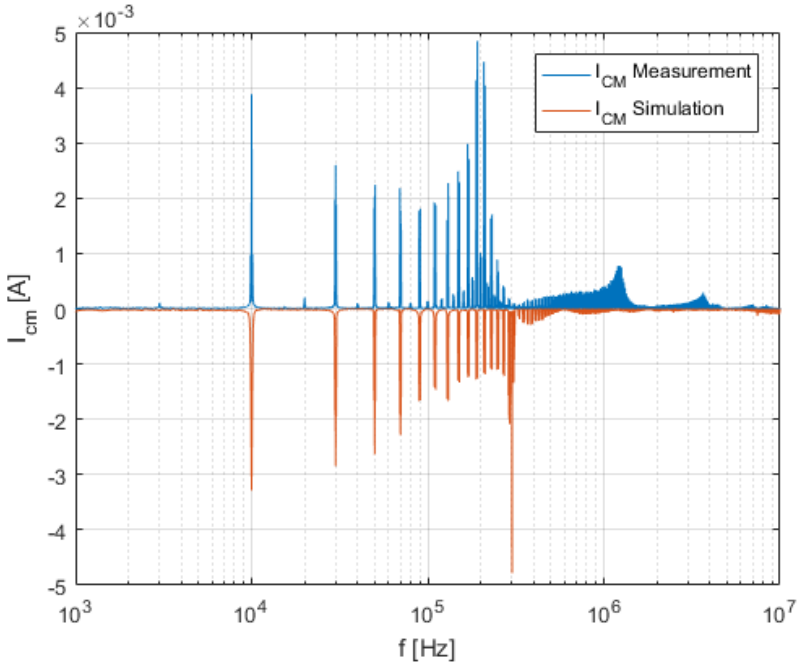


Fig. 5.6: Comparison of the frequency analysis of the CM current of the mixed mode simulation model and the measurement for 80 V supply voltage under neglection of the parasitic grounding path over the heat sink

A further source of deviation is the coupled inductor, since it is not known whether the coupled inductance has a considerable impact on its real behavior. It is possible that a simulation with two individual coils could represent the frequency response in a better way, as it was achieved with the coupled inductor model provided by the PLECS® component library. Another source of the deviation is the estimated value of the low inductive plate. Also here a measurement could not be performed, but its value showed a big importance for the resulting CM current, since it causes a damping of occurring peaks. The neglection of the parasitics caused by the connection cable between the coupled inductors could have served as an additional source for the difference.

However, the simulation matches the measurement for the occurring peaks caused by the switching frequency and with a further configuration of the parasitics it could be possible to reach a better agreement.

5.2 Common-Mode Model

Now, the MM model is evaluated an validated the same can be done for the CM model. Since this simulation uses the CM voltage of the MM model, only the CM current will be evaluated in this section. In Fig. 5.7 the simulation result is compared to the measurement.

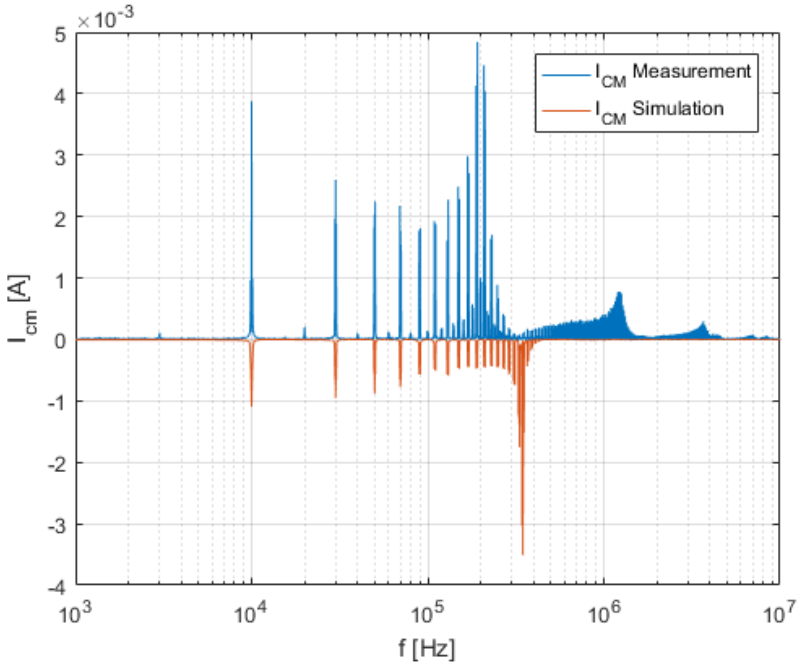


Fig. 5.7: Comparison of the frequency analysis of the CM current of the CM simulation model and the measurement for 80 V supply voltage

Also here the same differences as for the MM model can be observed, but the main intensity peak of the simulation occurs at a frequency of 347 kHz. The difference to the MM simulation can be explained by the additional parasitic inductance of the non-ideal MOSFETs and the mutual inductance, since this is not included in the CM model and replaced by one single coil. The intensity peaks of the CM model are lower than those resulting with the mixed mode model. This could be caused by an overestimated value of the inductance at the load side. This model represents a better match with the measurement when neglecting the parasitics of the heat sink to ground. The simulation result is shown in Fig. 5.8.

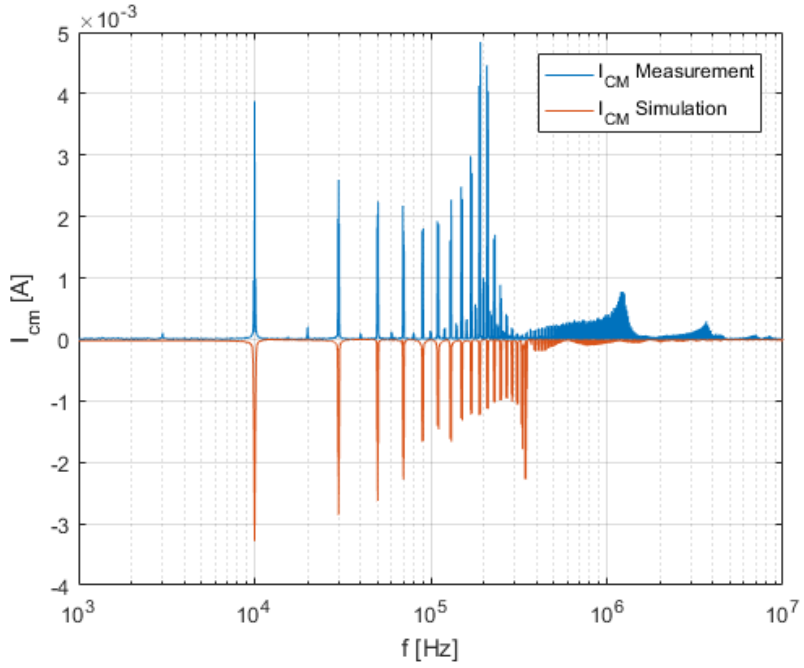


Fig. 5.8: Comparison of the frequency analysis of the CM current of the CM simulation model and the measurement for 80 V supply voltage under neglection of the parasitic grounding path over the heat sink

It can be seen that the form of the overall frequency behavior comes close to the measurement result, especially for the peaks caused by the switching frequency of 10 kHz. Since the CM model is directly dependent on the MM model CM voltage measurement, the root causes of the difference are the same as previously described in Section 5.1.

The comparison of the linearity of the CM current can be seen in Fig. 5.9. In this figure the peaks at 10 kHz for both simulations (MM and CM-model) are compared.

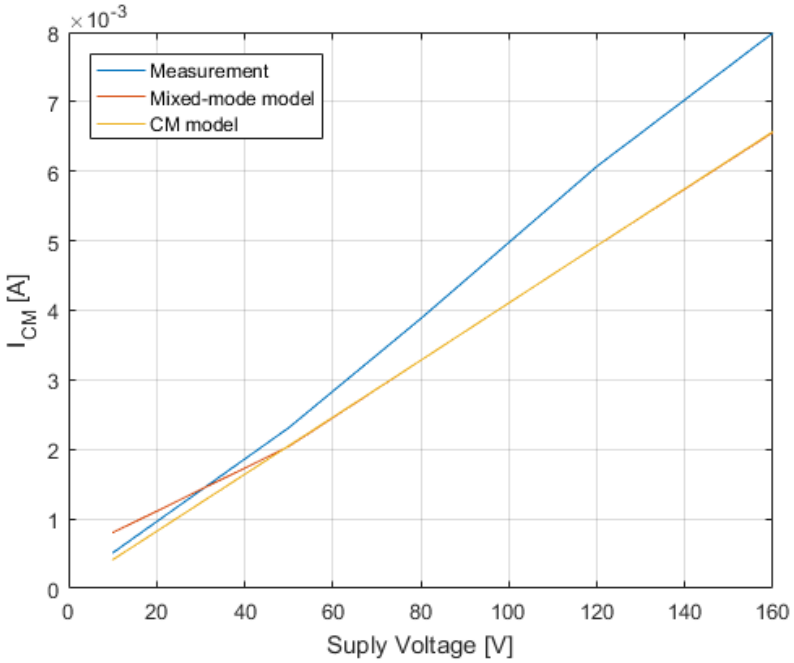


Fig. 5.9: Comparison of the CM current peak at 10 kHz of both simulation models and the measurement for different supply voltages

The deviation of each simulation to the measured value of the physical device is shown in Fig. 5.10.

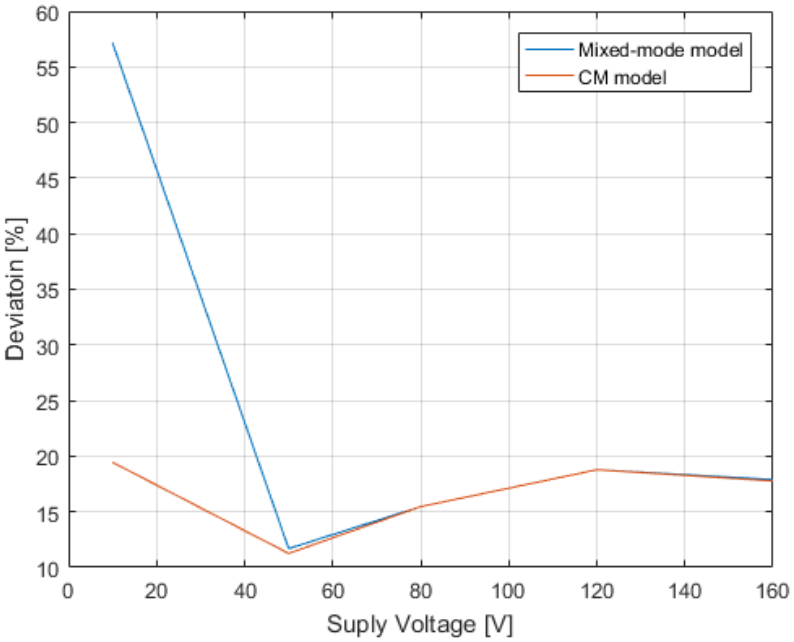


Fig. 5.10: Deviation of the CM current of both simulation models from the measurement

As can be seen, both, the MM simulation and the CM simulation, show a similar deviation

for a supply voltage higher than 50 V. Furthermore, the deviation of the CM model stays below 20% at all points. The high variance of the MM model for a supply voltage of 10 V could be an effect of the non-ideal switching devices and the free wheeling diodes, since both are not included in the CM model, which only consists of the parasitic capacitances to ground and inductances.

6 Conclusion

Because of costs and military capabilities of the U.S. Navy, the design concept of traditional naval ship power distribution systems was reconsidered and the approach of an all-electric ship was created. This new kind of future naval surface vessels uses a medium voltage DC power distribution system, but with the new distribution system new problems were discovered, caused by the effects of EMI. Especially the common-mode of conducted EMI causes undesired behavior of system components such as sensors and communication and is mainly caused by switching converters. Therefore, the understanding of the occurring common-mode phenomena and its effect on system components of an electrical ship is of great importance. In order to predict the possible CM behavior of single system components and to determine its affect on the overall system, an accurate simulation of the system is needed, capable of reproducing the CM behavior. A simulation model, which includes all parasitics and CM current pathways in great detail, is called MM model, since it represents the differential-mode (intended) and common-mode (unintended) of the system. A MM simulation yields a high computational effort. The model can be reconstructed into a CM model, which only emulates the CM behavior of the system. This approach and its capability to replicate the CM current of the device of interest was shown in [41]. This reference served as basis for this thesis. The goal was to replicate the CM behavior of a device under test within a simulation and to investigate the effect of parasitics occurring in switching elements.

In this work a basic DM simulation model was created of a PEBB with SiC MOSFET H-bridge of a medium voltage IMU designed by the Center for Power Electronics at Virginia Tech. The parasitic capacitive coupling effects of the physical device and the parasitic elements each individual component exhibits were identified by performing scattering parameter measurements and impedance measurements with a vector network analyzer. The DM model was extended to a MM model by adding the determined parasitic grounding paths of the source, the DC-link capacitor, the inverters heat sink and the coupled inductors considering symmetry way. To achieve a better match of the devices frequency behavior, frequency dependent components were constructed and implemented in the model. Based on the resulting model, a CM equivalent circuit was derived, which is capable of representing the PEBB's CM current. Both, the CM voltage and the CM current of the PEBB were measured, identified and analyzed. The CM voltage was compared to the simulation result of the MM model and the CM current was compared to both, the MM and

the CM model. The comparison of the CM voltages showed a good agreement, while the simulated CM current exhibits differences in comparison with the measurement results. However, the CM behavior of the device under test was reconstructed successfully with a simulation and an overall deviation off less than 8% for the CM voltage and 20% for the CM current. Moreover, it was shown that a neglection of the parasitic grounding of the MOSFETs over their heat sink lead to more accurate simulation results than if they were taken into account.

To achieve a higher accuracy of the replication of the PEBBs CM behavior, a more detailed investigation of the parasitics needs to be performed, especially for the low inductive plate, which connects the DC-link capacitors directly with the inverter. Furthermore, non-ideal MOSFETs were used in the MM simulation. These components required detailed values of the device, which had to be estimated or determined by a trial and error procedure, since no data sheet was available. In a next step, these values will be discussed with Virginia Tech. A further improvement can be achieved by performing a fitting of impedances by the use of evolutionary computing as performed in [41]. This would minimize the deviation between the measurement and simulation.

A further improvement could be reached, by implementing the diversification of the snubber capacitors, since this would effect the symmetry of the system and consequently the CM behavior of the device. Therefore, the true capacitance of each snubber capacitor should be determined. With the two connection points on the DC side and the two connection points on the AC side of the inverter one can perform up to six different measurements, which represent various parallel and series circuits of the capacitive components. Per measurement one obtains one equation. By performing four out of these six possible measurements one would be able to recalculate the capacitance of each snubber capacitor. Since it is not possible to separate the inverter from the low inductive plate and subsequently from the DC-link capacitor, the resulting capacitances could be influenced by the connected system parts. It still would represent a good estimation and grant insight into the scattering of the value of the snubber capacitors.

7 List of abbreviations

Abbreviation	Explanation
AES	All-electrical ship
CAPS	Center of Advanced Power Systems
CISPR	International Special Committee on Radio Interference
CM	Common-mode
CPES	Center for Power Electronics
DM	Differential-mode
DoD	Department of Defense
DUT	Device under test
EEC	European Economic Consortium
EMC	Electromagnetic compatibility
EMI	Electromagnetic interference
ESRDC	Electric Ship Research and Development Consortium
FCC	Federal Communications Commission
FSU	Florida State University
IEC	International Electrotechnical Commission
IMU	Impedance measurement unit
IPS	Integrated power systems
KCL	Kirchhoff's current law
KVL	Kirchhoff's voltage law
LSE	Least square error
MM	Mixed-mode
MVDC	Medium-voltage direct-current
ODE	Ordinary differential equation
ONR	Office of Naval Research
PEBB	Power electronic building block
PWM	Pulse-width modulation

Abbreviation	**Explanation**
RF	Radio frequency
SiC MOSFET	Silicon Carbide metal-oxide-semiconductor field-effect transistor
S-parameter	Scattering-parameter
SPWM	Sinusoidal pulse width modulation
VNA	Vector network analyzer
VT	Virginia Tech

8 List of figures

9 List of Tables

10 Bibliography

[1] Noel N Schulz, Robert E Hebner, Steinar Dale, Roger Dougal, Scott Sudhoff, Ed Zivi, and Chryssostomos Chryssostomidis. The us esrdc advances power system research for shipboard systems. In *Universities Power Engineering Conference, 2008. UPEC 2008. 43rd International*, pages 1–4. IEEE, 2008.

[2] L Graber, S Pekarek, and M Mazzola. Grounding of shipboard power systems-results from research an preliminary guidelines for the shipbuilding industry. *Perdue and FSU and MSU, FL, Tech. Rep*, (0014):08–1, 2014.

[3] JS Thongam, M Tarbouchi, AF Okou, D Bouchard, and R Beguenane. All-electric ships: A eeview of the present state of the art. In *Ecological Vehicles and Renewable Energies, 2013 8th International Conference and Exhibition on*, pages 1–8. IEEE, 2013.

[4] Breanne Wagner. All-electric ship could begin to take shape by 2012. *National Defense*, page 2, 2007.

[5] Lynn J Petersen, Donald J Hoffman, Joseph P Borraccini, and Steven B Swindler. Next-generation power and energy: Maybe not so next generation. *Naval Engineers Journal*, 122(4):59–74, 2010.

[6] Norbert Doerry. Naval power systems: Integrated power systems for the continuity of the electrical power supply. *IEEE Electrification Magazine*, 3(2):12–21, 2015.

[7] Doyle Busse, Jay Erdman, Russel J Kerkman, Dave Schlegel, and Gary Skibinski. Bearing currents and their relationship to pwm drives. *IEEE Transactions on Power Electronics*, 12(2):243–252, 1997.

[8] Bin Wu and Frank A DeWinter. Voltage stress on induction motors in medium-voltage (2300-6900-v) pwm gto csi drives. *IEEE Transactions on Power Electronics*, 12(2):213–220, 1997.

[9] Ning Dai and Fred C Lee. Characterization and analysis of parasitic parameters and their effects in power electronics circuit. In *Power Electronics Specialists Conference, 1996. PESC'96 Record., 27th Annual IEEE*, volume 2, pages 1370–1375. IEEE, 1996.

[10] Rudolf Ribeiro Riehl, Fernando de Souza Campos, Alceu Ferreira Alves, and Ernesto Ruppert Filho. Analysis and methodology for determining the parasitic capacitances in vsi-fed im drives based on pwm technique. In *Induction Motors-Applications, Control and Fault Diagnostics*. InTech, 2015.

[11] C Winterhalter, R Kerkman, D Schlegel, and D Leggate. The effect of circuit parasitic impedance on the performance of igbts in voltage source inverters. In *Applied Power Electronics Conference and Exposition, 2001. APEC 2001. Sixteenth Annual IEEE*, volume 2, pages 995–1001. IEEE, 2001.

[12] Lukas Graber, Diomar Infante, Michael Steurer, and William W Brey. Validation of cable models for simulation of transients in shipboard power systems. In *High Voltage Engineering and Application (ICHVE), 2010 International Conference on*, pages 77–80. IEEE, 2010.

[13] Dudi A Rendusara and Prasad N Enjeti. An improved inverter output filter configuration reduces common and differential modes dv/dt at the motor terminals in pwm drive systems. *IEEE Transactions on Power Electronics*, 13(6):1135–1143, 1998.

[14] Satoshi Ogasawara and Hirofumi Akagi. Modeling and damping of high-frequency leakage currents in pwm inverter-fed ac motor drive systems. *IEEE Transactions on Industry Applications*, 32(5):1105–1114, 1996.

[15] Doyle F Busse, Jay M Erdman, Russel J Kerkman, David W Schlegel, and Gary L Skibinski. An evaluation of the electrostatic shielded induction motor: a solution for rotor shaft voltage buildup and bearing current. *IEEE Transactions on Industry Applications*, 33(6):1563–1570, 1997.

[16] Satoshi Ogasawara, Hideki Ayano, and Hirofumi Akagi. Active cancellation of the common-mode voltage produced by a voltage-source pwm inverter. *Electrical Engineering in Japan*, 124(3):64–72, 1998.

[17] Ogasawara, Satoshi and Ayano, Hideki and Akagi, Hirofumi. An active circuit for cancellation of common-mode voltage generated by a pwm inverter. In *Power Electronics Specialists Conference, 1997. PESC'97 Record., 28th Annual IEEE*, volume 2, pages 1547–1553. IEEE, 1997.

[18] Kfir J Dagan, Adrian Zuckerberger, and Raul Rabinovici. Fourth-arm common-mode voltage mitigation. *IEEE Transactions on Power Electronics*, 31(2):1401–1407, 2016.

[19] Yick Po Chan, Man Hay Pong, Ngai Kit Poon, and Chui Pong Liu. Effective switching mode power supplies common mode noise cancellation technique with zero equipotential transformer models. In *Applied Power Electronics Conference and Exposition (APEC), 2010 Twenty-Fifth Annual IEEE*, pages 571–574. IEEE, 2010.

[20] Dudi A Rendusara, E Cengelci, Prasad N Enjeti, Victor R Stefanovic, and James W Gray. Analysis of common mode voltage-" neutral shift" in medium voltage pwm adjustable speed drive (mv-asd) systems. *IEEE transactions on power electronics*, 15(6):1124–1133, 2000.

[21] Alexander L Julian, Giovanna Oriti, and Thomas A Lipo. Elimination of common-mode voltage in three-phase sinusoidal power converters. *IEEE Transactions on Power Electronics*, 14(5):982–989, 1999.

[22] Kaushik Basu and Ned Mohan. A high-frequency link single-stage pwm inverter with common-mode voltage suppression and source-based commutation of leakage energy. *IEEE Transactions on Power Electronics*, 29(8):3907–3918, 2014.

[23] Daniel Cochrane. *Passive cancellation of common-mode electromagnetic interference in switching power converters*. PhD thesis, University Libraries, Virginia Polytechnic Institute and State University, 2001.

[24] Giovanna Oriti, Alexander L Julian, and Thomas A Lipo. A new space vector modulation strategy for common mode voltage reduction [in pwm invertors]. In *Power Electronics Specialists Conference, 1997. PESC'97 Record., 28th Annual IEEE*, volume 2, pages 1541–1546. IEEE, 1997.

[25] NLH Bang, NV Nho, NKT Tam, and NM Dung. A phase shifted pwm technique for common-mode voltage reduction in five level h-bridge cascaded inverter. In *Green Energy for Sustainable Development (ICUE), 2014 International Conference and Utility Exhibition on*, pages 1–7. IEEE, 2014.

[26] L Graber, M Steurer, J Kvitkovic, M Kofler, S Pekarek, RA Howard, A Taher, MS Mazzola, and AE Card. Time and frequency domain methods to evaluate grounding strategies for medium voltage dc shipboard power systems. In *Electric Ship Technologies Symposium (ESTS), 2013 IEEE*, pages 43–48. IEEE, 2013.

[27] Steven Pekarek Matthew Bosworth, Mischa Steurer. Grounding and common-mode characterization. Technical Report N0014-08-01-0080, N00014-15-1-2250, ESRDC, dec 2016.

[28] Dorca Lee, Diomar Infante, James Langston, Svetlana V Poroseva, Michael Steurer, and Thomas Baldwin. Grounding studies in a medium voltage dc shipboard power system with uncertain parameters. In *Proceedings of the 2010 Conference on Grand Challenges in Modeling & Simulation*, pages 113–120. Society for Modeling & Simulation International, 2010.

[29] Diomar Infante, James Langston, Lukas Graber, and Michael Steurer. Guiding the selection of physical experiments supporting validation of electric power system models. In *Proceedings of the 2011 Grand Challenges on Modeling and Simulation Conference*, pages 173–180. Society for Modeling & Simulation International, 2011.

[30] Hung-I Hsieh and Sheng-Fang Shih. Effects of transformer structures on the noise balancing and cancellation mechanisms of switching power converters. In *Power Electronics Conference (IPEC-Hiroshima 2014-ECCE-ASIA), 2014 International*, pages 2380–2384. IEEE, May 2014.

[31] Hung-I Hsieh, Sheng-Fang Shih, Hao Wang, and Yung-Hsin Liao. Novel techniques to reduce common-mode (cm) and mix-mode (mm) EMI noise emissions based on noise balance and cancellation. In *Power and Energy (PECon), 2016 IEEE International Conference on*, pages 145–149. IEEE, 2016.

[32] Henry W Ott. Understanding and controlling common-mode emissions in high-power electronics, 2001.

[33] Steven Keeping. Design trade-offs when selecting a high-frequency switching regulator, 2015-02-24. Online; Accessed: July 5, 2017.

[34] Firuz Zare. *Electromagnetic Interference Issues in Power Electronics and Power Systems*. Bentham Science Publishers, 2011.

[35] Erkuan Zhong and Thomas A Lipo. Improvements in EMC performance of inverter-fed motor drives. *IEEE Transactions on Industry Applications*, 31(6):1247–1256, 1995.

[36] Jay M Erdman, Russel J Kerkman, David W Schlegel, and Gary L Skibinski. Effect of pwm inverters on ac motor bearing currents and shaft voltages. *IEEE transactions on Industry Applications*, 32(2):250–259, 1996.

[37] SD Sudhoff, JL Tichenor, and JL Drewniak. Wide-bandwidth multi-resolutional analysis of a surface-mounted pm synchronous machine. *IEEE Transactions on Energy Conversion*, 14(4):1011–1018, 1999.

[38] S Chen, TW Nehl, J-S Lai, X Huang, E Pepa, R De Doncker, and I Voss. Towards EMI prediction of a pm motor drive for automotive applications. In *Applied Power Electronics Conference and Exposition, 2003. APEC'03. Eighteenth Annual IEEE*, volume 1, pages 14–22. IEEE, 2003.

[39] Jih-Sheng Lai, Xudong Huang, Elton Pepa, Shaotang Chen, and Thomas W Nehl. Inverter EMI modeling and simulation methodologies. *IEEE Transactions on Industrial Electronics*, 53(3):736–744, 2006.

[40] Liwei Wang, Carl Ngai-Man Ho, Francisco Canales, and Juri Jatskevich. High-frequency modeling of the long-cable-fed induction motor drive system using tlm approach for predicting overvoltage transients. *IEEE Transactions on Power Electronics*, 25(10):2653–2664, 2010.

[41] A. D. Brovont and S. D. Pekarek. Derivation and application of equivalent circuits to model common-mode current in microgrids. *IEEE Journal of Emerging and Selected Topics in Power Electronics*, 5(1):297–308, March 2017.

[42] S Chen, TA Lipo, and D Fitzgerald. Source of induction motor bearing currents caused by pwm inverters. *IEEE Transactions on Energy Conversion*, 11(1):25–32, 1996.

[43] Shaotang Chen, Thomas A Lipo, and Dennis Fitzgerald. Modeling of motor bearing currents in pwm inverter drives. *IEEE Transactions on Industry Applications*, 32(6):1365–1370, 1996.

[44] Shaotang Chen and Thomas A Lipo. Bearing currents and shaft voltages of an induction motor under hard-and soft-switching inverter excitation. *IEEE Transactions on Industry Applications*, 34(5):1042–1048, 1998.

[45] Richard Zhang, Xin Wu, and Timothy Wang. Analysis of common mode EMI for three-phase voltage source converters. In *Power Electronics Specialist Conference, 2003. PESC'03. 2003 IEEE 34th Annual*, volume 4, pages 1510–1515. IEEE, 2003.

[46] François Costa, Christian Vollaire, and Régis Meuret. Modeling of conducted common mode perturbations in variable-speed drive systems. *IEEE Transactions on Electromagnetic Compatibility*, 47(4):1012–1021, 2005.

[47] Qian Liu, Fei Wang, and Dushan Boroyevich. Modular-terminal-behavioral (mtb) model for characterizing switching module conducted EMI generation in converter systems. *IEEE Transactions on power electronics*, 21(6):1804–1814, 2006.

[48] Annette Muetze and Andreas Binder. Calculation of motor capacitances for prediction of the voltage across the bearings in machines of inverter-based drive systems. *IEEE Transactions on Industry Applications*, 43(3):665–672, 2007.

[49] Lei Zhang, WeiMing Ma, and Jin Meng. Prediction of common mode conducted EMI in pwm inverter-fed machine system. In *Electromagnetic Compatibility and 19th International Zurich Symposium on Electromagnetic Compatibility, 2008. APEMC 2008. Asia-Pacific Symposium on*, pages 827–830. IEEE, 2008.

[50] Yoshitsugu Koyama, Mitsuhiro Tanaka, and Hirofumi Akagi. Modeling and analysis for simulation of common-mode noises produced by an inverter-driven air conditioner. *IEEE Transactions on Industry Applications*, 47(5):2166–2174, 2011.

[51] Pengju Kong, Yan Jiang, and Fred C Lee. Common mode EMI noise characteristics of low-power ac–dc converters. *IEEE transactions on power Electronics*, 27(2):731–738, 2012.

[52] AD Brovont and SD Pekarek. Equivalent circuits for common-mode analysis of naval power systems. In *Electric Ship Technologies Symposium (ESTS), 2015 IEEE*, pages 245–250. IEEE, 2015.

[53] Gordana Felic and Rob Evans. Study of heat sink EMI effects in smps circuits. In *Electromagnetic Compatibility, 2001. EMC. 2001 IEEE International Symposium on*, volume 1, pages 254–259. IEEE, 2001.

[54] Andrea Dolente. *Analysis of the heatsink influence on conducted and radiated electromagnetic interference in power electronic converters.* PhD thesis, alma, 2007.

[55] International Electrotechnical Commission and others. International special committee on radio interference (CISPR),", 1975.

[56] Radiofrequency Electromagnetic Fields. Evaluating compliance with fcc guidelines for human exposure to radiofrequency electromagnetic fields. *OET Bulletin 65*, 1997.

[57] Henry W Ott. *Noise reduction techniques in electronic systems*, volume 442. John Wiley & Sons New York, 1988.

[58] Ashok Bindra. Understanding electromagnetic compatibility standards for switch-mode power supplies, 2012-06-05. Online; Accessed: July 3, 2017.

[59] Vrej Barkhordarian et al. Power mosfet basics. *Powerconversion and Intelligent Motion-English Edition*, 22(6), 1996.

[60] Christian R Mueller and Stefan Buschhorn. Impact of module parasitics on the performance of fastswitching devices. In *PCIM Europe 2014; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management; Proceedings of*, pages 1–8. VDE, 2014.

[61] David E Bockelman and William R Eisenstadt. Combined differential and common-mode scattering parameters: Theory and simulation. *IEEE transactions on microwave theory and techniques*, 43(7):1530–1539, 1995.

[62] David E Bockelman, William R Eisenstadt, and Robert Stengel. Accuracy estimation of mixed-mode scattering parameter measurements. *IEEE Transactions on Microwave theory and techniques*, 47(1):102–105, 1999.

[63] David E Bockelman and William R Eisenstadt. Pure-mode network analyzer for on-wafer measurements of mixed-mode s-parameters of differential circuits. *IEEE Transactions on Microwave Theory and Techniques*, 45(7):1071–1077, 1997.

[64] David E Bockelman and William R Eisenstadt. Combined differential and common-mode analysis of power splitters and combiners. *IEEE Transactions on Microwave Theory and Techniques*, 43(11):2627–2632, 1995.

[65] W Fan, Albert Lu, LL Wai, and BK Lok. Mixed-mode s-parameter characterization of differential structures. In *Electronics Packaging Technology, 2003 5th Conference (EPTC 2003)*, pages 533–537. IEEE, 2003.

[66] Marina Koledintseva and Tracey Vincent. Comparison of mixed-mode s-parameters in weak and strong coupled differential pairs. In *Electromagnetic Compatibility (EMC), 2016 IEEE International Symposium on*, pages 610–615. IEEE, 2016.

[67] Lore-Anne Ponirakis. Medium voltage silicon carbide power components, 2016-01-11. Online; Accessed: August 1, 2017.

[68] Jess Brown. Power mosfet basics: Understanding gate charge and using it to assess switching performance. *Vishay Siliconix, AN608*, 2004.

[69] Mohebali Behshad. Analysis of the imu: 2^{nd} report, 2015.

[70] Baseplate capacitance analysis for sic half-bridge modules.

[71] J Allmeling and W Hammer. Plecs-user manual, 2013.

[72] Todd H Hubing. Non-ideal behavior of components. In *Global EMC University, IEEE International Symposium on Electromagnetic Compatibility*, 2007.

[73] A. M. Niknejad and Joel Dunsmore. High frequency passive components, 2013.

[74] Martin O Hara. Modeling non-ideal inductors in spice. *Newport Components, UK*, 1993.

[75] Matthew Bosworth and Michael Steurer. A measurement based framework for the analysis of common mode coupling effects in power electronics dominated medium voltage power systems (part 1), 2016.

[76] Mohebali Behshad. Fixture impedance check (report), 2015.

[77] David Grider, Mrinal Das, Anant Agarwal, John Palmour, Scott Leslie, John Ostop, Ravisekhar Raju, Michael Schutten, and Al Hefner. 10 kv/120 a sic dmosfet half h-bridge power modules for 1 mva solid state power substation. In *Electric Ship Technologies Symposium (ESTS), 2011 IEEE*, pages 131–134. IEEE, 2011.

[78] Mrinal K Das, Craig Capell, David E Grider, Scott Leslie, John Ostop, Ravi Raju, Michael Schutten, Jeffrey Nasadoski, and Allen Hefner. 10 kv, 120 a sic half h-bridge power mosfet modules suitable for high frequency, medium voltage applications. In *Energy Conversion Congress and Exposition (ECCE), 2011 IEEE*, pages 2689–2692. IEEE, 2011.

[79] Igor Cvetkovic, Zhiyu Shen, Marko Jaksic, Christina DiMarino, Fang Chen, Dushan Boroyevich, and Rolando Burgos. Modular scalable medium-voltage impedance measurement unit using 10 kv sic mosfet pebbs. In *Electric Ship Technologies Symposium (ESTS), 2015 IEEE*, pages 326–331. IEEE, 2015.

[80] Max Fogiel. *Handbook of basic electricity*. Research & Education Assoc., 2002.

[81] Hewlett Packard. S parameter techniques for faster, more accurate network design. *Test & Measurement, Application Note*, pages 95–1, 1996.

[82] S-Parameter Design. Application note 154. *Agilent Technologies*, 1972.

[83] Ken Vaz and Michael Caggiano. Measurement technique for the extraction of differential s-parameters from single-ended s-parameters. In *Electronics Technology: Meeting the Challenges of Electronics Technology Progress, 2004. 27th International Spring Seminar on*, volume 2, pages 313–317. IEEE, 2004.

[84] Allan Huynh, Magnus Karlsson, and Shaofang Gong. Mixed-mode s-parameters and conversion techniques. In *Advanced Microwave Circuits and Systems*. InTech Open Access Publisher, 2010.

11 Appendix A: Scattering Parameters

Scattering-parameters (S-parameters) describe the electrical behavior of linear electrical networks when experiencing various steady state stimuli induced by electrical signals. S-parameters represent the linear electrical behavior of any linear time-invariant (LTI) system and are mostly used for the characterization of networks operating at radio frequencies (RF) and microwave frequencies, due to the fact, that currents and voltages are harder to quantify at high frequencies than signal power and energy. Therefore, their main application is in microwave engineering. A characterization of power electronic devices (PED) with this kind of measurement is not common, because PEDs are strongly not linear, since semiconductors and control circuits are included in almost any power electronic circuit. Nevertheless, the use of S-parameter measurements found their way into the characterization of MVDC systems.

The reason for this lies within the simplicity of the measurement itself, since there is no need for short or open circuits, as needed for the system characterization with impedance measurements, which could possibly hard to realize dependent on the hardware setup. Unlike an impedance analyzer scattering parameters use matched loads instead of open or short circuit conditions to characterize a linear electrical network, due to these terminations are much easier to use at high signal frequencies. This is the reason, why S-parameter measurements are helpful for the characterization of complex power electronic circuits. The quantities of the scattering matrix are measured in terms of power. In order to apply this measurement one assumption has to be made. Since there are hardly changes within the system for one specific frequency, the system can be seen as a LTI system approximation the S-parameter measurement is valid.

In the context of S-parameters, scattering refers to the way the traveling injected currents and voltages are affected, when they meet a discontinuity caused by the insertion of power signals into the circuit. In the S-parameter approach, an electrical network is regarded as a “black box”containing various interconnected electrical circuit components or lumped elements such as resistors, capacitors, inductors and transistors. The network is characterized by a square matrix of complex numbers called S-parameter matrix, which can be used to calculate its response to signals applied to the ports.

As mentioned before the system under test has to be a LTI system. For the S-parameter definition, that the entire network, which may contain any component, behaves linearly with incident small signals. It may also include many typical communication system components or blocks such as amplifiers, attenuators, filters, couplers and equalizers provided they are also operating under linear and defined conditions.

An electrical network described by S-parameters may have any number of ports, which are the points of the network at which electrical signals either enter or exit. A port describes a pairs of terminals. S-parameters are used at frequencies where the ports are often coaxial or wave-guide connections. The following information must be defined when specifying a set of S-parameters:

1. the frequency
2. the nominal characteristic impedance (in most cases 50 Ω)
3. the allocation of port numbers
4. conditions which may affect the network, such as temperature, control voltage and bias current, where applicable.

S-parameters are needed, when one is attempting to characterize or measure the wide-bandwidth behavior of power electronic systems, including switching-induced electromagnetic fields, and the behavior of a system in response to faults. The measurement of the single ended S-parameters of a 2-port system is depict in Fig. 11.1.

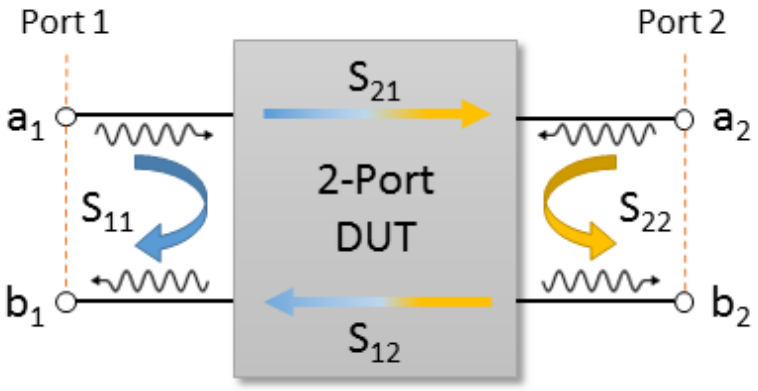


Fig. 11.1: S-Parameter measurement of a 2-port system

S_{11} represents the forward reflection and S_{22} the reverse reflection respectively. Both entries are also referred to as reflection coefficients. S_{21} and S_{12} are referred to as transmission coefficients and define the forward and reverse transmission. For S-parameter measurements, the first indicator represents the receiving port, while the second one specifies the transmitting port. For example $S21$ refers to the signal transmitted to port two

for the signal incident at port one. The generalized formalization can be written as

$$S_{ij} = \frac{\text{received wave at port i}}{\text{sent wave of port j}} \tag{11.1}$$

The result of the measurement is the S-matrix as follows

$$S = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} \tag{11.2}$$

Each of the entries is calculated by the ratio of the incident wave power (a_1, a_2) and the transmitted wave power (b_1, b_2). These wave powers are defined by:

$$a_i = \frac{V_i + Z_0 I_i}{2\sqrt{Z_0}} \tag{11.3}$$

$$b_i = \frac{V_i - Z_0 I_i}{2\sqrt{Z_0}} \tag{11.4}$$

where V_i represents the voltage across port i (e.g. the voltage across terminal a_1 and b_1 in Fig. 11.1), Z_0 the reference impedance, which exhibits a typical value of 50 Ω and I_i describes the current flowing into port i. A linear network can be characterized by a set of simultaneous equations describing the existing waves form each port in terms of incident waves. The following equations describe the derivation of each S-parameter [81]

$$S_{11} = \left.\frac{b_1}{a_1}\right|_{a_2=0} \tag{11.5}$$

$$S_{21} = \left.\frac{b_2}{a_1}\right|_{a_2=0} \tag{11.6}$$

$$S_{21} = \left.\frac{b_1}{a_2}\right|_{a_1=0} \tag{11.7}$$

$$S_{22} = \left.\frac{b_2}{a_2}\right|_{a_1=0} \tag{11.8}$$

This can be rewritten in matrix form as

$$\vec{b} = \mathbf{S} \cdot \vec{a} \tag{11.9}$$

$$\begin{bmatrix} b_1 \\ b_2 \end{bmatrix} = \begin{bmatrix} s_{11} & s_{12} \\ s_{21} & s_{22} \end{bmatrix} \begin{bmatrix} a_1 \\ a_2 \end{bmatrix} \tag{11.10}$$

In the same manner as the 2-port network an n-port measurement can be defined and results in [82]

$$\begin{bmatrix} b_1 \\ b_2 \\ \vdots \\ b_n \end{bmatrix} = \begin{bmatrix} s_{11} & s_{12} & \cdots & s_{1n} \\ s_{21} & s_{22} & \cdots & s_{2n} \\ \vdots & \vdots & \ddots & s_{34} \\ s_{n1} & s_{n2} & \cdots & s_{nn} \end{bmatrix} \begin{bmatrix} a_1 \\ a_2 \\ \vdots \\ a_4 \end{bmatrix} \tag{11.11}$$

S-parameters can be determined by using a VNA, but also can be derived with analytically calculations by numerical methods such as finite element analysis [39], which is used, if an

s-parameter measurement is not suitable or the system of interest is not available.

11.1 Mixed-Mode Scattering Parameters

Since the single-ended S-parameter matrix does not provide any information about the DM and CM matching and transmission, mixed-mode S-parameter matrices are needed. While a two-port single-ended network can be described by a 2x2 S-parameter matrix, a two-port differential-network as depict in Fig. 11.2 requires a 4x4 matrix to get characterized.

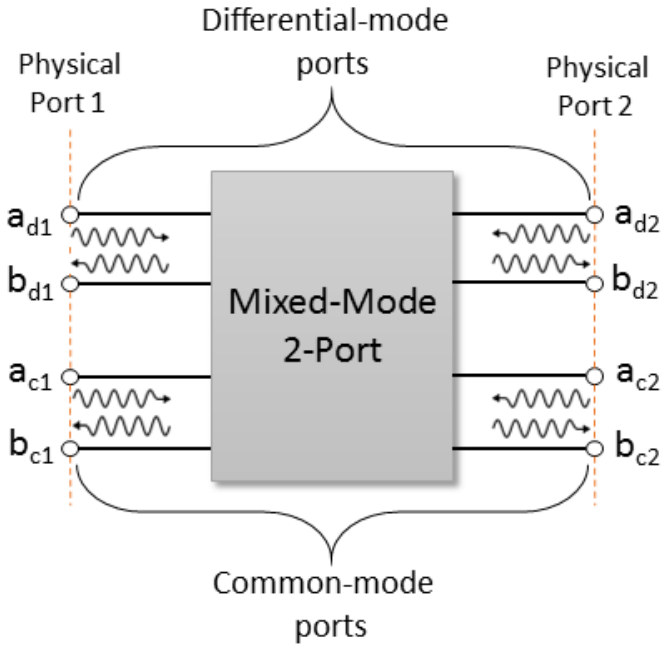


Fig. 11.2: Definition of a differential two-port network [61]

As presented in [61], generalized mixed-mode S-parameters can be written as

$$\vec{b}_{MM} = \mathbf{S}_{MM} \cdot \vec{a}_{MM} \tag{11.12}$$

$$\begin{bmatrix} b_{d1} \\ b_{d2} \\ b_{c1} \\ b_{c2} \end{bmatrix} = \begin{bmatrix} S_{dd} & S_{dc} \\ S_{cd} & S_{cc} \end{bmatrix} \begin{bmatrix} a_{d1} \\ a_{d2} \\ a_{c1} \\ a_{c2} \end{bmatrix} = \begin{bmatrix} s_{d1d1} & s_{d1d2} & s_{d1c1} & s_{d1c2} \\ s_{d2d1} & s_{d2d2} & s_{d2c1} & s_{d2c2} \\ s_{c1d1} & s_{c1d2} & s_{c1c1} & s_{c1c2} \\ s_{c2d1} & s_{c2d2} & s_{c2c1} & s_{c2c2} \end{bmatrix} \begin{bmatrix} a_{d1} \\ a_{d2} \\ a_{c1} \\ a_{c2} \end{bmatrix} \tag{11.13}$$

where the subscripts d and c denote DM and CM entries and 1 and 2 denote the ports 1 and 2, respectively. Each entry of the 2x2 S-parameter matrix on the right of equation

11.12 represents a sub-matrix. While S_{dd} refers to the four purely differential-mode S-parameters s_{d1d1} to s_{d2d2}, S_{cc} corresponds to the four purely common-mode S-parameters s_{c1c1} to s_{c2c2}. The other two terms S_{dc} and S_{cd} represent the mode-conversion between differential and common-mode, which describe the cross talk between these two modes. Therefore these parameters are also called cross-mode S-parameters [61]. In the further process, S_M will refer to the 4x4 mixed-mode S-parameter matrix in equation 11.12.

The matrix equation can be read as an expression of the output wave b_{di} or b_{ci} in terms of the four input waves a_{d1}, a_{d2}, a_{c1} and a_{c2}. This leads to the four following equations

$$b_{d1} = s_{d1d1}a_{d1} + s_{d1d2}a_{d2} + s_{d1c1}a_{c1} + s_{d1c2}a_{c2} \tag{11.14}$$

$$b_{d2} = s_{d2d1}a_{d1} + s_{d2d2}a_{d2} + s_{d2c1}a_{c1} + s_{d2c2}a_{c2} \tag{11.15}$$

$$b_{c1} = s_{c1d1}a_{d1} + s_{c1d2}a_{d2} + s_{c1c1}a_{c1} + s_{c1c2}a_{c2} \tag{11.16}$$

$$b_{c2} = s_{c2d1}a_{d1} + s_{c2d2}a_{d2} + s_{c2c1}a_{c1} + s_{c2c2}a_{c2} \tag{11.17}$$

The relationship between the incident waves of the single-ended S-parameter and incident waves of the the mixed-mode S-parameters can be written as

$$a_{d1} = \frac{1}{\sqrt{2}}(a_1 - a_2) \tag{11.18}$$

$$a_{d2} = \frac{1}{\sqrt{2}}(a_3 - a_4) \tag{11.19}$$

$$a_{c1} = \frac{1}{\sqrt{2}}(a_1 + a_2) \tag{11.20}$$

$$a_{c2} = \frac{1}{\sqrt{2}}(a_3 + a_4) \tag{11.21}$$

for the differential incident wave a_{di} and common-mode incident wave a_{ci}, respectively. The factor is used for normalization in order to keep the power level constant between the two S-parameter systems. The relationship of the reflected waves can be written in the same way.

$$b_{d1} = \frac{1}{\sqrt{2}}(b_1 - b_2) \tag{11.22}$$

$$b_{d2} = \frac{1}{\sqrt{2}}(b_3 - b_4) \tag{11.23}$$

$$b_{c1} = \frac{1}{\sqrt{2}}(b_1 + b_2) \tag{11.24}$$

$$b_{c2} = \frac{1}{\sqrt{2}}(b_3 + b_4) \tag{11.25}$$

It can be seen, that the choice of the signs are related to the definition of differential- and common-mode. The above cited relation of the incident waves a_i with $i = \{1, 2, 3, 4\}$ and a_{dj} (a_{cj}) with $j = \{1, 2\}$ can be rewritten in matrix form.

$$\begin{bmatrix} a_{d1} \\ a_{d2} \\ a_{c1} \\ a_{c2} \end{bmatrix} = \frac{1}{\sqrt{2}} \begin{bmatrix} 1 & -1 & 0 & 0 \\ 0 & 0 & 1 & -1 \\ 1 & 1 & 0 & 0 \\ 0 & 0 & 1 & 1 \end{bmatrix} \begin{bmatrix} a_1 \\ a_2 \\ a_3 \\ a_4 \end{bmatrix} \tag{11.26}$$

The resulted 4x4 matrix including the normalization factor is the so called mode conversion matrix **M** and leads to a compact form of

$$\vec{a}_M = \mathbf{M} \cdot \vec{a} \tag{11.27}$$

with

$$\mathbf{M} = \frac{1}{\sqrt{2}} \begin{bmatrix} 1 & -1 & 0 & 0 \\ 0 & 0 & 1 & -1 \\ 1 & 1 & 0 & 0 \\ 0 & 0 & 1 & 1 \end{bmatrix} \tag{11.28}$$

The same matrix also arise out of the relation of the response waves b_i and b_{dj} (b_{cj}) and the correlation can be written as

$$\vec{b}_M = \mathbf{M} \cdot \vec{b} \tag{11.29}$$

The conversion matrix is used for an easy conversion of the single-ended S-parameter matrix to a mixed-mode S-parameter matrix.

$$S_M = M \cdot S \cdot M^{-1} \tag{11.30}$$

By using equation 11.30 the four-port single-ended S-parameter matrix gets transferred into its representative mixed-mode version. The equation results in

$$S_M = \left[\begin{array}{cc:cc} \frac{s_{11}-s_{21}-s_{12}+s_{22}}{2} & \frac{s_{13}-s_{23}-s_{14}+s_{24}}{2} & \frac{s_{11}-s_{21}+s_{12}-s_{22}}{2} & \frac{s_{13}-s_{23}+s_{14}-s_{24}}{2} \\ \frac{s_{31}-s_{41}-s_{32}+s_{42}}{2} & \frac{s_{33}-s_{43}-s_{34}+s_{44}}{2} & \frac{s_{31}-s_{41}+s_{32}-s_{42}}{2} & \frac{s_{33}-s_{43}+s_{34}-s_{44}}{2} \\ \hdashline \frac{s_{11}+s_{21}-s_{12}-s_{22}}{2} & \frac{s_{13}+s_{23}-s_{14}-s_{24}}{2} & \frac{s_{11}+s_{21}+s_{12}+s_{22}}{2} & \frac{s_{13}+s_{23}+s_{14}+s_{24}}{2} \\ \frac{s_{31}+s_{41}-s_{32}-s_{42}}{2} & \frac{s_{33}+s_{43}-s_{34}-s_{44}}{2} & \frac{s_{31}+s_{41}+s_{32}+s_{42}}{2} & \frac{s_{33}+s_{43}+s_{34}+s_{44}}{2} \end{array}\right] \tag{11.31}$$

This is also presented in [63,83]. It can be seen, that each of the mixed-mode S-parameter terms is a summation of four single-ended S-parameters. This applies one limitation to the transformation. The accuracy can be significantly declined, if the summation consists of two large approximately equal values and two small values of opposite signs [62]. Equation 11.31 can be written separately for each quadrant of the matrix in four different terms.

The four entries on the upper left are the differential-to-differential terms

$$s_{d1d1} = \frac{1}{2}\left(s_{11} - s_{21} - s_{12} + s_{22}\right) \tag{11.32}$$

$$s_{d1d2} = \frac{1}{2}\left(s_{13} - s_{23} - s_{14} + s_{24}\right) \tag{11.33}$$

$$s_{d2d1} = \frac{1}{2}\left(s_{31} - s_{41} - s_{32} + s_{42}\right) \tag{11.34}$$

$$s_{d2d2} = \frac{1}{2}\left(s_{33} - s_{43} - s_{34} + s_{44}\right) \tag{11.35}$$

and the entries of the quarter on the bottom right are the common-mode-to-common-mode terms

$$s_{c1c1} = \frac{1}{2}\left(s_{11} + s_{21} + s_{12} + s_{22}\right) \tag{11.36}$$

$$s_{c1c2} = \frac{1}{2}\left(s_{13} + s_{23} + s_{14} + s_{24}\right) \tag{11.37}$$

$$s_{c2c1} = \frac{1}{2}\left(s_{31} + s_{41} + s_{32} + s_{42}\right) \tag{11.38}$$

$$s_{c2c2} = \frac{1}{2}\left(s_{33} + s_{43} + s_{34} + s_{44}\right) \tag{11.39}$$

The upper right entries represent the common-mode-to-differential terms

$$s_{d1c1} = \frac{1}{2}\left(s_{11} - s_{21} + s_{12} - s_{22}\right) \tag{11.40}$$

$$s_{d1c2} = \frac{1}{2}\left(s_{13} - s_{23} + s_{14} - s_{24}\right) \tag{11.41}$$

$$s_{d2c1} = \frac{1}{2}\left(s_{31} - s_{41} + s_{32} - s_{42}\right) \tag{11.42}$$

$$s_{d2c2} = \frac{1}{2}\left(s_{33} - s_{43} + s_{34} - s_{44}\right) \tag{11.43}$$

and the last four entries at the bottom left are the differential-to-common-mode terms, respectively.

$$s_{c1d1} = \frac{1}{2}\left(s_{11} + s_{21} - s_{12} - s_{22}\right) \tag{11.44}$$

$$s_{c1d2} = \frac{1}{2}\left(s_{13} + s_{23} - s_{14} - s_{24}\right) \tag{11.45}$$

$$s_{c2d1} = \frac{1}{2}\left(s_{31} + s_{41} - s_{32} - s_{42}\right) \tag{11.46}$$

$$s_{c2d2} = \frac{1}{2}\left(s_{33} + s_{43} - s_{34} - s_{44}\right) \tag{11.47}$$

The detailed calculations and derivations can be read in [84]. If the differential channels would be in perfect balance, all entries of the sub-matrices S_{dc} and S_{cd} would be zero. Consequently no mode conversion between DM and CM signals would occur. This case is impracticable for measurements of real physical devices, but if the cross-mode terms are small in comparison to the DM and CM terms, they may be negligible.

12 Appendix B: Common-Mode Measurement and Simulation Results

In this appendix all simulation and measurement results for the CM voltage and CM current are shown for each applied supply voltage. Five different voltages were used to gain information of the CM behavior of the device: 10 V, 50 V, 80 V, 120 V and 160 V.

12.1 Common-Mode Behavior at 10 V Supply Voltage

In the following figures the frequency analysis of the CM voltage and current can be seen. Fig. 12.1 shows the comparison of the CM voltage determined by a measurement of the PEBB powered by 10 V supply voltage with the simulation result.

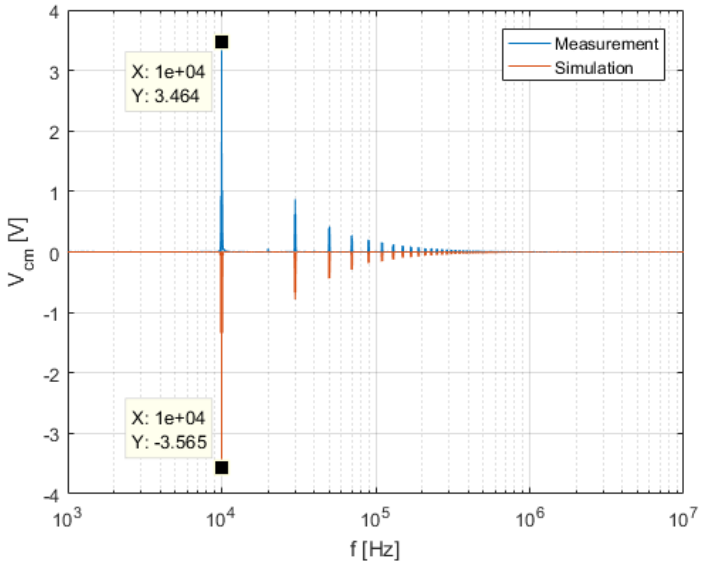


Fig. 12.1: Frequency analysis of the measured and simulated CM voltage for 10 V supply voltage

For the measurement of th CM current two different setups were used. The first hardware setup was under the use of the original XPLE connection cables between each half-bridge and the coupled inductor, which required two separate high current bandwidth probes in

order to measure the current of each rail, due to both cables did not fit into one probe. In this case the resulting signal data requires an additional processing, since the CM current is the sum of all currents through the connected wires. For the second hardware setup common copper wire with two mm in diameter were used instead of the XPLE cable. In this way, it was possible to measure the CM current directly with one current probe. The comparison of the frequency plot can be seen in Fig. 12.2.

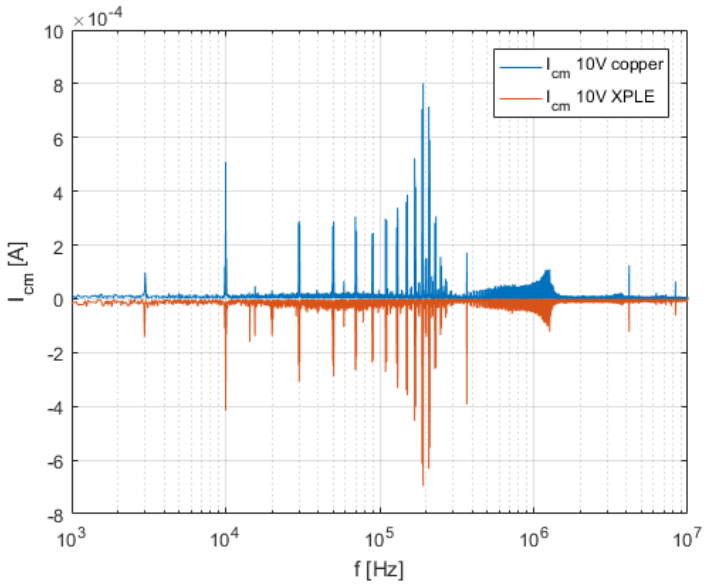
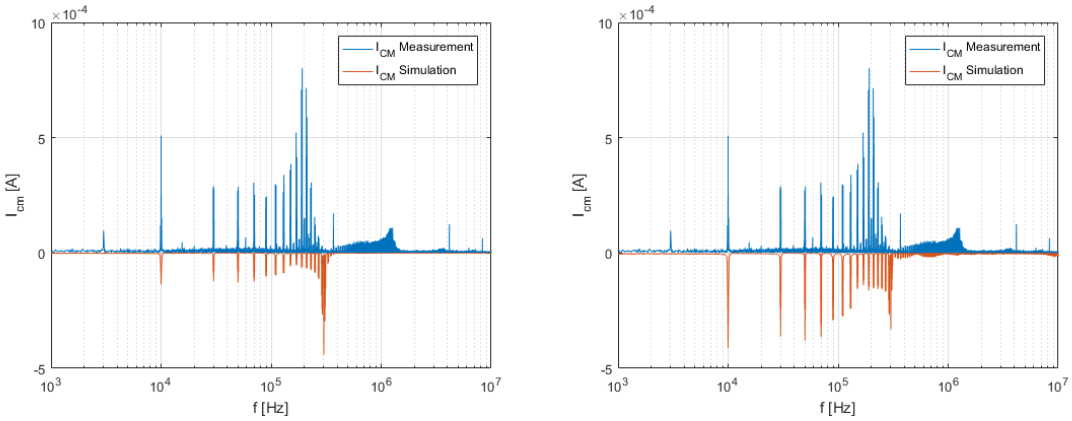


Fig. 12.2: Frequency analysis of the measured CM current for 10 V supply voltage

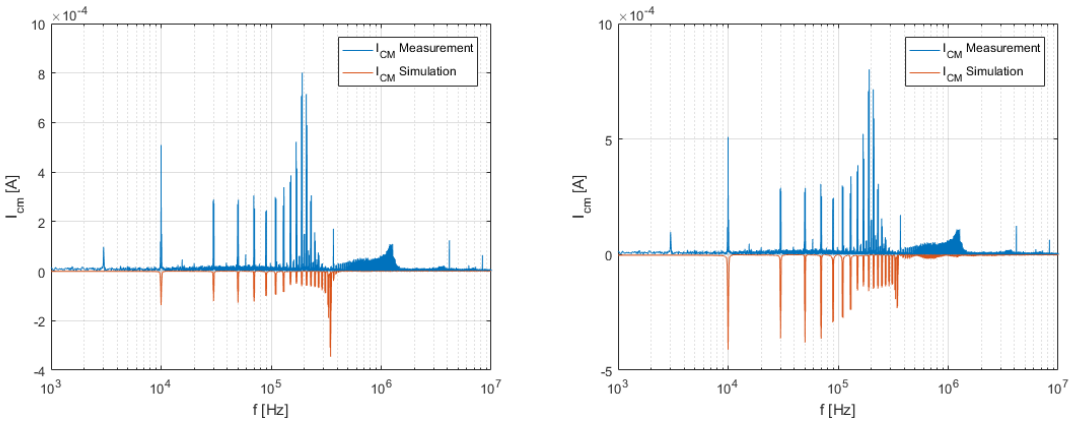
In Fig. 12.3 the CM current of the measurement is compared to the outcome of the mixed-mode simulation. In Fig. 12.3a the parasitic coupling to ground of each MOSFET over its heat sink is taken into account, while Fig. 12.3b shows the comparison under neglection of the parasitic effects of the H-bridge.



(a) (b)

Fig. 12.3: Comparison of the measurement and MM simulation of the CM current for 10 V supply voltage

The same comparison was performed for the CM simulation model and can be seen in Fig. 12.4.



(a) (b)

Fig. 12.4: Comparison of the measurement and CM simulation of the CM current for 10 V supply voltage

As can be seen these measurements exhibit a peak at exactly 3 kHz. Since it is shows up at exact 3 kHz it is assumed that it is not caused by parasitics. Furthermore, it was observed, that its intensity is hardly effected by the supply voltage, which can be seen in the following sections. This is the reason why the integrated control circuits of the power source and the high current bandwidth probe are under suspicion.

In the following sections the same comparisons were performed for another four different

supply voltages. Therefore, it wont be explained anymore.

12.2 Common-Mode Behavior at 50 V Supply Voltage

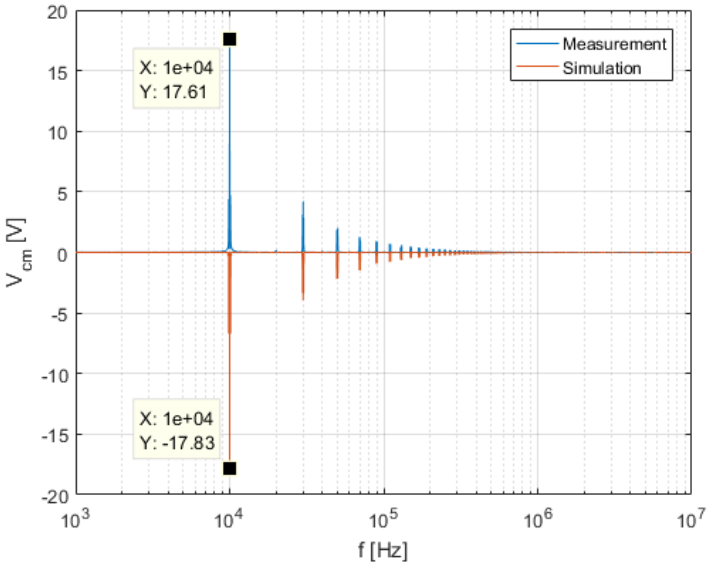


Fig. 12.5: Frequency analysis of measured CM voltage for 50 V supply voltage

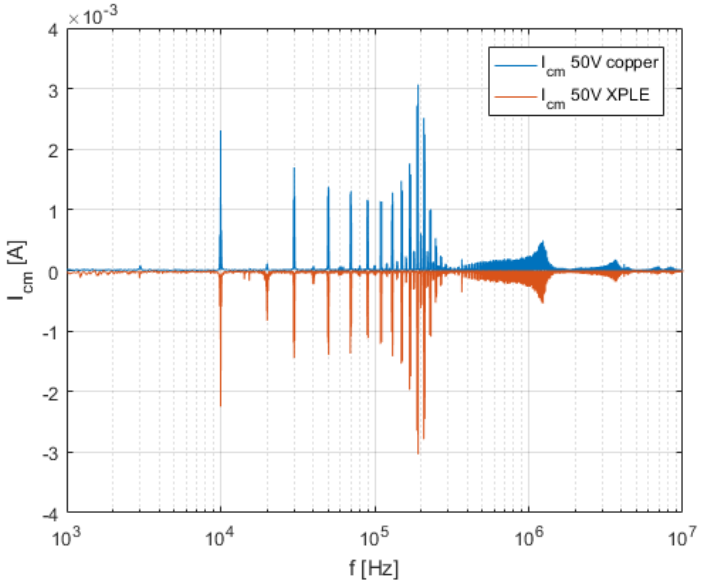
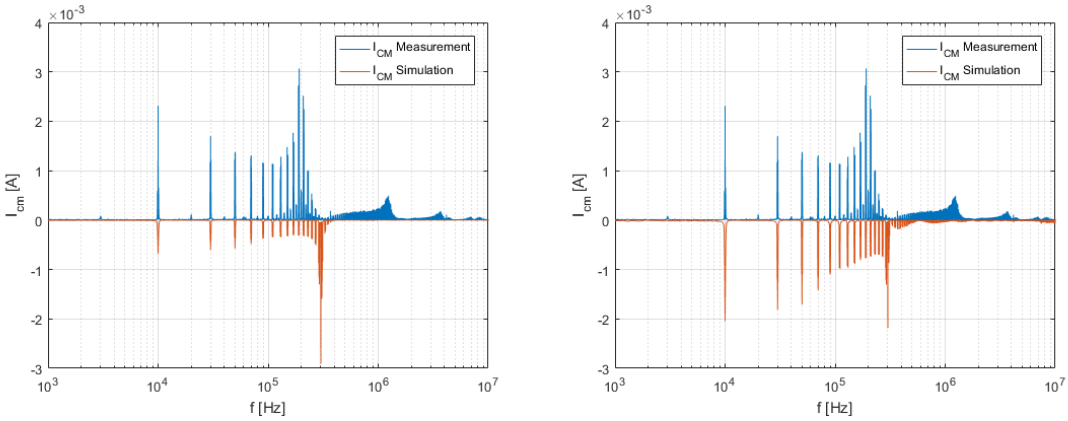
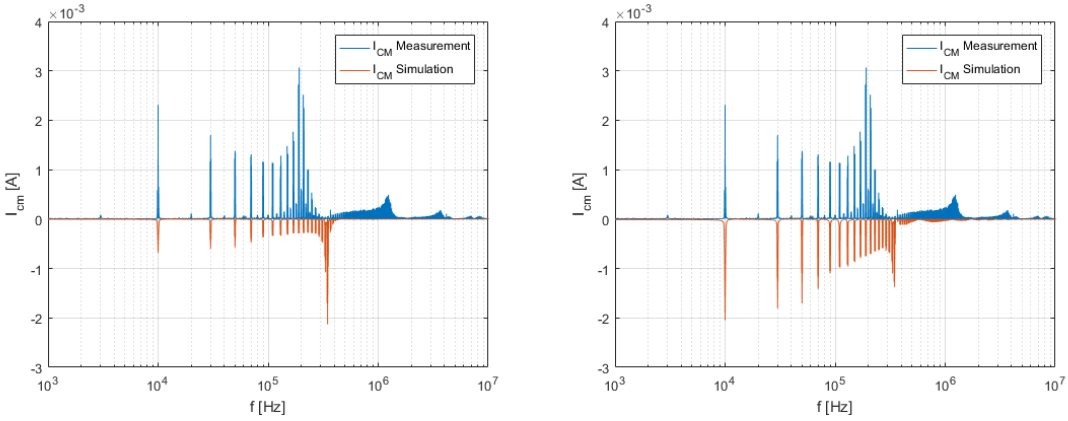


Fig. 12.6: Frequency analysis of the measured CM current for 50 V supply voltage



(a) (b)

Fig. 12.7: Comparison of the measurement and MM simulation of the CM current for 50 V supply voltage



(a) (b)

Fig. 12.8: Comparison of the measurement and CM simulation of the CM current for 50 V supply voltage

12.3 Common-Mode Behavior at 80 V Supply Voltage

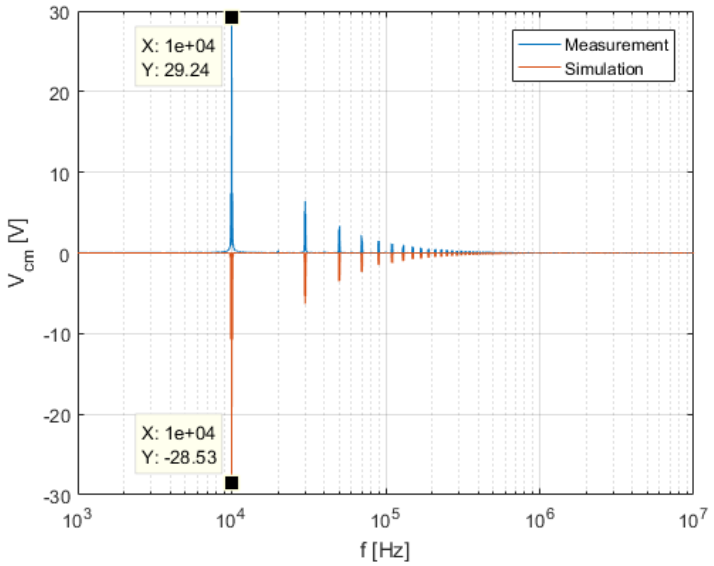


Fig. 12.9: Frequency analysis of measured CM voltage for 80 V supply voltage

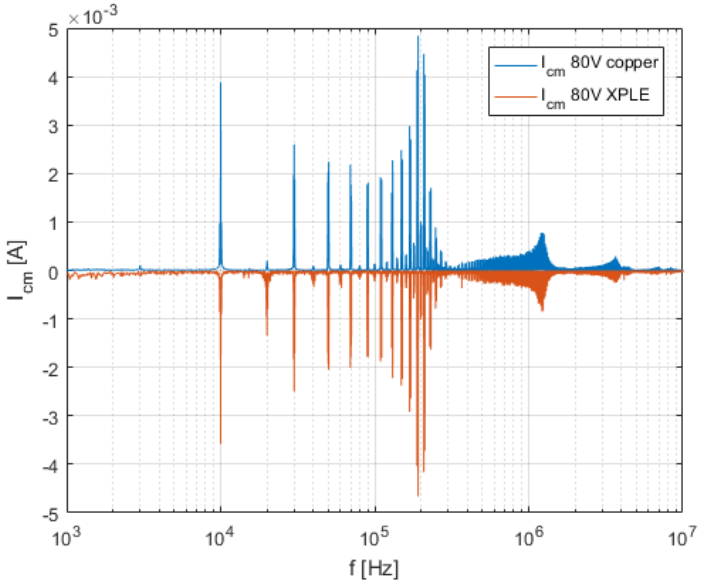


Fig. 12.10: Frequency analysis of the measured CM current for 80 V supply voltage

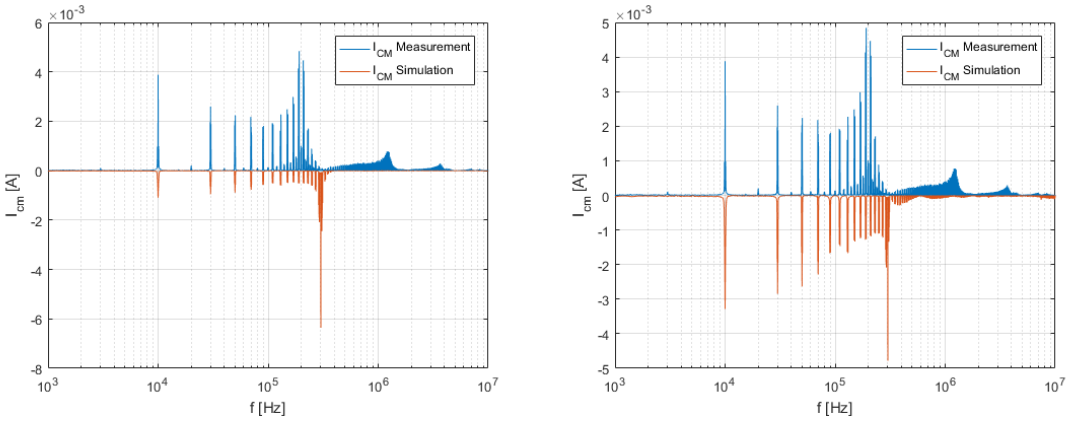


Fig. 12.11: Comparison of the measurement and MM simulation of the CM current for 80 V supply voltage

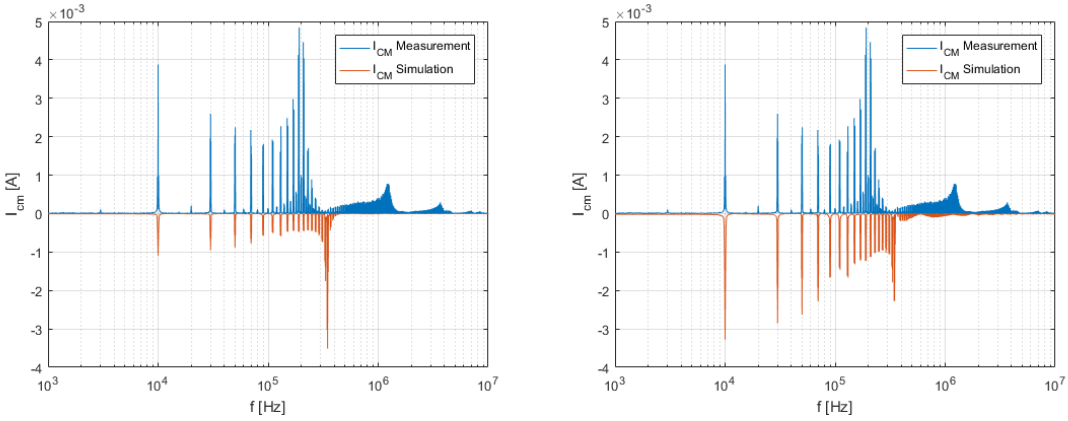


Fig. 12.12: Comparison of the measurement and CM simulation of the CM current for 80 V supply voltage

12.4 Common-Mode Behavior at 120 V Supply Voltage

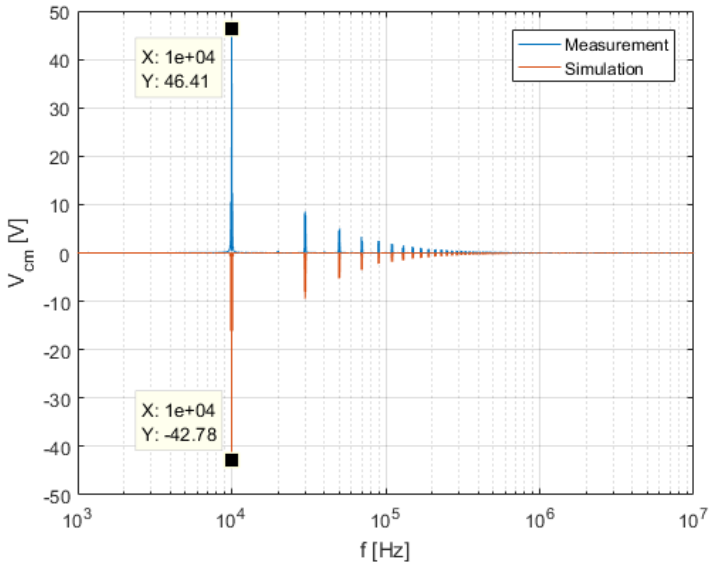


Fig. 12.13: Frequency analysis of measured CM voltage for 120 V supply voltage

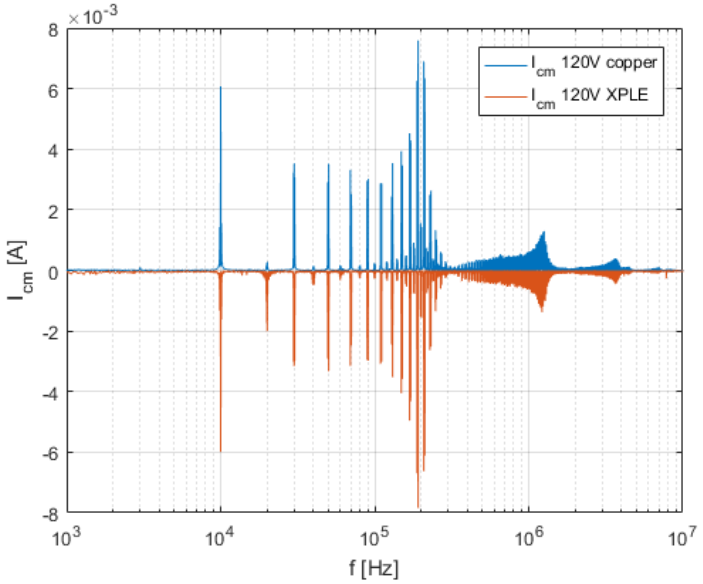
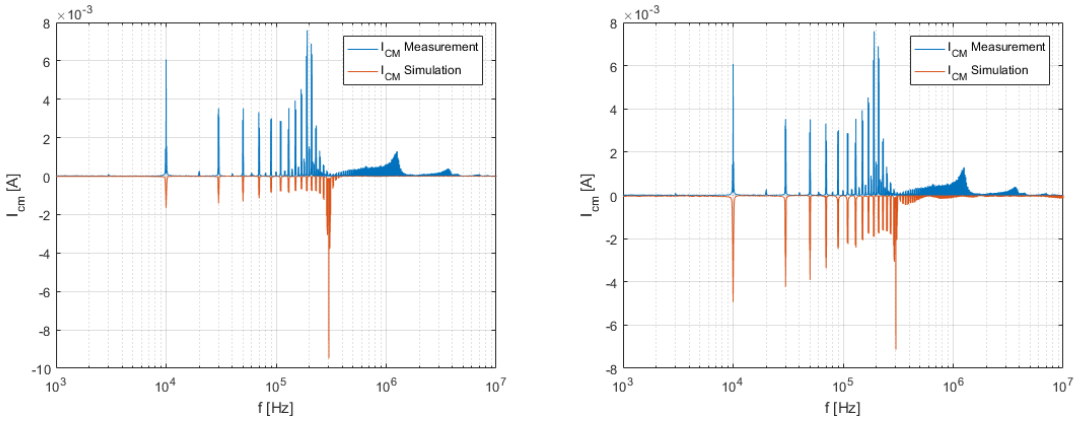
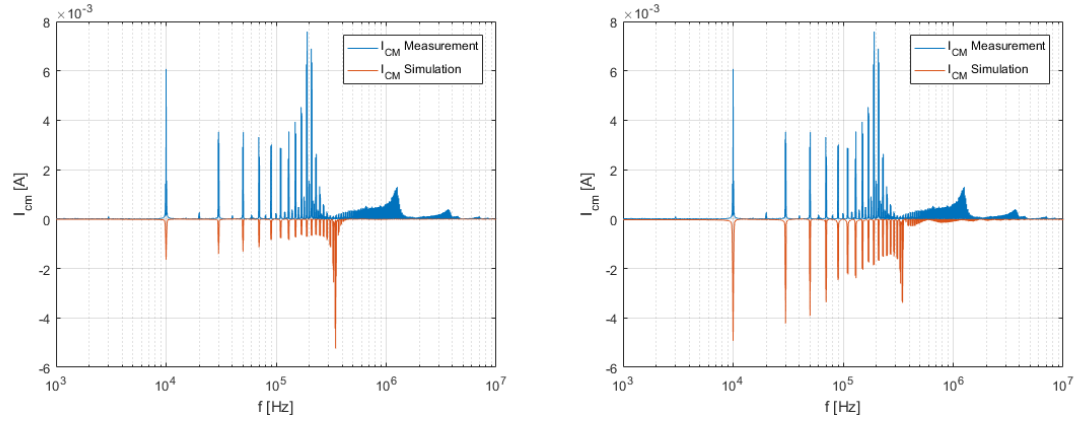


Fig. 12.14: Frequency analysis of the measured CM current for 120 V supply voltage



(a) (b)

Fig. 12.15: Comparison of the measurement and MM simulation of the CM current for 120 V supply voltage



(a) (b)

Fig. 12.16: Comparison of the measurement and CM simulation of the CM current for 120 V supply voltage

12.5 Common-Mode Behavior at 160 V Supply Voltage

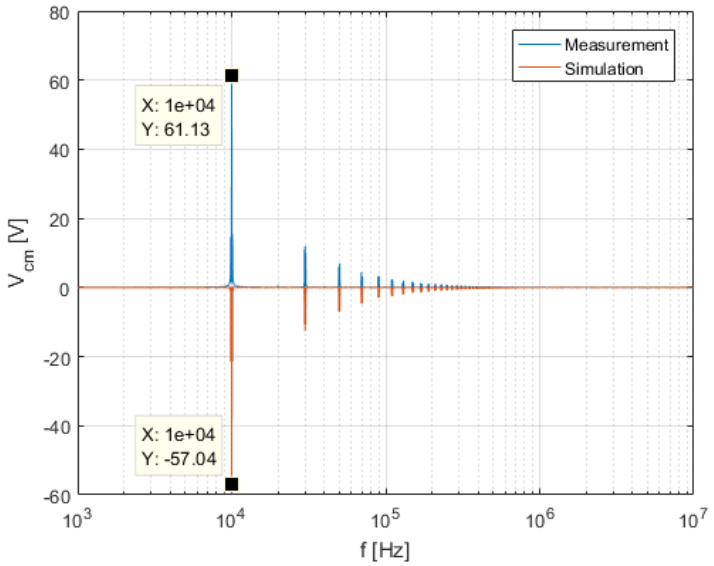


Fig. 12.17: Frequency analysis of measured CM voltage for 160 V supply voltage

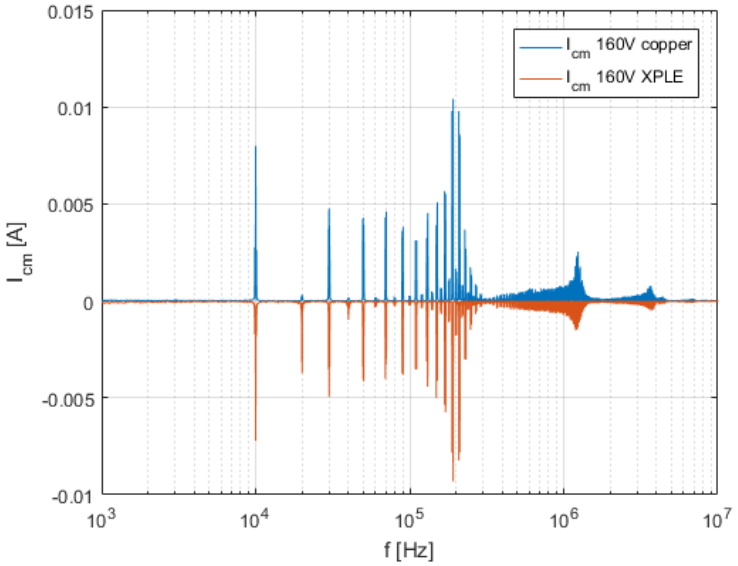
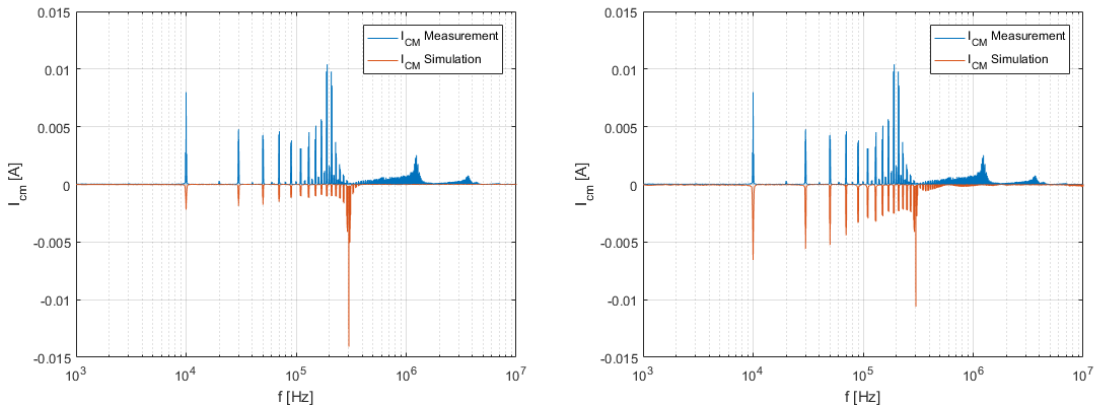
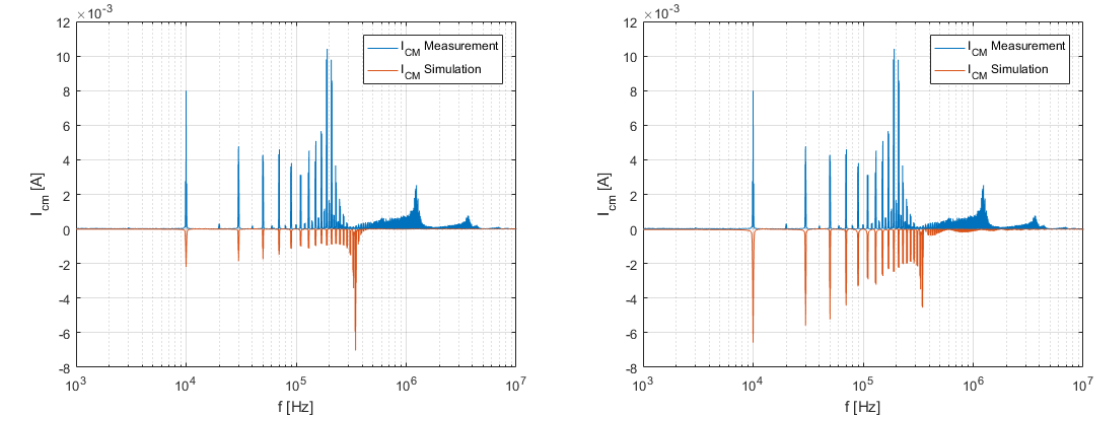


Fig. 12.18: Frequency analysis of the measured CM current for 160 V supply voltage



(a) (b)

Fig. 12.19: Comparison of the measurement and MM simulation of the CM current for 160 V supply voltage



(a) (b)

Fig. 12.20: Comparison of the measurement and CM simulation of the CM current for 160 V supply voltage