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STORED ENERGY MODULATION IN POWER ELECTRONIC CONVERTERS

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1 INTRODUCTION

Power electronics technology has brought high performance, high efficiency, energy savings, high reliability, maintenance-free operation and compactness to many electrical and electronic equipments. Practical applications of power electronics include motor drives, renewable energy systems, electric vehicles, micro-grids and so on [2]. The power density of these power electronic converters has doubled every ten years since 1970s. This can be attributed to the continuous advancement of power semiconductor device technology that allowed the increase in the switching frequencies of power converters. However, the pace of this advancement has slowed down in the recent past leading to exploration of alternative approaches, one of which is explored in this work.

The voltage source type of three phase power converters (VSC) form the workhorse for various motor drives and many other applications. These converters derive their name from the fact that the voltage at the AC terminals of each phase is typically switched between two discrete voltage levels, corresponding to the electrical potentials of the positive and negative DC terminals. This intermediate capacitive dc link terminal of most of the VSC topologies, commonly employ a bulk capacitor, typically featuring a significant amount of dc energy storage to maintain a stiff dc bus. The stiffness of the dc bus is tightly coupled to the output waveform quality, leading to the bulkiness of the dc bus capacitance. In most of the cascaded power converters, the amount of dc energy storage can typically provide several (say, 10-100) cycles of output at the rated power and hence they utilize bulky capacitors in the range of 100-3000μF. Such large amounts of energy storage and capacitance leads to a stiff dc bus, which allows ac waveform synthesis using various modulation approaches such as linear pulse width modulation (PWM). Furthermore, the most common type of capacitors used in such topologies are the electrolytic capacitors. These capacitors have a relatively shorter shelf and service life and higher equivalent series resistance and inductance values, affecting the overall reliability and limiting the high ripple current (or the power throughput) of power converters.

In order to improve the power density of the conversion system, there has been considerable interest in reducing the size of the reactive components in the system by increasing the switching frequency [2, 3]. While this approach leads to reduction of output filter components, it does not necessarily lead to reduction of dc link energy storage requirements. Many other topological alternatives have been proposed to eliminate or reduce the size of the bulky dc link capacitor. Some examples include matrix converters, converters in discontinuous conduction mode of operation, ac link converters and so on. While matrix converters do

not have a bulk dc capacitor, they have had low market penetration since their inception because of being silicon intensive and having commutation issues [4]. Alternatively, in the recent past, the approach of low energy storage at the link has been adopted in current source converters operating in discontinuous conduction mode [5] and ac-link power converters which employ an L - C link at the converter bus [6]. Since these topologies are either current source or consist of an ac link, they use at least double the number of switches and/or diodes as compared to conventional voltage source converters. Furthermore, these approaches impose a much higher voltage and/or current stress on the semiconductor devices of the power converter (typically by a factor of 2-3) leading to increased cost and reliability issues.

The proposed stored energy modulation (SEM) approach is primarily aimed to maintain a stiff dc bus as well as synthesize high quality waveforms, but without employing large energy storage. The proposed approach determines the switching intervals of the various solid state switching devices in an integrated fashion and places them within each switching period in a particular sequence determined by the desired voltage and current waveforms, using an intelligent controller, such that the stiffness of the DC link can be maintained without large amounts of energy storage. There are several advantages of implementing this idea. The size of the required DC link bulky can be reduced by several orders of magnitude (1-10μF against 100μF-3000μF). Furthermore, the conventionally used bulky electrolytic capacitors can be replaced with tiny film capacitors. These film capacitors have much higher shelf and service life with lower equivalent resistances, leading to reduced operating losses. The weight, volume, operating efficiencies and costs of the whole system can be significantly reduced. The simulation results, verifying the discussed approach, have been presented in various presentations and publications, in the recent past [7, 8]. This project aims at demonstrating and evaluating this novel idea of *Stored Energy Modulation* (SEM) in the real world. This will comprise of implementing the idea of SEM on one or several experimental setups in the host university's laboratory. Comprehensive analysis and comparison of the proposed approach with the conventional approaches in terms of efficiency and volume will be conducted as a part of the future work (which will be based on the laboratory setup developed in this work) to prove the feasibility of the SEM for the future high density electric machine drives with capacitors as tiny as 1μF vs. 100-3000μF.

The research task of illustrating the idea of SEM can be enumerated into several problem statements as described further.

- Simulation of the SEM concept for the load conditions selected for the laboratory set-up.

- Selection of the various power converter components to design a printed circuit board (PCB)
- Design of the printed circuit board (PCB) using a PCB design software
- Parts soldering, mechanical integration and board assembly
- Selecting the control implementation architecture
- Implementation of the SEM algorithm on a field programmable gate array (FPGA) interfaced to a micro-controller
- Test the setup by isolating various stages
- Run the setup with the proposed SEM concept.

The project report details the above items by describing them in several sections. Section 2 discusses the details of the design topology under study. In Section 3 and Section 4, the details of the plan of the printed circuit board and control platform for the experimental setup are presented. The results of the experimental setup are presented in Section 5. Section 6 concludes the report by summarizing this work and outlining the remaining and future work.

2 POWER CONVERTER TOPOLOGY

The circuit topology of a three-phase ac-ac power converter connected to an ac load, which is adopted in this work, is illustrated in Figure 1. Such a power converter architecture cascades a three-phase ac boost stage to a three-phase ac buck stage with an intermediate capacitive link. Alternatively, a three-phase ac stage may be replaced by a dc chopper circuit for dc-ac power conversion, as illustrated in Figure 2.

In these topologies, the size of the three phase line inductors follow the typical design norm chosen to feature negligible amount of ripple current. In the case of machine loads, the motor or generator side filtering is normally realized by the machine inductance. On the other hand, use of SEM allows the size of the dc link capacitor C to be orders of magnitude less than traditional designs (1-10μF against 100-3000μF). Since the tiny capacitor C at the link is unidirectional in voltage, the topologies utilize only standard three phase inverter bridges to interface to the two ac sides or dc sides, as illustrated in the figure.

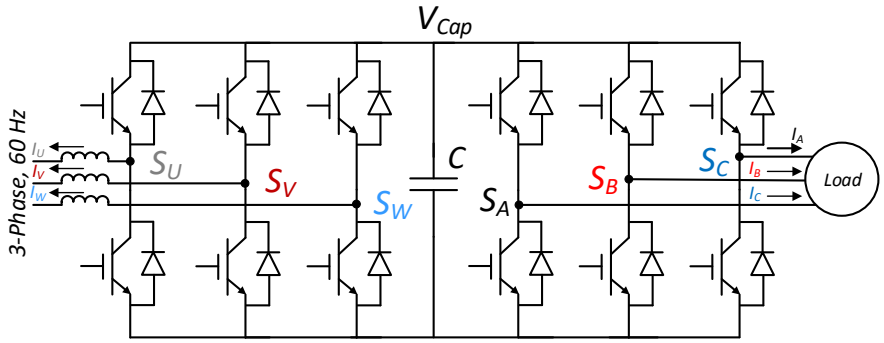

Figure 1: Circuit schematic of an ac-ac power converter with reduced link capacitor and ac source and load

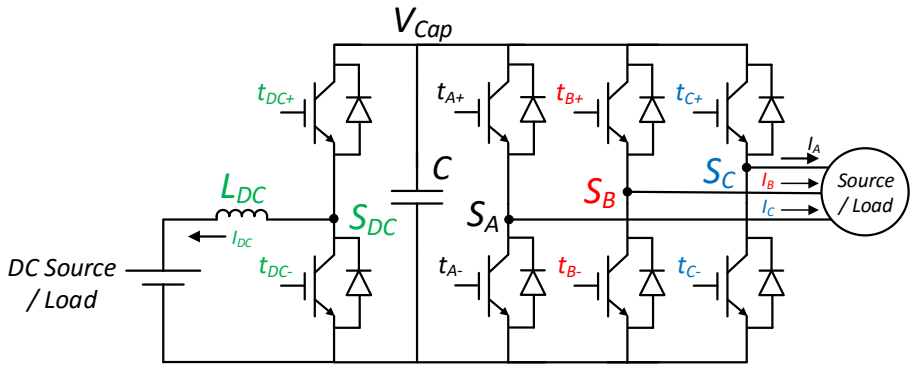

Figure 2: Circuit schematic of an dc-ac power converter with reduced link capacitor and ac source (or load) and load (or source)

Figure 2 illustrates the four-quadrant switch realization of a dc-ac power converter at the dc side. Reduced switch configurations can be incorporated for unidirectional power flow. Such a drive architecture, which comprises of a voltage boost stage, is commonly used for automotive electric traction applications.

Referring to Figure 1, while low cost power converters may have the three-phase active bridge at the input realized using a passive rectifier, stored energy modulation converters require an active front end as shown in the figure. At higher power levels, and in high performance applications specially aerospace and military applications, stringent power quality requirements mandate the use of an active front end interface to obtain sinusoidal input current waveforms as well as improved immunity to input transients such as voltage sags and voltage imbalances.

In the proposed modulation approach, the operation of the converter within each switch-

ing period follows a predetermined energy charge-discharge pattern at the dc link. Further, unlike conventional VSIs, the voltage across the dc link is not stiff. Rather, the capacitor energy, and hence the capacitor voltage V_{Cap}, is several orders of magnitude lesser than required by conventional modulation techniques. The SEM modulator maintains a nominal energy storage, indicated by $\frac{CV_N^2}{2}$, where V_N is the predetermined nominal capacitor voltage and C is the capacitance and C = 1-10μF against 100-3000μF. The typical voltage waveforms across the dc link capacitor in the case of SEM is indicated in Figure 3.

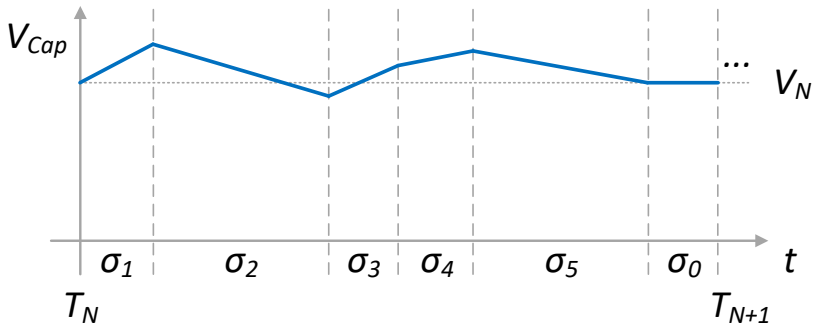

Figure 3: Voltage waveform across the reduced link capacitor of a multi-source multi-load dc-dc power converter with SEM modulation technique

The following discussion briefly illustrates the idea of the proposed modulation approach using a dc-ac inverter example. However, the concepts and techniques introduced here can simply be used to incorporate dc-ac rectifier, ac-ac converter and multi-source multi-load power converters [7, 8].

Every high frequency switching interval can be divided into several sub-intervals, denoted by σ. Assuming a stored energy modulated dc-ac inverter, during a sub-interval, the link capacitor may be charged or discharged from a dc source or an ac load. A dc source requires one sub-interval to charge the capacitor to a predetermined level. On the other hand, a three phase ac load requires two sub-intervals to discharge the capacitor for a predetermined power transfer. Hence, in a dc to three-phase ac system, every high frequency switching cycle consists of at least three active sub-intervals, σ_1, σ_2 and σ_3 and perhaps an idle (inactive) interval σ_0. The dc source can charge the capacitor while the ac load can charge or discharge the capacitor (depending on the ac power factor). Multiple dc and ac sources and loads can be connected to the dc bus capacitor during a particular sub-interval. The state and sequence of connection of these sources and loads to the dc bus can be simplified by reducing the ac sources and/or loads into equivalent sources and/or loads. Another salient feature of the proposed approach may be observed from the capacitor voltage waveform of Figure 3, which remains constant at its regulated nominal value of V_N at the end of every high frequency

switching cycle. These concepts have been proposed and discussed in previous presentations and publications. The author would direct the reader to [7, 8] for the details of SEM.

The following sections discuss the details of the experimental prototype developed in the work in order to prove that SEM can work in an laboratory setting.

3 PRINTED CIRCUIT BOARD DESIGN

This section discusses the design details of the new converter prototype built to run the SEM approach for dc-ac inverter and rectifier operation and ac-ac conversion operation. Altium Designer 17.0 has been used in order to design and layout the PCB board.

3.1 Board Layout

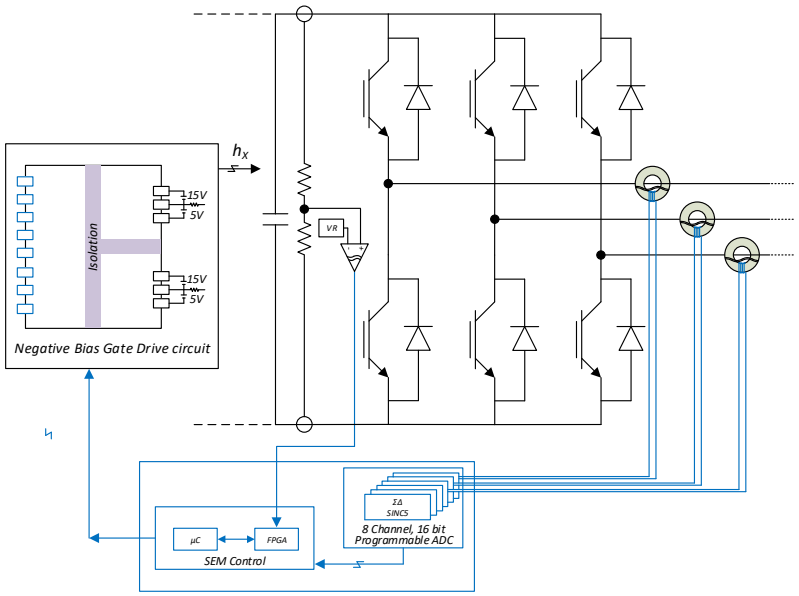

Figure 4: One three-phase ac converter schematic illustrating the gate driver, voltage sensing and current circuitry

The symmetry of the ac-ac converter topology may be observed from Figure 1. Due to the topological similarities in the source and load side ac bridges, Figure 1 may be reduced to Figure 4 for simplicity. The design of one three-phase inverter bridge of the figure may be replicated to arrive at Figure 1. It may also be observed that the three-phase inverter bridge may be reduced to a dc chopper circuit of Figure 2 and hence, may use similar design

rules. Figure 4 illustrates one three-phase ac inverter bridge design. The circuit includes transistor switches with anti-parallel diodes, gate driver circuitry with bipolar output voltages, dc bus voltage sensing circuitry using comparators and isolators, current sensing circuitry, analog-digital chip and the control platform for SEM implementation. The details of these components have been provided in the next few sections.

The circuit design of Figure 4 may further be reduced to Figure 5 wherein the design may be divided into a module board design and a motherboard design. The description of the two boards have been provided herein.

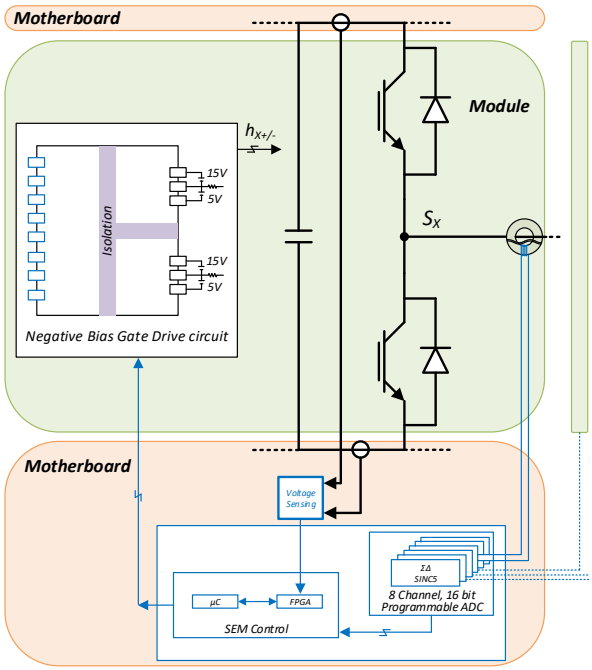

Figure 5: Illustration of the converter module board and motherboard

Converter Module: The module board hosts the transistor devices, anti-parallel diodes, the supporting gate drive circuitry, current sensors for closed loop feedback and a tiny link capacitor. Each module board represents a half-bridge, with its supporting circuitry, which may be used for the dc (or ac) source (or load) side. Hence, there will be several module boards.

Converter Motherboard: The modules may be hosted on another board titled as the *motherboard*. The transistor devices of these modules share the dc bus which is hosted on the motherboard. Along with the power stage, the analog-digital converter chip is also mounted on the motherboard. The motherboard also connects to the control board which processes the ADC outputs and provides the pulse-width modulated signals for the operation of the

transistors in the power stage.

For the current application, the motherboard is capable of hosting up-to seven modules which can be used for ac-dc conversion (which will require 4 module boards), ac-ac conversion (which will require 6 module boards) or dc-ac-ac conversion with multiple sources or loads (which will require 7 module boards). The design specifications of the power ratings of the printed circuit board includes up-to 700V dc bus with 7A of rms current capabilities per half-bridge. The circuit board may be used for up-to 5.5kW of power transfer.

3.2 Component Selection

The various power converter components have been selected from the products available in the market using the datasheet catalogs. These include selection of MOSFET modules, dc link capacitors, gate drivers and so on as per their design ratings. The datasheets of these devices have been studied for their current, voltage, loss, switching frequency, power dissipation limits, accuracy or other capabilities depending on the various components as discussed further.

Silicon Carbide MOSFETs and Diodes

Silicon carbide (SiC) solid state devices are the new commercially available devices which are much faster and more efficient than their traditional silicon counterparts. Furthermore, they are available with attractive voltage (>1700V) and current capabilities. The unique capabilities of these new devices make them superior. However, there are some unique characteristics that need to be considered in order to operate the devices to their full potential.

The controlled switching device selected for the desired application is N-channel enhancement mode SiC Power MOSFET *C3M0065090J* by Cree Inc. [1]. The device is rated upto 900V V_{DCmax} with a continuous rated drain current of 35A at 25°C case temperature. The device features a low impedance package with driver source pin (Kelvin connection) as shown in Figure 6. This eliminates common mode stray inductance in the gate drive path, preventing source degeneration and ringing in the gate loop.

The device, like most semiconductor switches, has high junction to ambient thermal resistance of $R_{\theta JA}$ = 40°C/W which translates into 40°C rise in temperature for every watt of power dissipation. The maximum operating junction temperature of the device is 150°C. Hence, in order to use the device to its full potential, heatsink is a requirement. The semiconductor losses can be estimated using the relevant parameters from the datasheet in order to estimate the size of the heatsink for the devices.

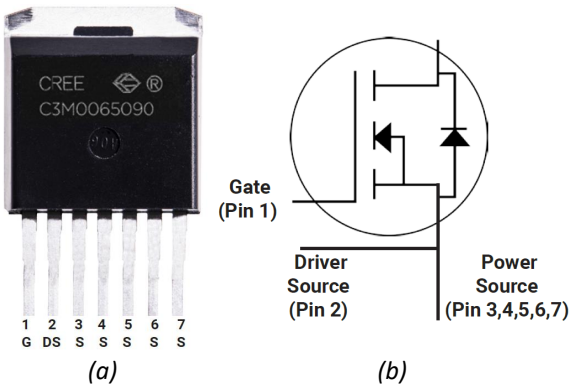

Figure 6: Kelvin connection (a) 7L D2PAK package (b) Equivalent circuit symbol of the MOSFET device [1]

In-spite of high blocking voltages, SiC MOSFETs have a comparatively low R_{DSon} as compared to their counterparts. At the desired operating drain to source RMS current of 7A and gate-source driving voltage $V_{GS} = 15V$, the on-resistance is $62m\Omega$. Hence, the conduction losses in a single SiC MOSFET, P_{cond} , is given by (1).

$$P_{cond} = I_{rms}^2 R_{DCon} = 7^2 \times 62mW = 3W \tag{1}$$

In order to estimate the switching losses at the operating frequency of $20kHz$, the switching energy loss can be obtained for the operating conditions of the device. In order to obtain the fast switching advantage of SiC devices and limit switching losses, low external gate resistances have been used. However, in order to avoid ringing and EMI during the fast switching times, the rise and fall times have been designed to be at-least 10ns. The turn-on gate resistor is designed to be 8Ω for a rise time t_r of $15ns$. This limits the on-energy loss to be within $100\mu J$. On the other hand, the turn-off gate resistor is designed to be 15Ω for a fall time t_r of $12ns$. This limits the off-energy loss to be within $50\mu J$. It may be observed that since MOSFETs do not have a tail current, they can be turned off faster than IGBTs. Hence, the average switching losses in a single SiC MOSFET, P_{sw} , is given by (2).

$$P_{sw} = f_S \frac{E_{on} + E_{off}}{V_{test} I_{test}} V_{op} I_{op} = 20 \frac{(100+50)}{400 \times 20} \times 700 \times 6.3 \times mW = 1.7W \tag{2}$$

where,

$$I_{op} = \frac{2I_{peak}}{\pi} = \frac{2 \times 7\sqrt{2}}{\pi} = 6.3A \tag{3}$$

and, V_{test}, I_{test} are the drain-source voltage and currents during the test operation respec-

tively, V_{op}, I_{op} are the peak operating voltage and averaged operating current of the switching device respectively and f_S is the switching frequency. Hence, the total losses in a single SiC MOSFET operating at 700V dc bus and 10A peak current is estimated to be 4.7W.

The surface mount heat sink 7106 by *Aavid Thermalloy* for D^2PAK TO-263 package removes the heat indirectly without direct contact [9]. The device and the heat sink are soldered to a modified drain pad. The drain pad is expanded to create a thermal path for heat transfer from the package to the high surface area heat sink. The estimated temperate rise above the ambient temperature for 4.7W heat dissipation is $80°C$. Assuming the ambient temperature $T_{amb} = 25°C$, the junction temperature can be estimated by (4).

$$T_J = R_{\theta JC} \times P_{diss} + T_C + T_A = 1.1°C/W \times 4.7W + T_C + T_A = 110°C \tag{4}$$

The operating junction temperature of the SiC device has to be -55°C to 150°C. Hence, the heat sink is optimally sized to provide for the desired heat transfer out of the device.

The SiC devices need to be driven with a higher gate-source voltage V_{GS} swing. One of the drawbacks of fast switching devices is that the parasitic inductances begin to effect the circuit operation. The parasitic inductances, which can be introduced due to non-ideal PCB layout and long package leads, result in ringing in the gate-source drive path. If the ringing is over the threshold voltage, it can lead to unintended turn-on and shoot-through. Hence, applying a negative bias on the gate driver is an acceptable technique to keep the ringing below the threshold and avoid a false turn-on of the device. The selected SiC switch has a V_{GSmax} of -8V/+19V. In order to reduce the on-resistance R_{DSon}, a high V_{GS} of 15V is selected for the turn-on operation. Due to availability of low-priced off-the-shelf dual dc-dc voltage supplies of +15/-5V, -5V is selected for the turn-off operation. The gate drive circuitry design is discussed in the next section.

In addition to the inherent anti-parallel body diode, SiC based Schottky diode has been added in the power circuit, with every transistor device, in order to reduce ringing and losses associated with forward voltage drops. The device series *IDM10G120C5* are the fifth generation of SiC Schottky diodes by Infineon Technologies [10]. These Schottky diodes have no forward and reverse recovery currents and a low forward voltage drop of 1.5V at 10A forward current. Characterized for high dv/dt ruggedness, they have reduced EMI benefits.

Gate drive circuitry

In order to take the full advantage of the new SiC devices, a new breed of gate drivers are tailored to meet the unique drive characteristics of their advantages. Since these devices have

lower transition times and gate charge (≈ 30nC), they typically tend to have lower switching losses. However, they exhibit higher ringing, requiring the need for good layout practice (discussed in Section 3.3).

The gate driver selected for the current application is $UCC21520$ isolated dual channel IC by Texas Instruments [11]. It is a half-bridge driver with a low propagation delay of 19ns. The dead time can be programmed allowing for change in external gate resistor values, if desired, in order to tune the rise and fall transition times. The input side is isolated from the output drivers by a 5.7kV reinforced isolation barrier. The internal functional isolation between the two drives allows a working voltage of up-to 1.5kV dc bus voltage which provides a safety margin by a factor of 2 for a 700V dc bus design. One of the important selection criteria for the IC is the high common mode transient immunity of the device which is > 100kV/μs. As per the above discussion on switch selection, the desired rise and fall times have been tuned to be ≈ 12-15ns, using the external gate resistors, which will lead to $\frac{0.7kV}{0.012\mu s} = 58kV/\mu s$ (< 100kV/μs CMTI of the gate driver).

The driver can source and sink 4A and 6A peak current respectively. These current capabilities can easily meet the application requirements as shown further. The peak source current of the high or low side gate drive can be calculated as given by (5).

$$I_+ = \frac{V_{DD} - V_F}{R_{NMOS}||R_{OH} + R_{on} + R_{G-int}} = \frac{20 - 0.7}{1.47||5 + 8 + 4.7} = 1.4A \quad (< 4A) \tag{5}$$

where, V_{DD} is the output stage supply, V_F is the nominal forward voltage drop across the diode in series with gate drive resistances, R_{NMOS} and R_{OH} are the impedances across the pull-up structure of the N-channel and P-channel MOSFET across the output stage respectively, R_{on} is the external gate resistance during the turn-on process and R_{G-int} is the internal gate resistance of the selected device. Similarly, the peak sink current of the high or low side gate drive can be calculated as given by (6).

$$I_- = \frac{V_{DD} - V_F}{R_{OL} + R_{off} + R_{G-int}} = \frac{20 - 0.7}{0.55 + 15 + 4.7} = 0.96A \quad (< 6A) \tag{6}$$

R_{OL} is the impedance across the pull-down state across the output stage and R_{off} is the external gate resistance during turn-off process. The device has small propagation delay of 19ns with fast transition times of up-to 7ns (typ.). In order to provide for a negative gate-driver voltage to the SiC devices, bipolar dc supplies are used as shown in Figure 7. The selection criteria for the supplies are discussed later in the report.

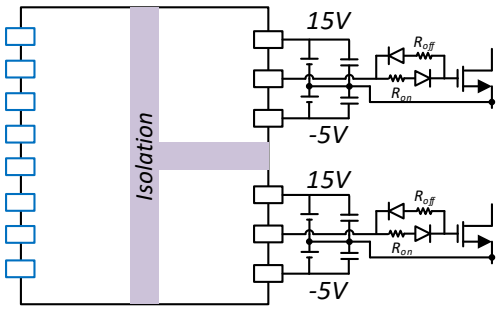

Figure 7: Negative bias with bipolar power supplies

Current sensing circuitry

In order to perform closed loop control, phase current feedback is necessary. Furthermore, since the current sense nodes are connected to the mid-point of the half-bridge which switches between the positive and the negative dc bus, they experience switching transients. Hence, *isolated* current feedback is required. In some applications, isolated current sensors are used which are then cascaded to ADC converters. In other cases, shunt resistors may be used along with isolated amplifiers or isolated ADC converters. A preliminary theoretical analysis with the available products in the market (not presented here) showed that cascading isolated current sensing with ADC converter was more accurate with better performance in areas of high common mode influence and hence was selected as the design choice. Other design choices such as adding a shunt resistor with isolated amplifiers suffered from lower common mode immunity and limited accuracy (with the products available in the market). This section discusses the current sense circuitry. The next section will provide details on ADC conversion circuitry details.

The *CKSR* model of LEM's insulated current transducers has been selected for the desired application [12]. The transducers are based on closed loop *fluxgate* technology providing for contact-free coupling and safe galvanic isolation. In this model, the internal voltage reference is provided on a separate secondary pin which is directly accessible. The application circuit has been designed to provide an external voltage to this reference pin via the ADC which improves the overall accuracy. The device datasheet lists the device to have an overall accuracy of 0.8% at $25^{\circ}C$ (which includes thermal drift effects, gain offsets etc.). The experimental results indicated an accuracy of within 0.2% during testing.

Although the datasheet does not provide an estimated value of coupling capacitance

between the primary side and the galvanically isolated secondary side, it provides some details on the common mode behavior of the device under high dv/dt conditions. Under high dv/dt test conditions of 20kV/μs, a disturbance of less than 250ns is observed. A small RC filter, with a cutoff frequency of about 50kHz, has been added in the circuit for filtering out the noise.

Analog-Digital Converter

An analog-to-digital converter (ADCs) has been included in the design to digitize the analog current sensed by the current sensing circuitry. While ADC conversion may be performed in a micro-controller, an external ADC has also been included as an option. A highly programmable 8-channel 16-bit, simultaneous sampling, $\sum -\Delta$ analog-to-digital converter with sinc5 digital filter, *AD*7761 by Analog Devices, has been selected [13]. The bit depth of the ADC of 16 bits is higher than most micro-controller ADCs. While most micro-controllers have successive-approximation-register (SAR) based technology, an external ADC allows for other suitable architectures such as $\sum -\Delta$. Furthermore, an external ADC can sample simultaneously and is much faster and can be directly connected to an FPGA for processing.

The SAR based ADC architecture determines the digital word by sampling the input signal and using an iterative process. On the other hand, $\sum -\Delta$ ADCs are based on oversampling and digital filtering. In general, $\sum -\Delta$ ADCs are typically high resolution ADCs with higher stability. However, they work at lower speeds as compared to SAR ADCs. The selected device *AD*7761 has an input bandwidth of up-to 110.8kHz with ADC output data rate of 256ksps per channel which meets the conversion rate requirements along with providing higher resolution and low error advantages as shown further.

Allowing for an error of 1% between current sensing and FPGA processing, the 0.8% accuracy of the current sensor leaves only 0.2% error for the ADC conversion. The overall accuracy of the ADC has been calculated by taking into account offset error, gain error, differential nonlinearity error etc. from the datasheet as described further.

- Since the current sense circuitry has a biased output of 0-5V for ac current, only 15 of the 16 bits are used during ADC conversion. 15 bits of accuracy translates into a resolution of 150μV or 0.003% error.
- The differential nonlinearity (DNL) error reveals how far a code is from a neighboring code. The datasheet indicates *no missing codes* which means that as the input voltage is swept over its range, all output combinations will appear at the converter output.

- The integral nonlinearity (INL) is defined as the integral of DNL. The INL error tells the deviation between the measured converter result and the ideal transfer-function value. The datasheet indicates ±1 LSB INL which means the maximum nonlinearity error may be $1/2^{16}$ or 0.0015% error.

- Full-scale error is the difference between the actual value that triggers the transition to full-scale and the ideal analog full-scale transition value. Full-scale error equals offset error (indicating the offset value) + gain error (indicating how well the slope of an actual transfer function matches the slope of the ideal transfer function). The datasheet indicates an offset error of ±1 LSB which means the maximum error may be $1/2^{16}$ or 0.0015% error. The datasheet indicates ±5 LSB gain error which translates into $5/2^{16}$ or 0.0076% error.

- The overall accuracy of the ADC has been calculated to be 0.01% by taking into account 15-bit resolution, DNL, INL and full-scale error which is well within 0.2% error window for ADC.

AD7761 has three independent power supplies with tied reference potentials: two analog circuitry power supplies of 5V (typ.) and one digital circuity power supply of 3.3V (typ.). The presence of two analog power supplies isolates the analog front end, reference input and common-mode output circuitry from the ADC core power supply for increased noise immunity. Three low dropout regulators (LDOs) by Analog Devices, *ADP7118* have been added to the ADC circuitry to provide for the chip's power supply requirements.

The ADC also requires an external clock and voltage reference signal. A 32.768MHz (= MCLK) crystal oscillator and 4.096V voltage reference generator has been selected to meet the functionality. Furthermore, small single pole double throw (SPDT) switches have been added near the ADC chip to program the modulation rate (= MCLK/x where, x = 4, 8 or 32), filter type (wideband filter or sinc5 filter), decimation rate (= x32, x64, x128, x1024), output format type (dedicated pin per channel vs. pin sharing) and so on.

Capacitor selection

The *MKP1848S* series of metalized polypropylene film capacitors by Vishay Intertechnology Inc. have been selected to form the tiny dc link capacitor bus [14]. The dc bus capacitance is distributed between the various modules, providing for a localized capacitance with every half-bridge circuitry. Every half-bridge module has a dc bus capacitance of $2\mu F$. These *slim line*, low building height capacitors allow the modules to be placed close to each other,

reducing the path distance between the individual half bridges. This allows for lower parasitic inductances in the path of the dc bus. The capcitors are rated for 1kVdc with a low self inductance of < 1nH/mm. As compared to the electrolytic capacitors with similar aspect ratios, they have lower ESR (≈ 15mΩ) and higher ripple current capabilities (≈ 4.5A).

Voltage sensing at the DC Bus

The voltage sense circuitry comprises of resistor based voltage divider, comparator, programmable voltage regulator and digital isolator for accurate and noise immune sensing of the dc bus voltage as described further.

In order to accurately scale down the high dc bus voltage, precision non-inductive planar resistors, Slim-Mox series by Ohmite [15], have been used to implement voltage divider circuitry. Rated for 1.5W, these resistors have low tolerance of 0.5%, high operating voltage capabilities and feature <1pF capacitance. Once the dc bus voltage is scaled down by the resistive voltage divider circuitry, it is compared against a reference command voltage. This digital signal is sent to the SEM control algorithm for dc bus voltage regulation as detailed in [7]. Hence, the second stage of the circuitry features an ultra-fast comparator *MAX961* by Maxim Integrated with 4.5ns propagation delay [16]. The IC comprises of fixed internal hysteresis circuitry to counter the parasitic effects and noise. Most high-speed comparators oscillate in the linear region when the voltage on one input is close to or equal to the voltage on the other input. The added hysteresis of the device creates two trip points: one for the rising input voltage and one for the falling input voltage. The difference between the trip points is the hysteresis. When the comparator's input voltages are equal, the hysteresis effectively causes one comparator input voltage to move quickly past the other, thus taking the input out of the region where oscillation occurs.

While one input of the comparator is the scaled dc bus voltage, the other input is provided by a programmable voltage regulator (*SC186* by SEMTECH) with output voltage tolerance of ±1.5% [17]. The IC is programmed using four SPDT switches wherein the regulated output voltage can be varied to be one of the 15 predefined voltages between 0.8V and 3.3V. Hence, the voltage sensing circuitry can be activated at various voltage levels without replacing or adding expensive precision planar resistors.

The final stage of the voltage sense circuitry galvanically isolates the comparator digital signal output from the power section using high CMTI (50kV/μs typ.) digital isolator *MAX12930* [18]. Rated for a maximum data rate of 150Mbps, they feature a typical propagation delay of $\approx 25ns$. This mixed signal voltage sensing circuitry has been designed to meet the voltage sensing requirements of the SEM approach as detailed in [7].

Miscellaneous components

This section briefly discusses other miscellaneous circuit components.

Gate driver supplies: In order to provide negative bias to the controlled switches (Figure 7), bipolar dc-dc power supplies have to be included. The *MGJ2* series of power supplies by Murata Power Solutions are optimized for gate drives. With low coupling capacitances of ≈3pF, they are one of the very few supplies with characterized dv/dt immunity information [19]. Regarding voltage regulation, as is common in similar power supplies, lower than 5% minimum loading results in an increase in output voltages by up-to 1.25 times. While the devices are rated for 2W applications, the steady-state power requirement of the gate drive load circuitry of these devices may violate the minimum load limit. Hence, in order to avoid violation of the positive and negative bias limits of the SiC MOSFETs, a resistive load is added for switch protection. The disadvantage of this approach is that it leads to ≈70mW of steady-state losses per gate driver circuitry. Although low power series of dc-dc converters could be used to reduce these losses, they were not used due to absence of dv/dt immunity testing.

Module to motherboard power connectors: The *IPS1* series of shrouded power connectors by Samtec have been selected to provide for power throughput between the various modules and the motherboard [20]. Each contact of the multi-pin connector is individually shrouded for electrical and mechanical protection and rated for up-to 775Vac/1095Vdc. The current rating per contact is 2.3A. In order to meet the current rating as well as provide for mechanical support, a 20 pin connector is selected.

Module power supply: The CKSR current transducer series, gate drive primary-side supply and gate drive secondary-side bipolar power supplies have been designed to work with a single +5 V power supply. This is a common power supply used in the power electronics world to make working the various other components. Every module board has a dedicated 5V, 1A power supply which meets the safety-limiting supply current and power ratings of the gate driver circuitry and the current sensor circuitry (which includes high current requirements during transient conditions) [21].

Decoupling capacitors: The circuit consists of decoupling capacitors near the various power supplies, LDOs of the ADC etc. These capacitors suppress the high-frequency noise in the power supply signals and are laid-out as close as possible to the respective ICs. These low-ESR low-ESL capacitors are rated to briefly supply power at the correct voltage during voltage slag conditions. In general two different-valued capacitors are placed because some capacitor impedances will be better than others at filtering out certain frequencies of noise.

LEDs, SPDT switches, test points: Various LEDs have been placed with the gate drive circuitry ICs, module power supplies and ADC power supples in order to provide a visual

indication of the working condition of the various components. SPDT switches are connected with many ICs in order to turn them off during ideal modes. Under these conditions, only the small quiescent current is consumed by the circuitry, reducing power consumption. Test points have been connected at various critical circuit paths in order to monitor the state of the test signals.

3.3 Layout Rules

In order to achieve optimum performance for the various PCB components such as SiC modules, gate drivers etc. one must pay close attention to PCB layout. Below are some key points which were considered while routing the PCB boards in Altium Designer.

- Low-ESR and low-ESL capacitors have been connected close to the power supply pins of all the ICS to support high peak currents when turning on and during other transient conditions. Small SMD packages such as 0805 and 1206 are used wherever possible in order to achieve smallest possible footprint solution.
- The PCB copper which connects various power pins to the ICs have been increased without violating minimum clearance distances. It also improves heat dissipation.
- The drain pad of the silicon carbide switches have been modified and extended in order to mount the heat sink for thermal transfer path and easier assembly.
- The routing paths for the module power circuitry connecting the two half-bridge switches to the positive and the negative dc bus, are high surface area solid planes, in order to increase copper and reduce the parasitic ESR and ESL in the high current critical paths.
- In order to confine the high peak currents that charge and discharge the transistor gates to a minimal physical area, the gate driver is placed as close as possible to the transistors This decreases the loop inductance and minimizes noise on the gate terminals of the transistors, avoiding false turn-on/turn-off scenarios. The Kelvin connection package of the SiC switches allow for further reduced loop inductance.
- The turn-on gate driver path is laid-out symmetrical to the turn-off driver path. Due to the critical nature of this signal, the return paths of the signal carrying the return current lie over the original path (on a different layer) in order to reduce parasitic inductance and cross-talk.

- In order to ensure isolation between the primary and secondary side of the gate driver, a PCB cutout is placed in order to prevent any coupling and minimize cross-talk.
- For high-side/low-side configurations of the gate driver, where the two channels of the drivers could operate with a DC-link voltage up to 1500 VDC, another PCB cutout is placed to increase creep-age distance and minimize cross-talk.
- In general, a parallel array of small capacitors is superior to one large capacitor. Parasitic inductance is minimized and so is cost. The solution has been adopted by placing small capacitors in every module.
- The signal connector of the module carries the PWM input signals from the micro-controller and current sensor output signals to the ADC placed on the motherboard. The PWM signals have their dedicated ground pin connection to minimize cross-talk. The output of the current sensor is provided between the output pin and the reference pin of the current sensor. In order to reduce cross-talk and minimize noise in this analog signal, the two paths are routed next to each-other.
- In order to maintain stable operation, the crystal oscillator for the ADC and the LDOs are placed as close as possible to the ADC chip.
- The motherboard is a 4 layer PCB board. While the traces are laid out in the two outer layers, the two inner layers consist of the signal ground layer and the signal power planes. This applies plenty of copper to common connections and helps ensure power flows as effectively as possible with minimal impedance or voltage drop, and that ground return paths are adequate. The ground plane is run over a large section of one layer and can have a positive impact on cross-talk between lines running on an adjacent layer.

The above guidelines provide a brief list of few general rules-of-thumb that were adopted in order to design the circuit boards.

3.4 Board Assembly

The smallest IC to be assembled on the board is a 3mm by 3mm chip. In order to assemble the board, SMD stencil was fabricated along with the board fabrication. The sole purpose of an SMD stencil is to transfer solder paste to a bare circuit board. Applying solder paste using syringes may lead to non-uniform solder paste application. Too much solder paste may

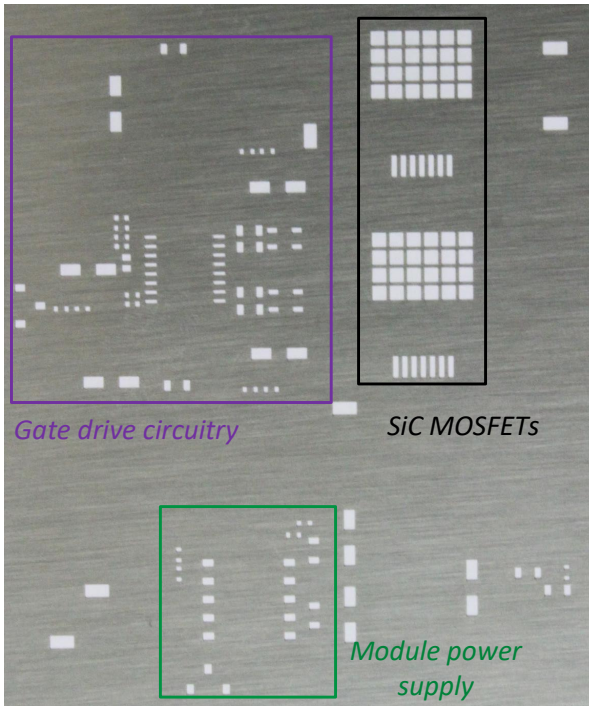

Figure 8: SMD stencil for power module board

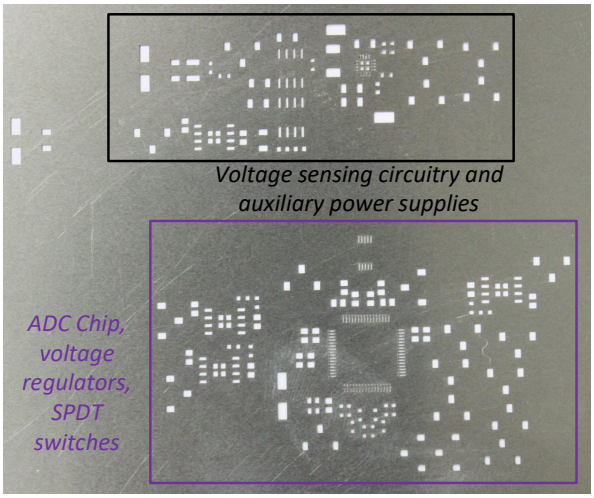

Figure 9: SMD stencil for motherboard

cause solder balling, bridging, and tomb-stoning. A lack of solder paste creates insufficient solder joints. To fabricate a stencil, a stainless steel foil is laser cut creating an opening for every surface mount device on the board. Once the stencil is properly aligned on top of the board, solder paste is applied over the openings. This process, as opposed to hand soldering methods, ensures consistency and saves time, particularly for the surface mount components.

Subsequently, a re-flow oven is used for re-flow soldering of the surface mount electronic components placed after the application of the solder paste. Figure 8 and Figure 9 illustrate the SMD stencils for the module and motherboard respectively. The figures also label the stencil cuts for the various circuitries.

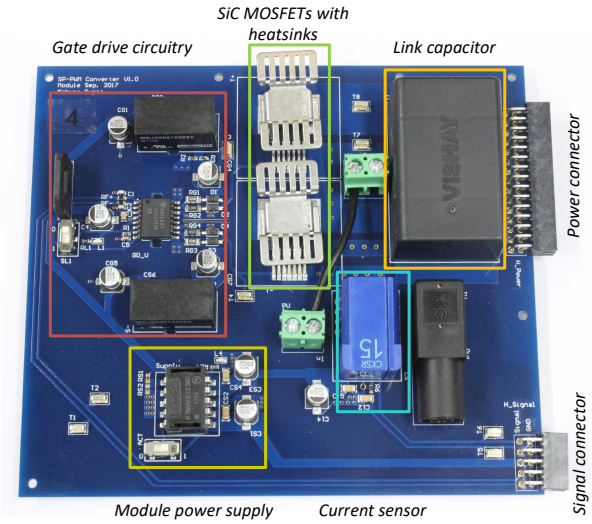

Figure 10: Assembled printed circuit module board

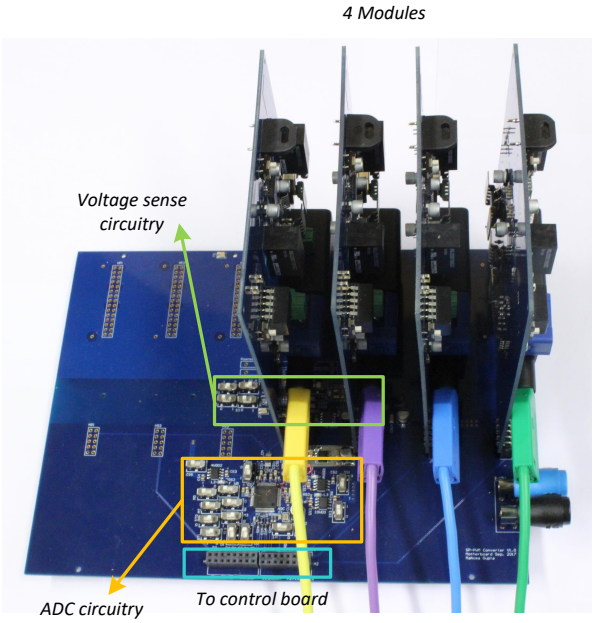

Figure 11: Assembled printed circuit motherboard

Figure 10 and Figure 11 illustrate the assembled printed circuit boards for the module board and the motherboard respectively. The rectangular traces on the figures label the vari-

ous circuitries of the two boards. In Figure 11, four modules are hosted on the motherboard illustrating dc-ac conversion. The motherboard can host up-to seven modules for multiple source-load dc-ac power conversion.

4 CONTROL PLATFORM

Field Programmable Gate Arrays (FPGAs) are semiconductor devices that are based around a matrix of configurable logic blocks (CLBs) connected via programmable interconnects. FPGAs can be reprogrammed to desired application or functionality requirements after manufacturing. They contain an array of programmable logic blocks, and a hierarchy of reconfigurable interconnects that allow the blocks to be programmed, like many logic gates that can be inter-wired in different configurations. Logic blocks can be configured to perform complex combinational functions, or merely simple logic gates like AND and XOR. In most FPGAs, logic blocks also include memory elements, which may be simple flip-flops or more complete blocks of memory [22, 23]. The benefits of the FPGA include the following: faster I/O response times, more computing power of digital signal processors, rapid prototyping, implementing custom functionality and so on [22, 23]. The FPGA configuration is generally specified using a hardware description language (HDL) which includes Verilog, VHDL etc.

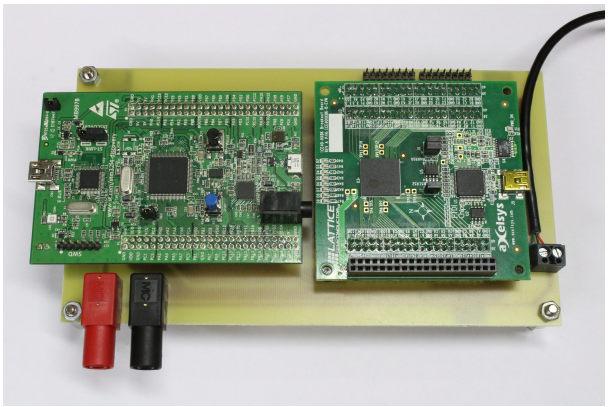

Figure 12: Control platform: FPGA board interfaced with a micro-controller

The approach of stored energy modulation involves non-standard pulse width modulated signals. In order to avail the benefits of FGPAs while implementing the SEM algorithm, a FPGA interfaced to a micro-controller is used. The *iCE40-HX8K* Breakout Board is a simple low-cost board for evaluation and development with the iCE40 FPGA by Lattice Semiconductor [24]. It consists of 7680 programmable logic cells and is equipped with two phase-locked loop units which meets the design requirements. The programming language used for designing FPGA

is VHDL. VHDL stands for *Very High Speed Integrated Circuit Hardware Description Language*. It provides a modern approach to design digital systems and includes combinational or sequential logic design. It implements the digital design in multiple design units as entities and architectures. Further details may be found in [25].

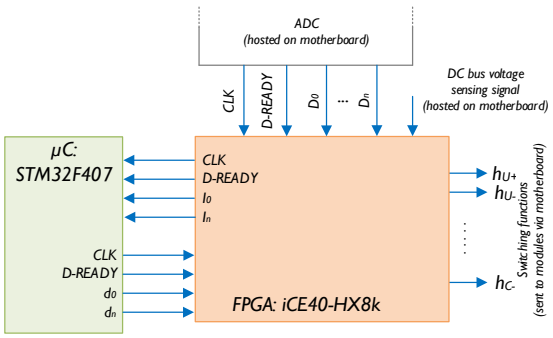

Figure 13: Simplified block diagram of the control architecture

A micro-controller *STM32F407* discovery board by ST Microcontrollers [26] is interfaced with the FPGA to perform mathematical calculations. It is an ARM Cortex M4 based unit which includes a floating-point unit. The programming language used for programming the micro-controller is C. Figure 12 shows the complete control platform used for implementing the proposed algorithm which is connected to the motherboard. While the input to the control board consists of analog-digital converter output signals and dc bus voltage sensing digital signals, the platform outputs pulse-width modulated signals to control the transistor devices and perform stored energy modulation as illustrated by the block diagram of Figure 13.

5 Experimental Results

The proposed algorithm of stored energy modulation has been verified by using a dc-ac photovoltaic inverter example design connected to resistor-inductor (RL) load as described further. The design parameters for a 340W, 85V dc to 70V 3-phase ac boost-buck converter, switching at 20kHz are as follows: $L_{DC} = 10mH$, $L_o = 10mH$ $R_o = 14.5\Omega F$ with a small dc link capacitance of $8\mu F$. The inverter represents a $0.02J$ of energy transfer during each switching period of $50\mu s$, with a nominal energy storage in the dc link of $0.1J$. Although the energy storage is maintained to be about five times the energy throughput, this factor may be reduced for further volume reduction at the penalty of higher ripple voltage. On the other

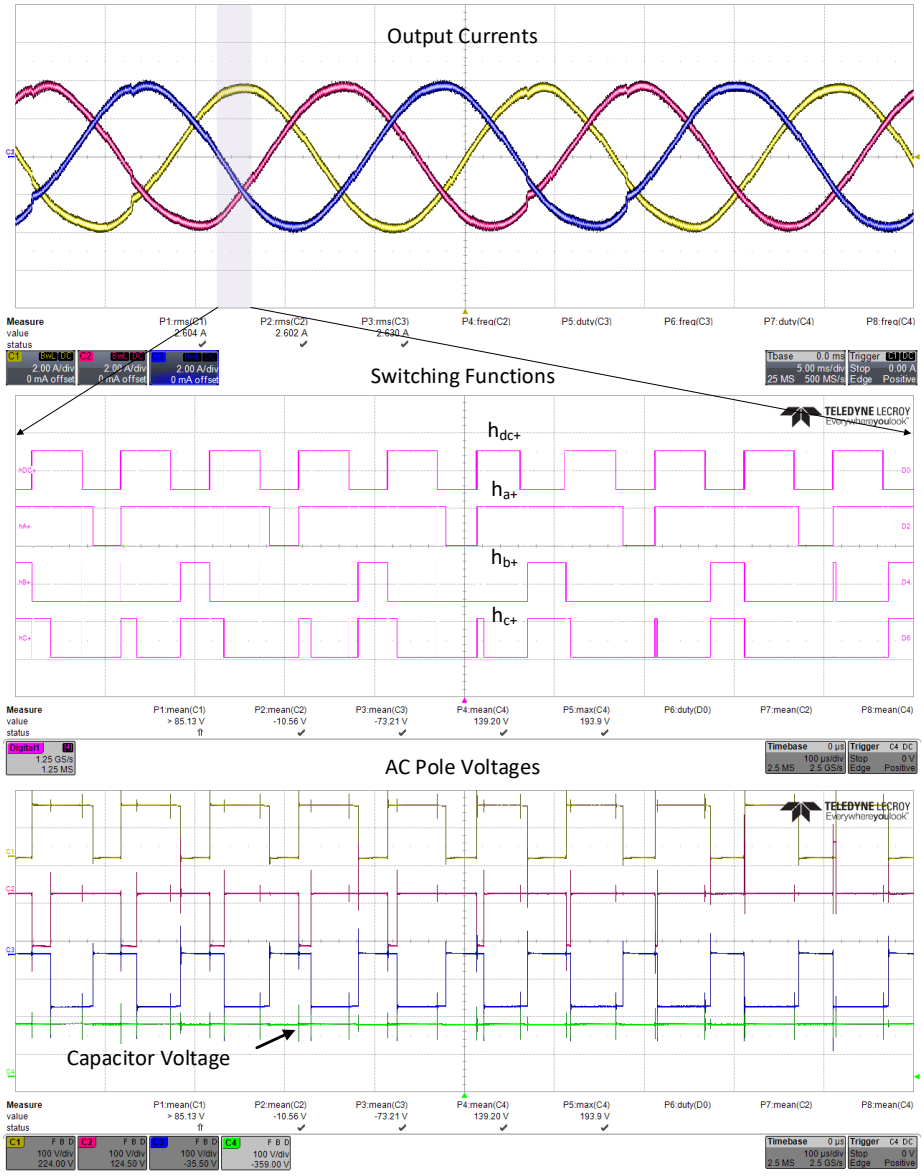

Figure 14: Results from the experimental prototype under 340W, 85Vdc to 3 phase 88Vac testing conditions

hand, this energy storage may be increased to meet the application specifications of minimal energy storage requirement during power outage. The output filter components have been designed to limit the output voltage ripple to within 5%. Selected simulation results are presented in Figure 14. Figure 15 illustrates the experimental setup under testing.

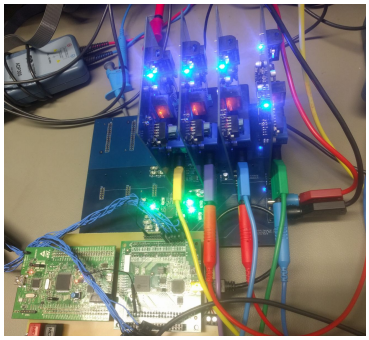

Figure 15: Experimental setup

The top trace of Figure 14 indicates the waveforms of the 3-phase output currents over several cycles of the power frequency of 60Hz. The high quality of the output currents despite of a small link capacitor of 10μF is clearly visible. The figure also indicates the high frequency switching functions h_X which were implemented using micro-controller STM32F407 Discovery board interfaced with FPGA iCE40-HX8k board. Here, $X = dc+, a+, b+$ $c+$ which refer to the top switches of the four half-bridge phase legs. The bottom switch switching functions are complementary to the top switch switching functions and hence are not shown here. The bottom traces of Figure 14 indicate the waveforms of the 3-phase output pole voltages over several switching periods. The well-regulated ripple voltage across the link capacitor can be observed from the green trace. The mapping of the segments of the capacitor voltage to the dc and three phase ac pole voltages can be observed from the pole voltage waveforms. The experimental results presented in this section verify the proposed concept of stored energy modulation for cascaded power converters with stiff but tiny dc link of only 8μF.

6 Conclusion and Future Work

This section presents a summary of the research work, highlighting and discussing the key results.

Conclusion

- The work presents the design of a 5kW AC-DC-AC cascaded power converter prototype with up-to 700V dc bus voltage.
- The key features of the power converter board include the following
  - Fast switching SiC MOSFET devices as controlled switches
  - Negative Bias Gate Drive circuit implementation with Isolated Bipolar Power Supplies
  - Insulated and highly accurate current sensing with CKSR LEM sensors
  - On-board 8 Channel 16 bit Delta-Sigma ADCs for the phase currents
  - DC bus voltage sensing through voltage divider circuitry compatible with the SEM algorithm
  - Stored energy algorithm implementation on FPGA iCE40 HX8k evaluation board interfaced with STM32F4 Discovery micro-controller board
- The experimental results for DC-AC power conversion with passive R-L loads were presented in the final section. These results verify the proposed concept of stored energy modulation for cascaded power converters. The prototype was successfully tested to provide high quality output in-spite of a small dc-link capacitance. The working proof of concept prototype of the proposed SEM technique has been developed by the end of the work.

A list of remaining future work has been identified and presented in the next section. It is primarily based on using the developed prototype for further verification of the proposed SEM technique. The work will be undertaken at the author's home university.

Remaining Future Work

- The list of experiments can be extended to validate and evaluate the following
  - The dynamic performance of the SEM control concept due to changes in load conditions needs to be evaluated using the developed prototype.
  - Implementation of a simple constant V/Hz Induction machine drive using ac-ac conversion will be undertaken.

  - Comparative analysis of the proposed SEM concept with the conventional PWM will be completed.
  - Experimental validation of the failure mode analysis of the SEM based power converters will be undertaken after the analytical work on failure modes.

- Verification of design principles and calculations adopted during PCB layout effects of SiC MOSFETs gate circuitry, parasitic inductances, acceptable ringing levels, overall accuracy of current sensing circuitry, loss measurements, temperature rise estimations etc.
- Since the power converter topology is generic, the circuit board may be adopted for experimental work by other students wherein power converter prototype development is not the primary task.
- The work will be further documented and published for future reference. Experts in the field will be able to read the material and adopt the technology for their application.

7 ACKNOWLEDGMENTS

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