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General Introduction:

The report is based on the research carried out at Graz University of Technology on "Investigation of high frequency bearing currents in five-phase three-level inverter drive systems", with the financial support of the Austrian Marshall Plan Scholarship.

It is mainly divided into four chapters:

Chapter 1: The first chapter reviews the state-of-the-art of the common mode voltage (CMV) in inverter drives. A comprehensive and thorough review of the literature that addresses the CMV issues is reviewed. It covers both two-level and multilevel inverter drives in three-phase and multiphase systems. Much of the work has been presented on three-phase systems, hardly anything on multiphase systems.

Chapter 2: The second chapter discusses the CMV in single ended (SE) inverter systems. It sets forth the definitions, quantifications and characterization of the CMV. Expressions are generalized to include not only two-level three-phase inverter systems, but also multilevel multiphase systems.

Chapter 3: The third chapter of this report represents the findings on the double ended (DE) inverter systems. Double ended systems refer to the configuration in which two inverters (of the same number of levels, in this case) are connected at either end of the stripped open stator winding of an electric machine. The analysis looks at the same/similar characteristics as those in the SE systems.

For chapters 2 and 3, three-phase and five-phase systems were considered and the number of inverter levels that were analyzed is two, three and five. Four control methods are considered for the multilevel systems. These are the phase disposition (PD), phase opposition disposition (POD), alternate phase opposition disposition (APOD) and new carrier based PWM (NCBPWM) methods. They are analyzed to determine how their applications can reduce the number of occurring CMV levels and their frequencies of occurrence. Of the four, the NCBPWM method has all levels existing (present) for SE drives, whereas the others have some of the highest levels (including the maximum and minimum levels, $+v_{dc}/2$ and $- v_{dc}/2$ respectively) eliminated; where v_{dc} is the dc link voltage, being the dc supply of the inverter.

For the two-level inverter, a sinusoidal pulse width modulation (SPWM) method has been employed, and the results are used to compare with the multilevel counterparts.

In the DE systems, it was found out that all the four methods (for multilevel) and the SPWM (for two-level) resulted in reduced number of occurring CMV levels, eliminating the highest, (including the maximum and minimum levels, i.e. $+ v_{dc}$ and $- v_{dc}$ respectively). The total number of occurrences increases twice as much as that of the SE systems for the PD and 2LSPWM, four times for the NCBPWM, and remains the same for the POD and APOD methods.

Chapter 4: The fourth chapter consists of two manuscripts which have been prepared for initial review for journal and/or conference publications. The first paper is on "*On the common mode voltage in multilevel multiphase single- and double-ended diode-clamped voltage source inverter systems*" and will be submitted to the joint issue of Industry Applications Society and Power Electronics Society (IEEE Transactions IAS/PELS Special Issue 2012) in December 2011, whereas the second paper which is titled "*On the influence of different PWM techniques on the occurrence of the different common mode voltage levels in multilevel multiphase single and double-ended diode-clamped VSI systems*" will have its digest submitted to the IEEE Energy Conversion Congress and Exposition (ECCE 2012) in mid January 2012, upon completion with additional measurements in the laboratory in Tennessee Tech.

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Manuscripts submitted for journal and/or conference publications

1. IEEE Transactions IAS/PELS Special Issue 2012: "On the Common Mode Voltage in Multilevel Multiphase Single- and Double-Ended Diode-Clamped Voltage Source Inverter Systems"
2. IEEE ECCE 2012 Conference (with subsequent submission to IEEE Transactions IAS): "On the Influence of Different PWM Techniques on the Occurrence of the Different Common Mode Voltage Levels in Multilevel Multiphase Single and Double-Ended Diode-Clamped VSI Systems"

Chapter 1

LITERATURE REVIEW ON COMMON MODE VOLTAGE IN VOLTAGE SOURCE INVERTERS

1. INTRODUCTION

Due to advance in power electronics, voltage source inverters (VSIs) have been extensively used in electrical drive systems. Different topologies of VSIs have been developed to accomplish the purpose. Mostly, the inverter topologies can be differentiated from each other by classification of the number of levels in the output voltage. The lowest number of levels for a VSI is two and thus, a two-level inverter. As the need for decreasing the harmonic content in the output voltage, less switching frequency, higher efficiency, and lower voltage devices [1] [2], arises, inverters with more number of levels were proposed. There are three-level, four-level, five-level and *n*-level inverters (*n* being the number of levels in the inverter output voltage) [1] [2] [3] [4] [5].

The conventional, existing electrical power system is either a *dc*, or a single- or three-phase *ac* system, and thus limiting the number of phases for the voltage source inverter to three. With the advancement in semiconductor technology, an inverter can be designed to have any number of phases regardless of the existing power system. This has led to *m*-phase systems (with *m* being the number of phases) with more than three phases that are now known as the multi-phase systems. Typically, in these systems, an inverter with more than three phases operates a machine with the same number of phases. These multiphase systems have the advantages of redundancy of the phases such that with one or more phases missing, the system can still be able to perform its function at a reduced power rating. Other advantages are such as the increased torque/ampere (for concentrated stator winding with injection of the harmonic current or voltage), reduction in the motor current harmonics and increased motor efficiency [6] [7] [8] [9]. Multiphase drives find their application in electric ship propulsion, traction (including electric and hybrid electric vehicles) and the concept of 'more-electric' aircraft [6] [7].

With two-level inverters, typically sinusoidal PWM (SPWM) and space vector PWM (SVPWM) control methods are used. The same techniques have also been proposed and used for control of multi-level inverters, with the necessary modifications in the modulation schemes. The most common control techniques for multilevel inverters are phase disposition (PD), phase opposition disposition (POD) and alternate phase opposition disposition (APOD) sinusoidal PWM techniques. Modified space vector PWM techniques for multilevel inverters have also been proposed.

Another type of a multilevel inverter is obtained by having two inverters connected at either end of the load [10] [11] [12] [13] [14] [15] [16] [17] [18] [19] [20] [21] [22] [23] [24]. Such configurations have been named differently in the literature, such as dual-inverter [10] [14] [15], double-ended inverter [24], and open-end inverter [12] [21] [22]. From now on, this type of configuration will be referred to as the "double-ended inverter", except when referring to a particular literature. The resulting voltage across the load is the resultant of the individual inverter voltages and it can be of several levels. In this regard, the analysis of the double-ended inverters will be grouped with the multilevel inverters.

2. REVIEW: HIGH-FREQUENCY COMMON MODE VOLTAGE AND INVERTER-INDUCED BEARING CURRENTS.

Voltage source inverter drives are known to provide a high-frequency (HF) common mode voltage (CMV) at the output of the inverter that also appears – if no additional measures such as CMV filters are used – as a CMV at the input terminals of the electrical motor. As a matter of fact, an *m*-phase electrical machine supplied from a balanced *m*-phase sinusoidal voltage source will have the sum of its phase voltages equal to zero which is not the case with a machine fed from the VSI. This voltage may cause additional electromagnetic interference (EMI), additional charging of the motor cables, additional losses, as well as inverter-induced bearing currents. Such bearing currents may increase the aging rate of the bearings and hence lead to their premature failures [25] [26] [27] [28]. So, in addition to the conventional bearing currents that have been known for a long time [29], the existence of the common mode voltage due to the inverter increases the effects of these currents [25] [26] [27] [28].

The CMV is inherent to the voltage source inverter and typically changes with every switching event. Because of its parasitic effects on the drive, methods have been investigated to reduce or eliminate the CMV, almost since VSIs have started to be more widely used. Two different approaches can be distinguished to achieve this goal.

- Filters that do not eliminate the HF CMV at the inverter output but return it to its source, thereby eliminating its occurrence at the terminals of the electric machine.
- Specially developed modulation and/or control schemes that aim to reduce the number of switching incidences that also entail a change of the CMV and/or the states that result in a rather high level of CMV.

3. COMMON MODE VOLTAGE REDUCTION IN TWO LEVEL INVERTERS

In two-level inverters, several methods have been suggested to reduce/eliminate the CMV [30] [31] [32] [33] [34] [35] [36]. These techniques can mainly be grouped into three categories, namely (i) filters [34] [35], (ii) modulation and control [31] [36] [37] [38], and (iii) filters, modulation and control [30] [32] [33].

By adding an external capacitance to the common mode output of the VSI (modifying the equivalent electro-static circuit of an adjustable speed drive system) [34] the CMV at the motor terminals can be highly attenuated. A so called auxiliary zero state synthesizer (AZSS) [39] is introduced to substantially reduce the generated common mode voltage and thus reducing the common mode current by several orders of magnitude. Modifications are made on the inverter topology as well as the modulation strategy to achieve the desired goals. The zero (null) states responsible for the maximum levels of the CMV to occur $\pm\frac{1}{2}v_{dc}$ are avoided in the modulation strategy. As a result the common mode current is also attenuated. In [35], a common-mode transformer (CMT) and normal-mode filters (NMF's) are used together to reduce the EMI resulting from both the common-mode and normal-mode currents.

Using a modified SVPWM [31], a modulation strategy which reduced the CMV to a constant value of $-\frac{v_{dc}}{6}$ was proposed. This was achieved by allowing any fluctuation of the CMV by

switching only even or only odd states. Using SVPWM method [36], a technique using three adjacent active space vectors to synthesize the output voltage is presented. It avoids using the zero space vectors and thus thereby reduces the peak-to-peak values of the CMV in one PWM cycle. Several techniques on reducing the CMV to the peak-to-peak value of $\frac{1}{3}v_{dc}$ are compared and found out that the dead time and sector transitions cause the actual pea-to-peak value at those instances to be equal to v_{dc} [37]. This is well addressed by proposing a SVPWM modulation technique which takes into consideration the dead time compensation and spikes in CMV at sector transitions and reflected wave compensation. A modulation technique is introduced in [38] to modify the one presented in [37] by extending the range of the modulation index by correctly compensating for the voltage-second distortion caused by the reflected wave compensation. These methods held the peak-to-peak value of the CMV to one third of the *dc* link voltage ($\frac{1}{3}v_{dc}$).

In [30], the CMV is eliminated by adding a fourth leg to the bridge of a three-phase inverter and modifying the modulation strategy to achieve a three-phase star-output neutral-to-ground voltage. In addition, the four-phase LC filter is also included for the purpose of creating the line-to-line voltages across the load. A modified SVPWM was used in this strategy. An active common-noise canceler (ACC) capable of reducing the ground current and conducted EMI is proposed [32]. This ACC superimposes a compensating voltage of the same magnitude and opposite polarity to that of the common-mode voltage and thus cancelling its effect. A common-mode transformer is necessary for this strategy. In [33], a reactor, RC and RLC filters (at the motor terminals and inverter output terminals) are compared. Also their positions in the circuit are a focus on the analysis, whereby the RLC at the inverter output is favored to the other two filters (i.e. reactor and RC).

At this point, it is worth mentioning that two two-level inverters in a double-ended configuration constitute a multilevel system and therefore their discussion is the section on multilevel inverters.

4. COMMON MODE VOLTAGE REDUCTION IN MULTI-LEVEL INVERTERS

As it has been mentioned in the introduction, multilevel inverters have attracted more attention due to the advantages they have over their two-level counterparts. This section is dedicated to the reduction of CMV in this class of inverters, which can be classified into two categories (i) single multilevel inverter drives (SMID) and (ii) double-ended inverter drives (DEID).

Single multilevel inverters (SMID) refer to a drive system containing only one multilevel inverter connected to the stator winding of an electrical machine. The number of levels in the output voltage is greater than or equal to three.

A double-ended inverter drive (DEID) configuration consists of two VSI connected at either side of the open stator winding of the electrical machine. Individual inverters can be of any level, but have to be of the same number of phases as the electrical machine.

On contrast to the work on two-level inverters, where many filters have been proposed, most work on reducing or eliminating the CMV of multi-level inverters has focused on the modulation and/or control scheme used.

4.1 SINGLE MULTILEVEL INVERTER DRIVES (SMID)

Using SVPWM for a three-level diode-clamped PWM inverter, a passive EMI filter which is connected to the ungrounded motor neutral point and uses the stator windings as part of the filter has been proposed in [40][1]. This can be extended to any number levels.

More work on multilevel multiphase inverters can be found in [41] for the elimination of the CMV by using a reduced common mode hysteresis current regulation technique. It employs the difference between the line current errors and the matching of the generated inverter switched states to the reduced states of an ((n+1)/2)-level inverter that ensure zero CMVs. In [42], three SPWM methods, namely, PD, POD and APOD are employed for multilevel inverter control. It is stated that, for a three-phase inverter, the minimum step size of the CMV is $\pm\frac{v_{dc}}{3}$ with the SPWM technique. In PD-SPWM, the CMV of a five-level three-phase inverter is reduced to the step of $\pm\frac{v_{dc}}{12}$ at the crossing of each reference wave with the rising edge of the carrier signal. It further states that the APOD and POD modulation techniques are able to reduce the CMV levels to $\frac{v_{dc}}{12}$ as compared to PD which reduces it to $\pm\frac{v_{dc}}{6}$.

Tests on a medium voltage multilevel inverter drive using SVPWM are presented in [27]. A three-phase three-level neutral-point-clamped (NPC) VSI induction motor drive is used to investigate the CMV. It was shown that at low frequency operation or low modulation index (inner hexagon), the peaks of the resulting CMV were equal to $\pm v_{dc}$, whereas the peaks were equal to $\pm\frac{2}{3}v_{dc}$ for high frequency operation (outer hexagon). Several solutions for motor shaft voltage and bearing currents proposed are such as reducing/eliminating the $\pm v_{com}$ (e.g. using simple double-triangle modulator, solidly grounding the motor neutral etc.), eliminating/reducing coupling from motor stator winding to shaft, eliminating motor shaft voltage by grounding the shaft and eliminating/reducing the motor neutral voltage by redesigning the common-mode circuitry.

In [43], inverters with odd number of levels are considered. By only switching among certain states, zero CMV is generated. Both SPWM and SVPWM are used in the proposed modified schemes that entail zero CMV. For higher number of levels ($n \geq 7$), a modulation strategy for multilevel inverters is proposed in [44] using a selection of the voltage vectors that generate zero CMV at low switching frequency in which the total harmonic distortion, the number of commutations and the linearity are studied. The method works for the number of levels greater than or equal to seven since at lower number of levels the quality of the line currents is significantly affected.

In [45] a new plane called the zero common mode plane is introduced in which medium space vectors are used to eliminate the CMV in the three-level diode clamped three-phase voltage

[1] *Similar to the solutions for two-level three-phase inverters.*

source inverter. An $(n+1)/2$ level imaginary inverter is discussed in [46]. In this technique, the line voltages of an $(n+1)/2$ level inverter are used as the phase voltages of an $n-$level inverter and it works only for odd number of levels. The line voltages of an imaginary inverter are used as the phase voltages of the real inverter and it can be implemented using both SVM and SPWM techniques. A selective carrier based PD modulation technique is used and the CMV is eliminated. Integration of dual-random (random switching frequency (RSF) and random pulse placement (RPP)) and reduced common mode (RCM) PWM techniques for controlling a three-phase three-level NPC inverter drive are discussed in [47]. In [48] a cascaded multilevel inverter (CML) and neutral point clamped (NPC) inverters for medium voltage PWM adjustable speed drive (MV-ASD) systems are analyzed. Modulation strategies to reduce the CMV are also suggested. The configuration for the CML in this analysis makes use of the transformers whose secondary windings have uneven voltage stresses and thus requiring attention during the design stage.

4.2 DOUBLE-ENDED INVERTER DRIVES (DEID):

In [13] a modulation scheme to eliminate the CMV generated by the two individual inverters in the double-ended inverter configuration is proposed. In [23], a dual five-level inverter open-end-winding induction motor drive structure for the three-phase system is used for the simultaneous elimination of the CMV and *dc*-link capacitor voltage imbalance using SPWM and the states that generate zero CMV on the space voltage vectors. The same approach is applied in [18] for a three-level open-end winding induction motor drive and in [19]. More work on CMV reduction/elimination in double-ended inverter configurations is discussed in [16] [22] [49] [15]. In [16], an 8-level inverter is realized by having a four level inverter (from three two-level inverters in cascade) on one side of the stator winding and a two-level inverter on the other side. A SPWM strategy is employed which reduces the switching events as well as the CMV which can be completely eliminated if the voltage vectors selected for the reference vector avoid the states producing it. Using modified SVPWM method by selecting a combination of voltage vectors with zero CMV [22], the CMV is eliminated in the double-ended configuration a dual two-level inverter fed induction motor drive.

5. COMMON MODE VOLTAGE REDUCTION IN MULTI-PHASE MACHINES

Although multiphase machines have received greater attention for the last century, at this point the author is not aware of any work which has addressed the reduction/elimination of CMV in multiphase drives. Most of the available literature is on the modulation and/or control techniques as presented in Appendix C.1. Nevertheless, the analysis presented on the *n*-level three-phase drive systems can be extended to *n*-level *m*-phase drive systems. In light of this, it would be interesting to study how the increase in the number of phases as well as inverter voltage levels affect the step sizes and magnitudes of the CMV.

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APPENDIX

A. MULTILEVEL AND MULTIPHASE DRIVES

Multiphase inverters for variable-speed drives were first proposed in the 1960s [7]. As mentioned in the previous sections, multiphase machines have several advantages over their three-phase counterparts. These include reduction in copper loss and attenuation of phase belt harmonics [50], yield the improvements of efficiency, and reduction in torque pulsation, an improved fault tolerance without additional hardware [51], [52] and reduced power handling requirement for each phase [7], [53]. Multiphase drives find their applications in controlling multiphase brushless machines or multiphase permanent-magnet motors for electrical vehicles and ships and for low-torque propulsion [53]. Using the additional degrees of freedom in multiphase inverters, it is possible to control other multiphase machines independently [54] [55] [56], for example, a multiphase multi-motor system driven by a single voltage source inverter (VSI), the allowable number of motors that can be serially connected in a system depending on the phase number of the motors. More advantages of using multiphase machines are such as low-harmonic current waveforms, low voltage drop cross switches for the same current ratings and relatively low switching frequencies compared with two-level inverters are found in the multilevel inverters [5] [4].

Recently, hysteresis current regulation method [57] has been proposed to drive the multilevel inverters for the improvement of the output voltage on a five-level flying capacitor inverter ensuring balanced capacitor voltages and maintaining the desired current. In direct torque control, multilevel inverters are used to reduce switching losses [58] [59] as they are capable of producing the required voltage by working at low switching frequencies. The techniques were tested for 11-level and 81-level cascaded inverters respectively. To be able to control the multiphase machine, however, the strategy of generating the PWM switching signals for the respective multilevel multiphase inverter used in multiphase machine is a point of interest. In [10] a control method of a six-phase inverter for dual three-phase machines via vector space decomposition is presented. It requires the analysis of three two-dimensional orthogonal subspaces. The concept of multiple *d-q* spaces is discussed in [60] for five-phase non-sinusoidal voltages in which torque per ampere is maximized when multiphase motors have concentrated winding and a non-sinusoidal air-gap flux density distribution. To allow the full usage of voltage levels in multilevel three-phase systems, a harmonically optimal strategy is proposed in [61] by adding a *dc* carrier offset to the reference signal in key lower modulation depths. In [4] a general SVPWM method for over-modulation operation is suggested using a five-level cascaded (H-bridge) inverter.

In [53] a five-level five-phase was used to introduce a multilevel multiphase SVPWM algorithm for converters with switching state redundancy, extending the modulation index and reducing switching losses by minimizing the number of switching. Using a two-level multiphase modulator, a multilevel multiphase modulator with low computational complexity can be realized as discussed in [62].

B. DOUBLE ENDED INVERTER DRIVES (DEID)

Another approach of generating medium and high voltage is using two inverters connected in a double ended configuration for high-power applications. A review of different high-power inverter drives was presented in [11] [12]. Different configurations were introduced to eliminate the inter-phase reactors used to combine the outputs of two inverters to supply large *ac* drives rated at more than several thousands of kilowatts, as these earlier configurations resulted in losses and acoustic noise [11]. In a double-ended inverter drive (DEID) configuration, two electrically isolated *n*-level *m*-phase inverters connected to each end of an open-stator winding of an *m*-phase electrical machine.

The multilevel inverter technology has been widely recognized as a viable solution to overcome the voltage limits of the power switching converters in high-power medium voltage drive systems [14], [17]. Multilevel converters produce voltages with high number of steps and thus a possibility of reducing the harmonic distortion. Such topologies include the diode-clamped, the flying-capacitor, and the cascaded converters [3]. Among the cascaded converters, the dual two-level inverter configuration [14] [17] [3] [24] [21] [20] has received large attention due to simplicity of the power stage.

A space vector based method of synchronized PWM for control of dual inverter-fed motor drives is proposed in [49] with the two inverters being supplied from two separate sources, providing continuous control of power sharing in dependence with the magnitudes of the voltage and the required power ratio between the *dc*-link sources. The switching technique for the similar configuration is also discussed in [15]. The limits of the power sharing as the function of the modulation index is also determined to ensure correct voltage level generation.

Chapter 2

COMMON MODE VOLTAGE IN SINGLE ENDED DIODE-CLAMPED VOLTAGE SOURCE INVERTERS

1. INTRODUCTION

This report summarizes the work on the common mode voltage due to the use of multilevel multiphase inverters. The generated common voltages are compared to those of the two-level three-phase and five-phase voltage source inverters. The voltage levels in the common mode voltage for different inverter levels are determined. The number of occurrences of these levels in one switching cycle (or switching period T_s) when applying several inverter control methods is also determined and compared among the chosen methods.

2. TOPOLOGIES OF THE MULTI-LEVEL INVERTERS, INVERTER CONTROL METHODS AND SCOPE OF THE REPORT

Any n-level inverter has $2(n-1)$ semiconductor switching devices in a leg. The two-level inverter topology is the simplest of all with two semiconductor switching devices per leg. There are different topologies of the multilevel multi-phase inverters. In this report, only diode clamped inverters are considered for both three-level and five-level three-phase and five-phase inverters. In considering the three-level and five-level diode-clamped three-phase and five-phase voltage source inverter, Fig. 1 is chosen as an example to show the configuration of a three-level diode-clamped five-phase voltage source inverter. Independent of the number of phases (m), the number of switching devices is the same in each leg.

Three inverter control (modulation) methods are considered:

(a) Phase Disposition (PD) Method.
(b) Alternate Phase Opposition Disposition (APOD) Method.
(c) Novel Carrier Based PWM (NCBPWM) Method.

All of the above methods are carrier based. For the first two (a) and (b), multicarrier triangular waveforms are used. The number of the carrier signals is equal to $(n-1)$ where n is the number of levels. A modulation signal of desired magnitude and frequency is compared to the carrier signals to produce the switching functions. For the third method, (c), one carrier signal is used. The reference modulation signal of the desired magnitude and frequency is used to reproduce

three modulation signals which are compared to the carrier signal to generate the switching functions.

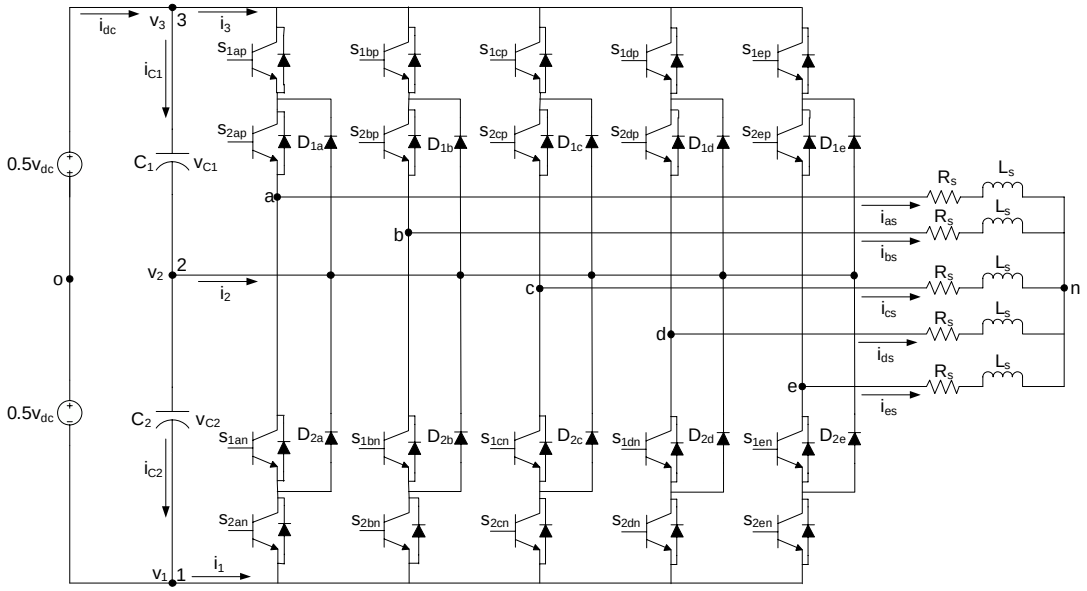

Figure 1: Configuration of a three-level diode-clamped five phase VSI.

3. THEORY OF THE COMMON MODE VOLTAGE

The expressions of common mode voltage, v_{com}, for the three-phase and five-phase voltage source inverters is given by:

$$v_{com} = \frac{1}{3}(v_{ao} + v_{bo} + v_{co}) \tag{1}$$

$$v_{com} = \frac{1}{5}(v_{ao} + v_{bo} + v_{co} + v_{do} + v_{eo}) \tag{2}$$

Where v_{io} $i = (a, b, c, d, e)$ is the pole (or switched voltage). That is the voltage between the phase $'i'$ and the mid-point of the dc source as shown in Figure 1.

For the three-level inverters, the governing equation for the switched voltage is:

$$v_{io} = \frac{(S_i - 1)v_{dc}}{2} \tag{3}$$

Where S_i is the switching function and can take values of 2, 1 and 0 such that: when $S_i = 2$, $v_{io} = \frac{v_{dc}}{2}$; when $S_i = 1$, $v_{io} = 0$ and when $S_i = 0$, $v_{io} = -\frac{v_{dc}}{2}$. These are the three levels of the switched phase voltage obtained from a three-level diode-clamped inverter. An example is given for the one leg of the inverter representing phase 'a' as depicted in Figure 2. When the switches

S_{ap1} and S_{ap2} are on, then $S_a = 2$ and $v_{ao} = \frac{v_{dc}}{2}$; when the switches S_{ap2} and S_{an1} are on, then $S_a = 1$ and $v_{ao} = 0$; when the switches S_{an1} and S_{an2} are on, then $S_a = 0$ and $v_{ao} = -\frac{v_{dc}}{2}$.

For the five-level inverters, the governing equation for the switched voltage is:

$$v_{io} = \frac{(S_i - 2)v_{dc}}{4} \tag{4}$$

Where S_i is the switching function and can take values of 4, 3, 2, 1 and 0 such that: when $S_i = 4$, $v_{io} = \frac{v_{dc}}{2}$; when $S_i = 3$, $v_{io} = \frac{v_{dc}}{4}$, when $S_i = 2$, $v_{io} = 0$, $S_i = 1$, $v_{io} = -\frac{v_{dc}}{4}$ and when $S_i = 0$, $v_{io} = -\frac{v_{dc}}{2}$. These are the five levels of the switched phase voltage obtained from a five-level diode-clamped inverter. When the switches S_{ap1} and S_{ap2} are on, then $S_a = 2$ and $v_{ao} = \frac{v_{dc}}{2}$; when the switches S_{ap2} and S_{an1} are on, then $S_a = 1$ and $v_{ao} = 0$; when the switches S_{an1} and S_{an2} are on, then $S_a = 0$ and $v_{ao} = -\frac{v_{dc}}{2}$.

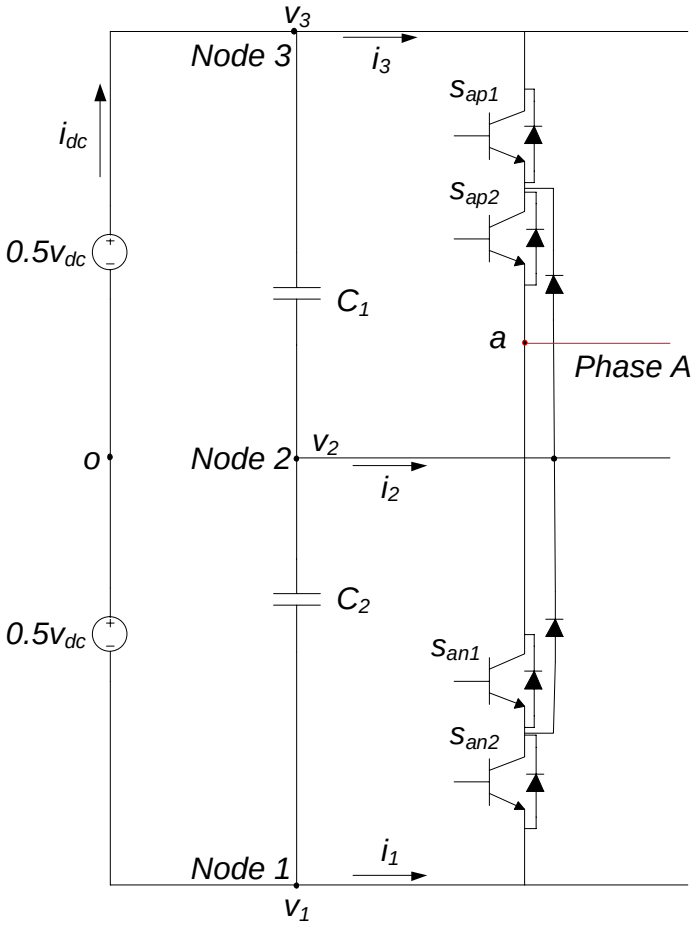

Figure 2: Phase 'a' leg of a three-level five-phase VSI

The combination of the switches when the inverter is controlled will give different levels of the common mode voltage depending on the individual inverter phase output voltages v_{io}, the maximum and minimum levels of the common mode voltage (i.e. $\frac{v_{dc}}{2}$ and $-\frac{v_{dc}}{2}$) occurring when all the output voltages are equal to $\frac{v_{dc}}{2}$ and $-\frac{v_{dc}}{2}$, respectively.

An example of the switching modes for a three-level inverter leg is shown in Fig. 2 for phase 'A'. In Fig. 2, when S_{ap1} and S_{ap2} are on, $S_a = 2$, when S_{ap2} and S_{an1} are on, $S_a = 1$ and when S_{an1} and S_{an2} are on, $S_a = 0$. When these states are substituted in (3), then the three levels of the switched phase voltage are obtained as it has already been described in the preceding section.

4. LEVELS OF VOLTAGES IN THE COMMON MODE VOLTAGE.

The number of possible levels of voltages that can exist in the common mode voltage depend on the number of converter levels *n* and the number of phases *m*. Table 1 shows an example of the number of voltage levels in the common mode voltage $n_0 v_{com}$ and of the step size of the common mode voltage $\Delta_{min} v_{com}$ for the 2, 3 and 5 level inverter configurations in the three-phase and five-phase systems. (Note that positive and negative values are counted separately.)

TABLE 1: Number of possible voltage levels in common mode voltage and the respective step size $\Delta_{min} v_{com}$. (Note that positive and negative values are counted separately.)

Inverter Level (n)	Number of Phases (m)	Number of possible voltage levels in common mode voltage $n_0 v_{com}$	Step size $\Delta_{min} v_{com}$
2	3	$1 \cdot 3 + 1 = 4$	$\frac{v_{dc}}{3}$
2	5	$1 \cdot 5 + 1 = 6$	$\frac{v_{dc}}{5}$
3	3	$2 \cdot 3 + 1 = 7$ (incl. 0)	$\frac{v_{dc}}{6}$
3	5	$2 \cdot 5 + 1 = 11$ (incl. 0)	$\frac{v_{dc}}{10}$
5	3	$4 \cdot 3 + 1 = 13$ (incl. 0)	$\frac{v_{dc}}{12}$
5	5	$4 \cdot 5 + 1 = 21$ (incl. 0)	$\frac{v_{dc}}{20}$

In general,

- **the unit step size of the common mode voltage, $\Delta_{min} v_{com}$ is $\Delta_{min} v_{com} = v_{dc}/[(n\text{-}1)m]$**
- **number of voltage levels in the common mode voltage is $n_0 v_{com} = (n\text{-}1)m + 1$**

The list of voltage levels in the common mode voltage available in three phase and five-phase ac systems for the 2-, 3- and 5-level inverters is presented in Table 2 as follows:

TABLE 2: List of levels in the three-phase and five-phase systems for 2, 3 and 5-level inverters

SN	2-Level		3-Level		5-Level	
	3-Phase	5-Phase	3-Phase	5-Phase	3-Phase	5-Phase
1	$\pm\frac{v_{dc}}{6}$	$\pm\frac{v_{dc}}{10}$	0	0	0	0
2	$\pm\frac{3v_{dc}}{6}$	$\pm\frac{3v_{dc}}{10}$	$\pm\frac{v_{dc}}{6}$	$\pm\frac{v_{dc}}{10}$	$\pm\frac{v_{dc}}{12}$	$\pm\frac{v_{dc}}{20}$
3	-	$\pm\frac{5v_{dc}}{10}$	$\pm\frac{2v_{dc}}{6}$	$\pm\frac{2v_{dc}}{10}$	$\pm\frac{2v_{dc}}{12}$	$\pm\frac{2v_{dc}}{20}$
4	-	-	$\pm\frac{3v_{dc}}{6}$	$\pm\frac{3v_{dc}}{10}$	$\pm\frac{3v_{dc}}{12}$	$\pm\frac{3v_{dc}}{20}$
5	-	-	-	$\pm\frac{4v_{dc}}{10}$	$\pm\frac{4v_{dc}}{12}$	$\pm\frac{4v_{dc}}{20}$
6	-	-	-	$\pm\frac{5v_{dc}}{10}$	$\pm\frac{5v_{dc}}{12}$	$\pm\frac{5v_{dc}}{20}$
7	-	-	-	-	$\pm\frac{6v_{dc}}{12}$	$\pm\frac{6v_{dc}}{20}$
8	-	-	-	-	-	$\pm\frac{7v_{dc}}{20}$
9	-	-	-	-	-	$\pm\frac{8v_{dc}}{20}$
10	-	-	-	-	-	$\pm\frac{9v_{dc}}{20}$
11	-	-	-	-	-	$\pm\frac{10v_{dc}}{20}$

It has already been mentioned that there are several methods used to synthesize the output voltage from the inverter. Table 3 is used to compare the three methods (PD, APOD and NCBPWM) by listing the levels of voltages that will show up in the common mode voltages when used for controlling the three- and five-phase three- and five-level voltage source inverters. (Note that these results can be obtained by inspection, but, more reliably, as it has been done in this work, from the counter of the occurrences presented in the following section.)

TABLE 3: Levels of voltages that available in 3-level and 5-level three-phase and five-phase inverters for different modulation techniques

SN	v_{com} Levels				PD				APOD				NCBPWM			
	3-LEVEL		5-LEVEL		3-PHASE		5-PHASE		3-PHASE		5-PHASE		3-PHASE		5-PHASE	
	3-PHASE	5-PHASE	3-PHASE	5-PHASE	3-Level	5-Level	3-Level	5-Level	3-Level	5-Level	3-Level	5-Level	3-Level	5-Level	3-Level	5-Level
1	0	0	0	0	YES	YES	YES	YES	YES	YES	YES	YES	YES	YES	YES	YES
2	$\pm\frac{v_{dc}}{6}$	$\pm\frac{v_{dc}}{10}$	$\pm\frac{v_{dc}}{12}$	$\pm\frac{v_{dc}}{20}$	YES	YES	YES	YES	YES	YES	YES	YES	YES	YES	YES	YES
3	$\pm\frac{2v_{dc}}{6}$	$\pm\frac{2v_{dc}}{10}$	$\pm\frac{2v_{dc}}{12}$	$\pm\frac{2v_{dc}}{20}$	YES	YES	YES	YES	NO	NO	NO	YES	YES	YES	YES	YES
4	$\pm\frac{3v_{dc}}{6}$	$\pm\frac{3v_{dc}}{10}$	$\pm\frac{3v_{dc}}{12}$	$\pm\frac{3v_{dc}}{20}$	NO	NO	NO	YES	NO	NO	NO	NO	YES	YES	YES	YES
5	-	$\pm\frac{4v_{dc}}{10}$	$\pm\frac{4v_{dc}}{12}$	$\pm\frac{4v_{dc}}{20}$	-	NO	NO	NO	-	NO	NO	NO	-	YES	YES	YES
6	-	$\pm\frac{5v_{dc}}{10}$	$\pm\frac{5v_{dc}}{12}$	$\pm\frac{5v_{dc}}{20}$	-	NO	NO	NO	-	NO	NO	NO	-	YES	YES	YES
7	-	-	$\pm\frac{6v_{dc}}{12}$	$\pm\frac{6v_{dc}}{20}$	-	NO	-	NO	-	NO	-	NO	-	YES	-	YES
8	-	-	-	$\pm\frac{7v_{dc}}{20}$	-	-	-	NO	-	-	-	NO	-	-	-	YES
9	-	-	-	$\pm\frac{8v_{dc}}{20}$	-	-	-	NO	-	-	-	NO	-	-	-	YES
10	-	-	-	$\pm\frac{9v_{dc}}{20}$	-	-	-	NO	-	-	-	NO	-	-	-	YES
11	-	-	-	$\pm\frac{10v_{dc}}{20}$	-	-	-	NO	-	-	-	NO	-	-	-	YES

Three-level three-phase voltage source inverter

Three-level five-phase voltage source inverter

Five-level three-phase voltage source inverter

Five-level five-phase voltage source inverter

5. COUNTER FOR THE OCCURRENCES OF THE DIFFERENT POSSIBLE VOLTAGE LEVELS IN THE COMMON MODE VOLTAGE

Using MATLAB/Simulink, counters were implemented to determine the occurrences of the different levels of v_{com} in the three-level and five-level 3- and 5-phase voltage source inverters. Also the number of transitions from one level to another has been determined.[1]

Fig. 3 shows how the counter for the determination of the occurrences of the different levels of v_{com} in the particular control was implemented.

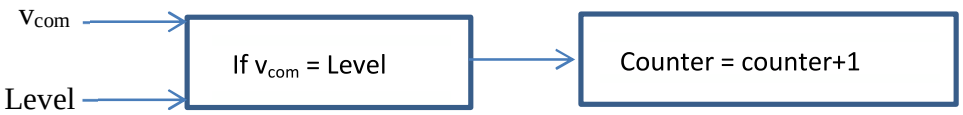

Figure 3: Counter to determine the presence of the particular voltage level in the common mode voltage using the Simulink model.

The following observations were made regarding the number of occurrences of the different levels of the common mode voltage for the three investigated control patterns.

(a) NOVEL CARRIER BASED PWM (NCBPWM)

It has been deduced that in one switching cycle (T_s), all levels, except for the minimum and maximum levels (i.e. $\frac{v_{dc}}{2}$ and $-\frac{v_{dc}}{2}$) occur $\frac{2t_{sim}}{T_s}$ and the minimum and maximum levels occur $\frac{t_{sim}}{T_s}$ times, where, t_{sim} is the total simulation time and T_s is the switching period. (E.g. for a three-level five-phase inverter, the levels 0, $\pm\frac{1}{10}v_{dc}$, $\pm\frac{1}{5}v_{dc}$, $\pm\frac{3}{10}v_{dc}$, and $\pm\frac{2}{5}v_{dc}$ occur $\frac{2t_{sim}}{T_s}$, and the level $\pm\frac{1}{2}v_{dc}$ $\frac{t_{sim}}{T_s}$ times.)

In general, with 1 switching event per device and cycle, 2(*n*-1) devices per leg (phase), there are

2(*n*-1)*m* individual levels of v_{com} generated during one switching cycle (T_s) of an *m*-phase *n*-level inverter.

Except for the minimum and maximum levels of v_{com} (i.e. 2 levels)

all other levels of $n_0 v_{com}$ (i.e. $n_0 v_{com}$ -2) occur two times,

resulting in the 2(*n*-1)*m* individual levels of v_{com}: $2(n_0 v_{com} - 2) + 2 = 2((n-1)m + 1 - 2) + 2 = 2((n-1)m - 1) + 2 = 2(n-1)m$.

[1] For the three-level five-phase inverter, when implementing the counter for the level $\pm\frac{3v_{dc}}{10}$ care must be taken since the MATLAB/Simulink relational operator as well as the logical code failed to detect the existence of these levels. In this particular instance it was decided to multiply both the v_{com} and $\pm\frac{3v_{dc}}{10}$ by $10e^{10}$ before comparing them.

(b) PD & APOD

Although the occurrences of the different voltage levels in the common mode tend to follow a systematic pattern, it has not been possible to generalize their number as it was for the NCBPWM.

Exemplarily, Tables 4 and 5 show the results for one switching cycle for both a three-level and a five-level inverter.

TABLE 4: Number of levels occurrences in a switching cycle in a ***three-level*** inverter:

	3-Level		PD		APOD		NCBPWM	
SN	3-Phase	5-Phase	3-Phase	5-Phase	3-Phase	5-Phase	3-Phase	5-Phase
1	0	0	2	2	3	5	2	2
2	$\pm\frac{v_{dc}}{6}$	$\pm\frac{v_{dc}}{10}$	1.5+1.5=3	2+2=4	1.5+1.5=3	2.5+2.5=5	2+2=4	2+2=4
3	$\pm\frac{2v_{dc}}{6}$	$\pm\frac{2v_{dc}}{10}$	0.5+0.5=1	1.5+1.5=3	-	-	2+2=4	2+2=4
4	$\pm\frac{3v_{dc}}{6}$	$\pm\frac{3v_{dc}}{10}$	0	1	-	-	1 + 1 = 2	2+2=4
5	-	$\pm\frac{4v_{dc}}{10}$		-	-	-		2+2=4
6	-	$\pm\frac{5v_{dc}}{10}$		-	-	-		1+1=2
			$\sum 2\cdot3 = 6$	$\sum 2\cdot5 = 10$	$\sum 2\cdot3 = 6$	$\sum 2\cdot5 = 10$	$\sum 2\cdot2\cdot3 = 12$	$\sum 2\cdot2\cdot5 = 20$

TABLE 5: Number of levels occurrences in a switching cycle in a ***five-level*** inverter:

	5-Level		PD		APOD		NCBPWM	
SN	3-Phase	5-Phase	3-Phase	5-Phase	3-Phase	5-Phase	3-Phase	5-Phase
1	0	0	2	2	3	2	2	2
2	$\pm\frac{v_{dc}}{12}$	$\pm\frac{v_{dc}}{20}$	1.5+1.5=3	2+2=4	1.5+1.5=3	2.5+2.5=5	2 + 2 = 4	2 + 2 = 4
3	$\pm\frac{2v_{dc}}{12}$	$\pm\frac{2v_{dc}}{20}$	0.5+0.5=1	1.5+1.5=3	-	1.5+1.5=3	2 + 2 = 4	2 + 2 = 4
4	$\pm\frac{3v_{dc}}{12}$	$\pm\frac{3v_{dc}}{20}$	-	0.5+0.5=1	-	-	2 + 2 = 4	2 + 2 = 4
5	$\pm\frac{4v_{dc}}{12}$	$\pm\frac{4v_{dc}}{20}$	-	-	-	-	2 + 2 = 4	2 + 2 = 4
6	$\pm\frac{5v_{dc}}{12}$	$\pm\frac{5v_{dc}}{20}$	-	-	-	-	2 + 2 = 4	2 + 2 = 4
7	$\pm\frac{6v_{dc}}{12}$	$\pm\frac{6v_{dc}}{20}$	-	-	-	-	1 + 1 = 2	2 + 2 = 4
8	-	$\pm\frac{7v_{dc}}{20}$	-	-	-	-	-	2 + 2 = 4
9	-	$\pm\frac{8v_{dc}}{20}$	-	-	-	-	-	2 + 2 = 4
10	-	$\pm\frac{9v_{dc}}{20}$	-	-	-	-	-	2 + 2 = 4
11	-	$\pm\frac{10v_{dc}}{20}$	-	-	-	-	-	1 + 1 = 2
			$\sum 2\cdot3 = 6$	$\sum 2\cdot5 = 10$	$\sum 2\cdot3 = 6$	$\sum 2\cdot5 = 10$	$\sum 2\cdot4\cdot3 = 24$	$\sum 2\cdot4\cdot5 = 40$

The results for the PD and APOD methods have been obtained by running the simulation for different simulation times related to the switching period. When run at 166.7 Ts, which is equivalent to one cycle of the fundamental waveform (60 Hz system), the average number of occurrences period was obtained. The tables showing the simulation results are attached in the Appendix A (Tables A1 through A8).

(c) SPWM FOR TWO-LEVEL INVERTERS

For the sake of completeness, Table 6 shows the number levels occurrences in the 2-level 3- and 5-phase voltage source inverter when controlled using the Sinusoidal Pulse Width Modulation (SPWM). The tables showing the simulation results are attached in the Appendix A (Tables A9 and A10).

TABLE 6: Number of levels occurrences in a switching cycle in a *two-level* inverter:

	2-Level		SPWM	
SN	3-Phase	5-Phase	3-Phase	5-Phase
1	$\pm\frac{v_{dc}}{6}$	$\pm\frac{v_{dc}}{10}$	1 + 1 = 2	1 + 1 = 2
2	$\pm\frac{3v_{dc}}{6}$	$\pm\frac{3v_{dc}}{10}$	2 + 2 = 4	2 + 2 = 4
3	-	$\pm\frac{5v_{dc}}{10}$	-	2 + 2 = 4
			$\sum 2\cdot3 = 6$	$\sum 2\cdot5 = 10$

From results of the tables in (b) and (c) it can be stated that

the total number of level occurrences in a period is equal to $2m$.

Thus, if the number of occurrences of the voltage level in one fundamental period (T_m) is known, then, the average number of occurrences for each level in a switching period is given by:

$$\boldsymbol{average\ number\ of\ level\ occurence} = \frac{(\boldsymbol{number\ of\ level\ occurences\ in\ one\ fundamental\ period}) * \boldsymbol{T_m}}{\boldsymbol{switching\ period}\ (\boldsymbol{T_s})}$$

Where T_m is the fundamental period of the electrical machine and is given as: $T_m = \frac{1}{f_m}$ with f_m being the fundamental frequency of the electrical machine. The switching period of the inverter, T_s, is given by $T_s = \frac{1}{f_s}$, with f_s being the switching frequency of the inverter.

6. COUNTER FOR THE OCCURRENCES OF THE TRANSITIONS IN THE COMMON MODE VOLTAGE

Fig. 4 shows the counter for determination for the number of transitions from one level of voltage to another. The logic determines the transition at the leading edge.

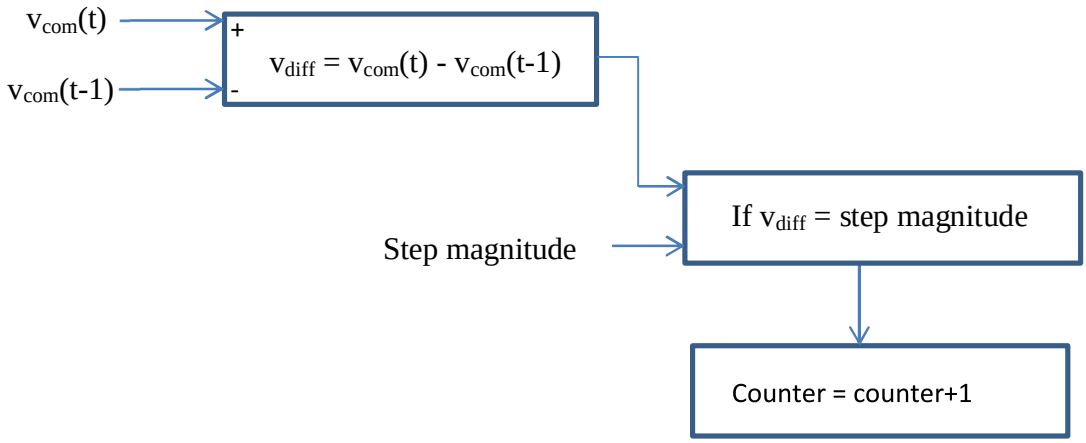

Figure 4: Counter to determine the number of transitions form one level to another in the common mode voltage using the Simulink model.

The following observations were made regarding number of transitions from one level of voltage to another for the three investigated control patterns.

(a) NOVEL CARRIER BASED PWM (NCBPWM)

Only steps of the unit step size $\Delta_{min}v_{com} = v_{dc}/[(n\text{-}1)m]$ exist.

As there are $2(n\text{-}1)m$ individual levels of v_{com} generated during one switching cycle (T_s) of an m-phase n-level inverter, there are also

$2(n\text{-}1)m$ transitions during T_s,

$(n\text{-}1)m$ transitions are by $+\Delta_{min}v_{com}$ $(n\text{-}1)m$ by $-\Delta_{min}v_{com}$.

(I.e. for a three-level five-phase inverter, the number of transitions from one level to another is given by $2\frac{10t_{sim}}{T_s} = \frac{20t_{sim}}{T_s}$. Only the steps of $\frac{v_{dc}}{10}$ do exist.)

(b) PD & APOD

Only steps of the unit step size $\Delta_{min}v_{com} = v_{dc}/[(n\text{-}1)m]$ exist.

From the results of the tables in the Appendix A, it can be generalized that for PD and APOD methods,

the number of transitions are equal to $2m\frac{t_{sim}}{T_s}$,

what is also confirmed in the two tables given in the previous section.

(c) SPWM FOR TWO-LEVEL INVERTERS

Similarly, from the results of tables in the Appendix A, it can be generalized that for SPWM method for 2-level inverters,

the number of transitions are equal to $2m\frac{t_{sim}}{T_s}$.

Figs. 5 through 10 show the transitions of the voltage levels when the switching frequency of 10 kHz, for the input dc link voltage of $v_{dc} = 500V$ for a three-level diode-clamped five-phase voltage source inverter for simulation times $20T_s$ and T_s for NCBPWM, PD and APOD methods. Figs. 11 and 12 show the same results for a 2-level five-phase inverter using SPWM method.

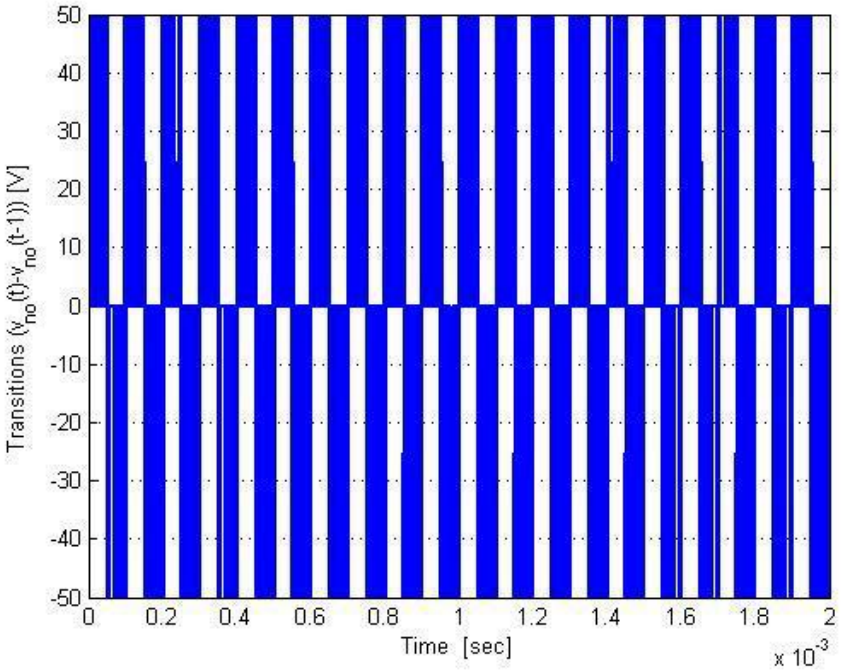

Figure 5: Transitions of the voltage steps in the common mode voltage for a three-level diode-clamped five-phase voltage source inverter, switching frequency of 10 kHz and simulation time of 0.002s = 20 T_s (NCBPWM method).

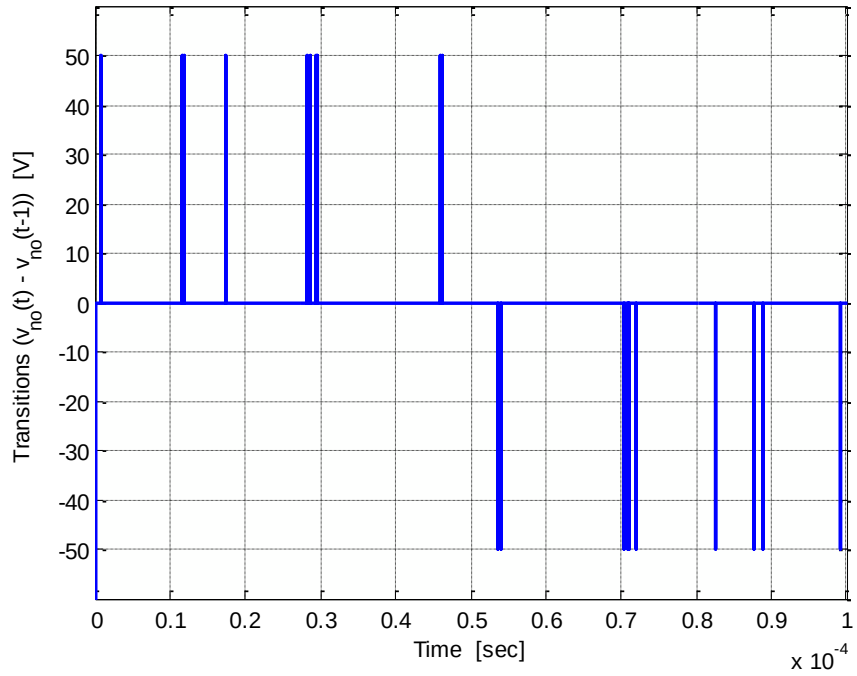

Figure 6: Transitions of the voltage steps in the common mode voltage for a three-level diode-clamped five-phase voltage source inverter, switching frequency of 10 kHz and simulation time of 0.0001s = T_s (NCBPWM method).

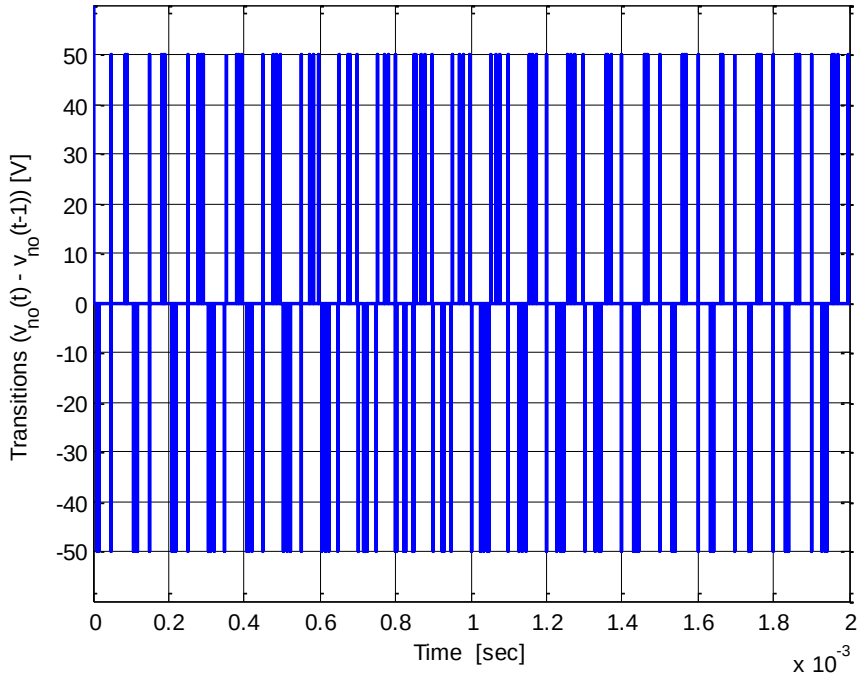

Figure 7: Transitions of the voltage steps in the common mode voltage for a three-level diode-clamped five-phase voltage source inverter, switching frequency of 10 kHz and simulation time of 0.002s = 20 T_s (PD method).

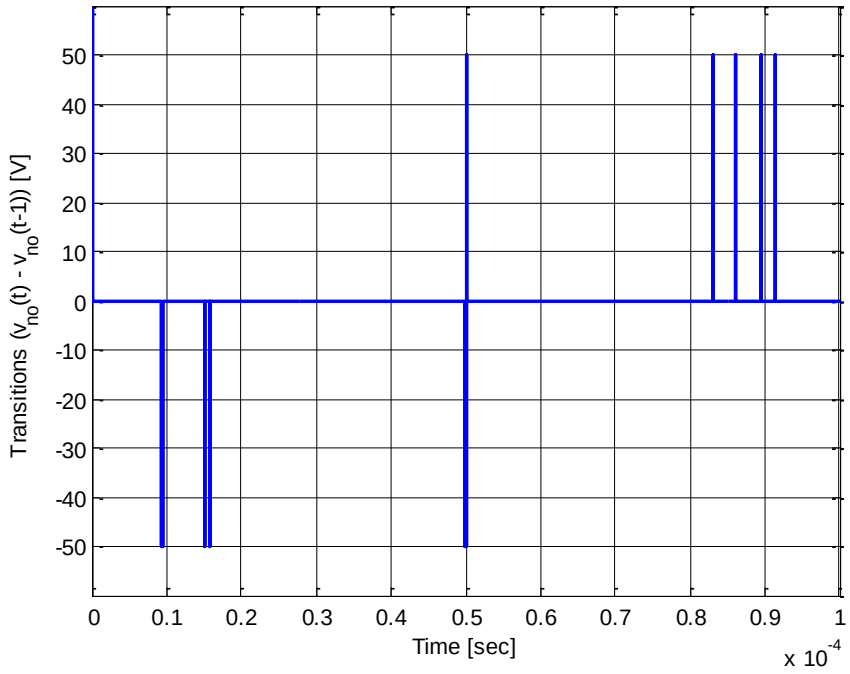

Figure 8: Transitions of the voltage steps in the common mode voltage for a three-level diode-clamped five-phase voltage source inverter, switching frequency of 10 kHz and simulation time of 0.0001s = T_s (PD method).

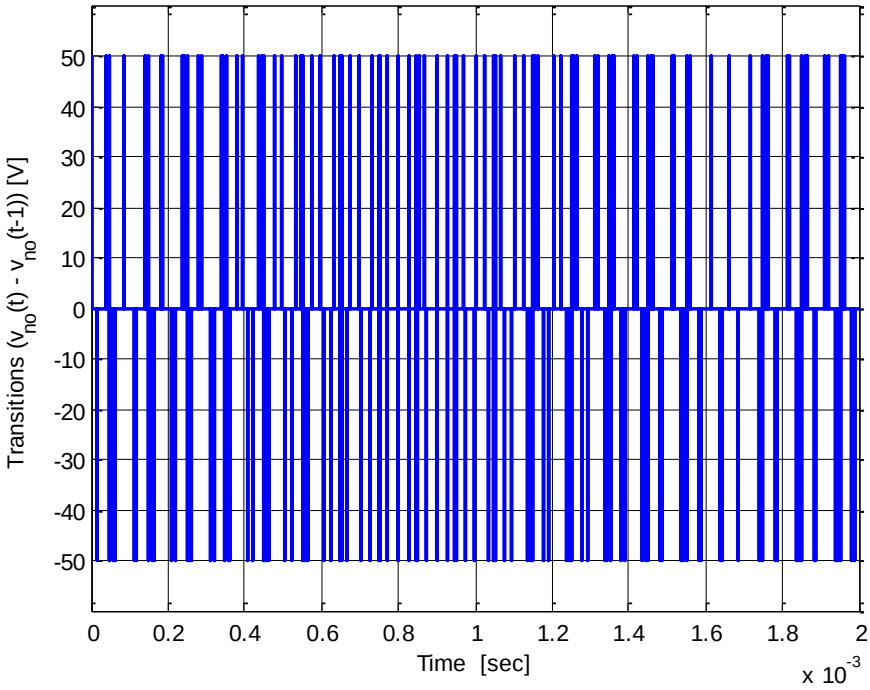

Figure 9: Transitions of the voltage steps in the common mode voltage for a three-level diode-clamped five-phase voltage source inverter, switching frequency of 10 kHz and simulation time of 0.002s = 20 T_s (APOD method).

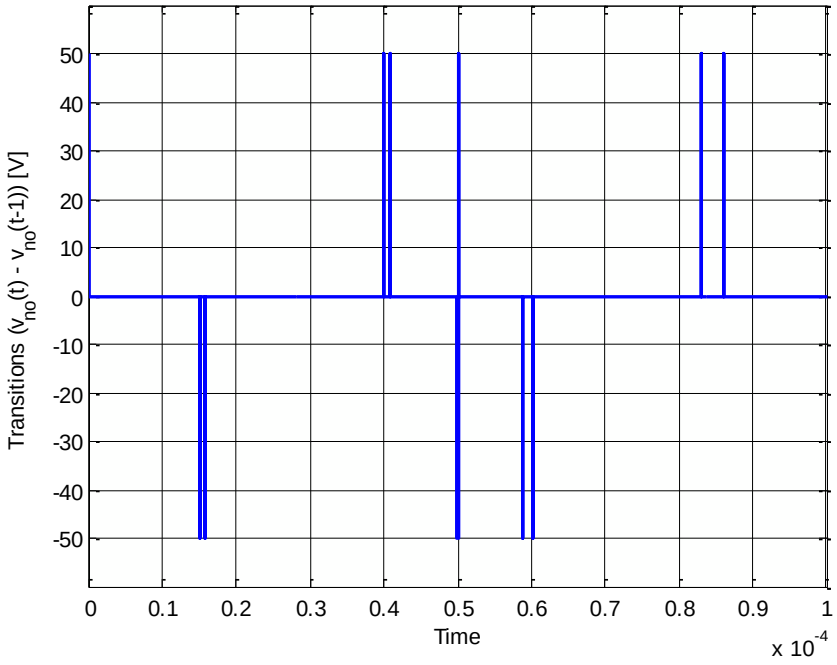

Figure 10: Transitions of the voltage steps in the common mode voltage for a three-level diode-clamped five-phase voltage source inverter, switching frequency of 10 kHz and simulation time of 0.0001s = T_s (APOD method).

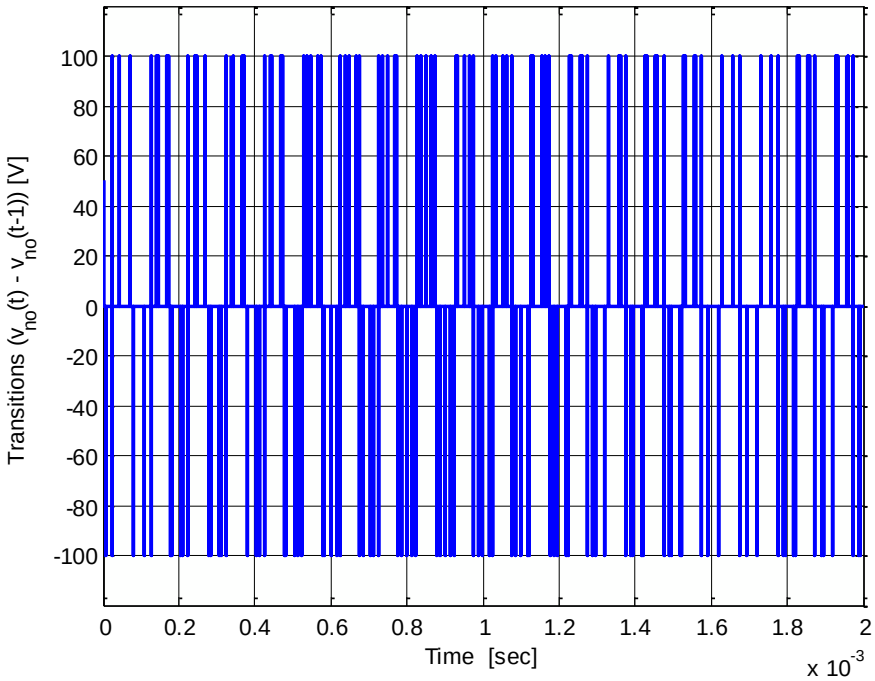

Figure 11: Transitions of the voltage steps in the common mode voltage for a two-level five-phase voltage source inverter, switching frequency of 10 kHz and simulation time of 0.002s = 20 T_s (SPWM method).

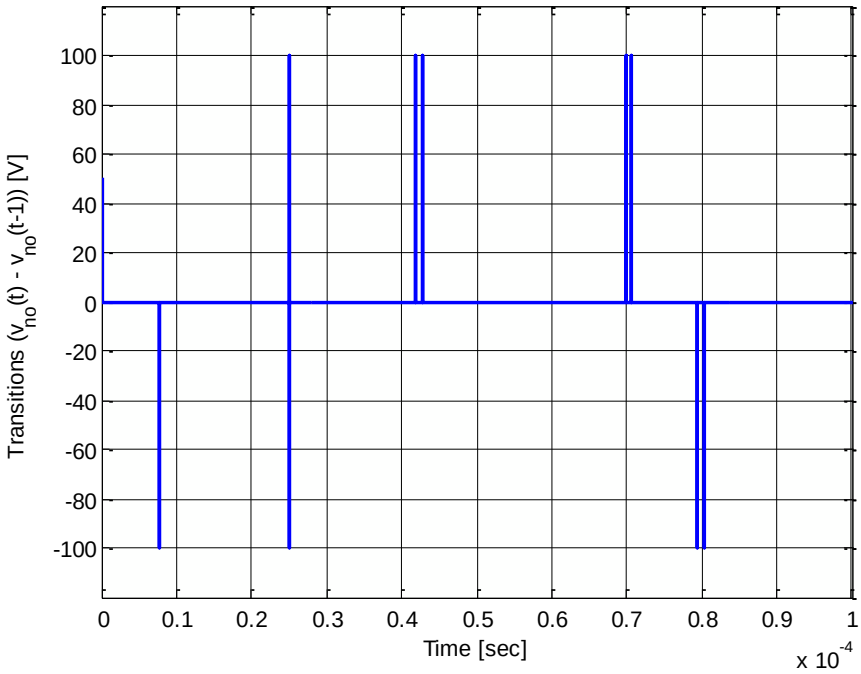

Figure 12: Transitions of the voltage steps in the common mode voltage for a two-level five-phase voltage source inverter, switching frequency of 10 kHz and simulation time of 0.0001s = T_s (SPWM method).

7. RESULTS WAVEFORMS

In the following Figs. 13 through 28, different time intervals in a five-phase voltage source inverter are presented for the common mode voltage for the three investigated sinusoidal PWM methods i.e. the PD, APOD, NCBPWM and also including one for the two level inverter. (Note that the PWM methods converge back to "normal PWM" in the two-level case …). The idea is to show the common pattern for each of the methods on different voltage levels in v_{com}. In Figs. 29 through 34, the common mode voltages are shown for the five-level three-phase and five-phase inverters for the three different control methods.

- The results for Figs. 13 through 28 were obtained using the following data:
  - ✓ The DC link voltage $v_{dc} = 500\ V$.
  - ✓ The switching frequency, $f_{sw} = 10\ kHz$.
- The results for Figs. 29 through 34 were obtained using the following data:
  - ✓ The DC link voltage $v_{dc} = 1\ V$ (or equivalently 1 p.u. with v_{dc} as the base value).
  - ✓ The switching frequency, $f_{sw} = 1\ kHz$.

Figs. 35 through 38 show the common mode voltages for the two-level 3- and 5-phase voltage source inverters.

- The results for Figs. 35 through 36 were obtained using the following data:
  - ✓ The DC link voltage $v_{dc} = 1\ V$ (or equivalently 1 p.u. with v_{dc} as the base value).
  - ✓ The switching frequency, $f_{sw} = 10\ kHz$.
- The results for Figs. 37 through 38 were obtained using the following data:
  - ✓ The DC link voltage $v_{dc} = 1\ V$.
  - ✓ The switching frequency, $f_{sw} = 1\ kHz$.

7.1 Sinusoidal PWM for 2-Level 5-Phase VSI

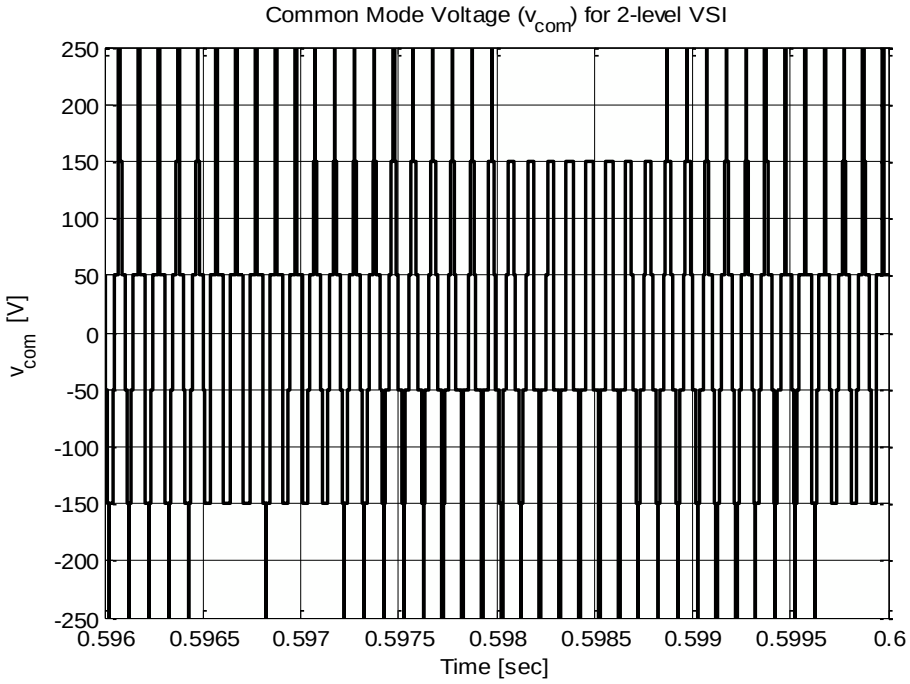

Figure 13: Common mode voltage (v_{com}) for the two-level inverter range 0.596 sec to 0.6 sec.

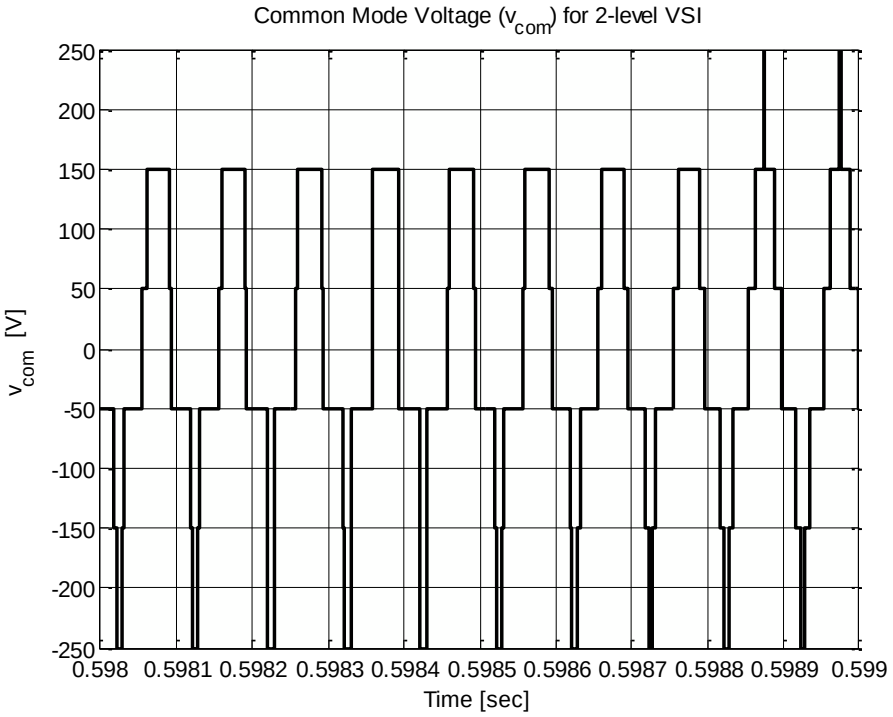

Figure 14: Common mode voltage (v_{com}) for the two-level inverter range 0.598 sec to 0.599 sec.

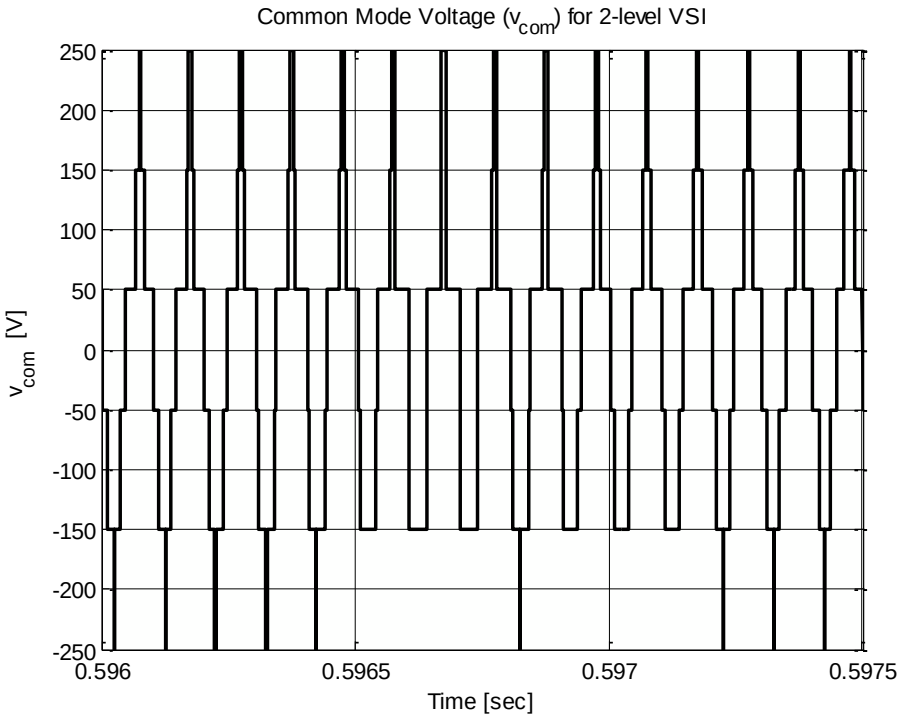

Figure 15: Common mode voltage (v_{com}) for the two-level inverter range 0.596 sec to 0.5975 sec.

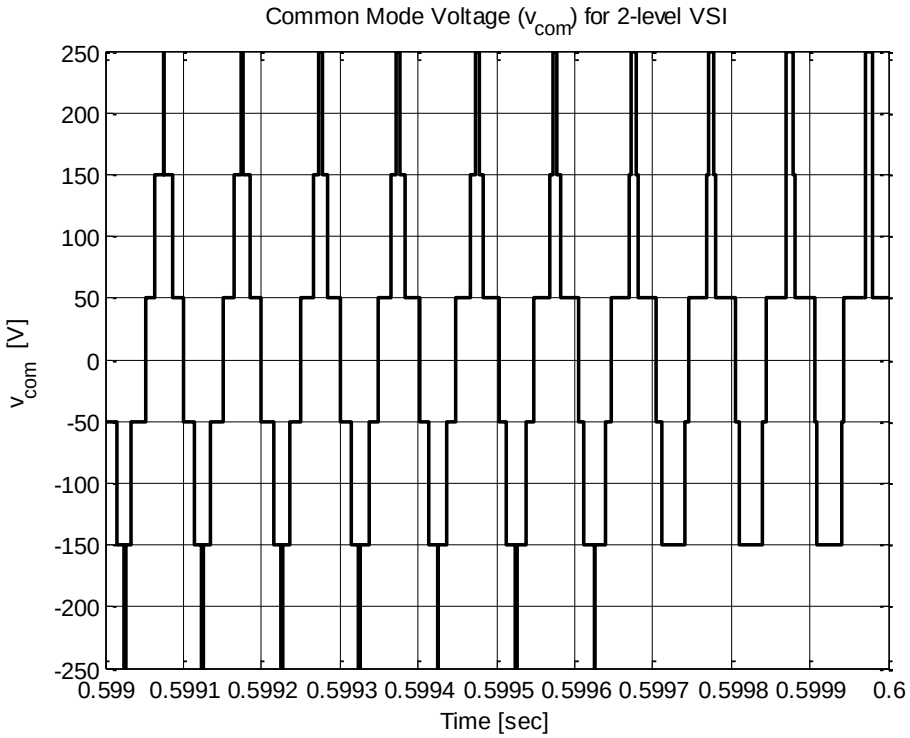

Figure 16: Common mode voltage (v_{com}) for the two-level inverter range 0.599 sec to 0.6 sec.

7.2 Phase Disposition Method for 3-Level 5-Phase VSI

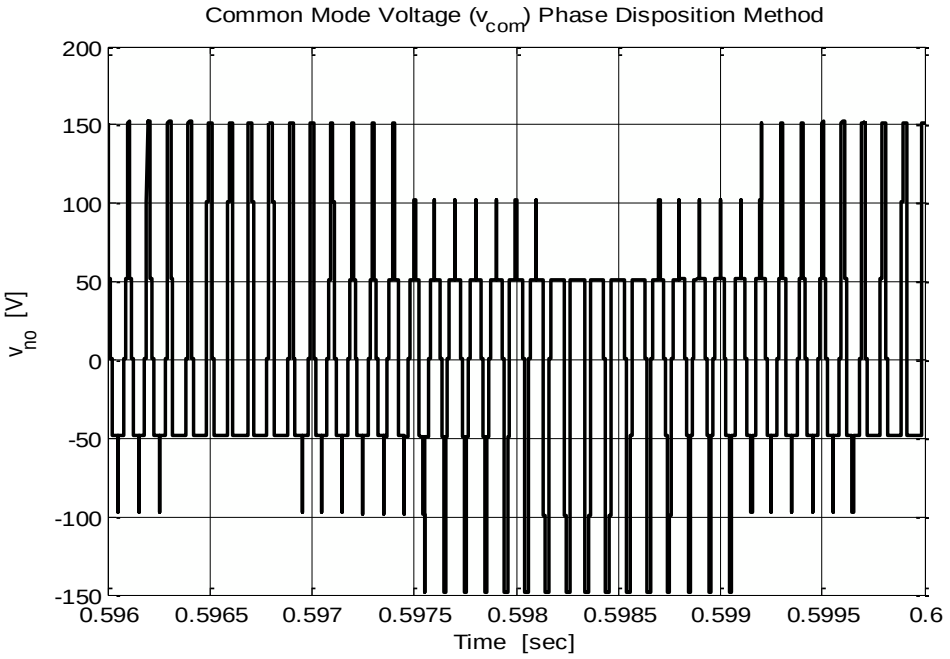

Figure 17: Common mode voltage (v_{com}) for the PD method: time range 0.596 sec to o0.6 sec.

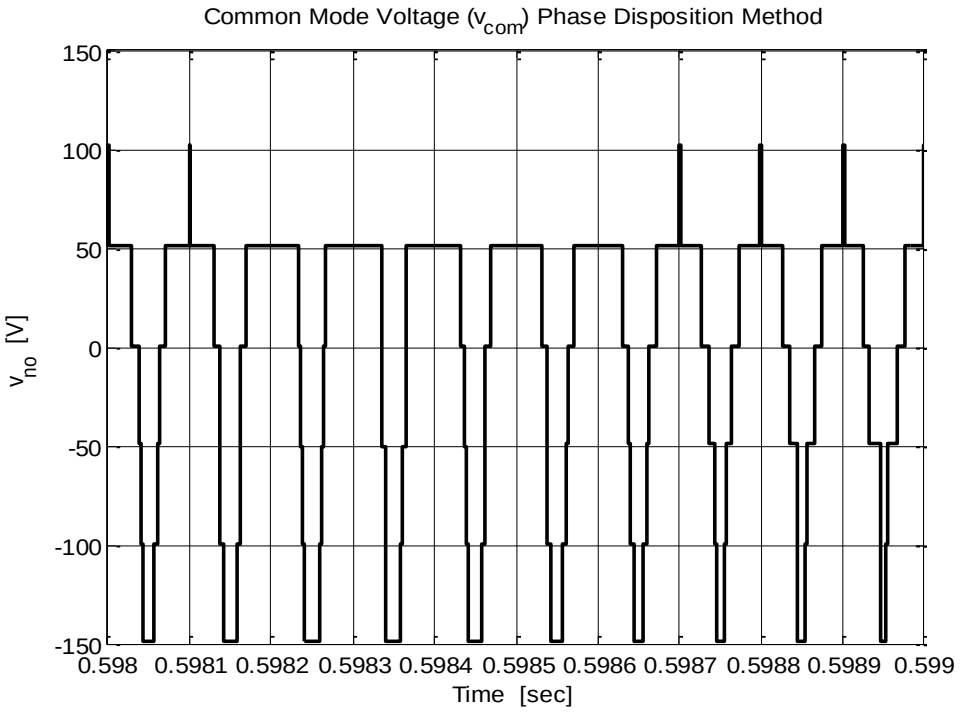

Figure 18: Common mode voltage (v_{com}) for the PD method: time range 0.598 sec to o0.599 sec.

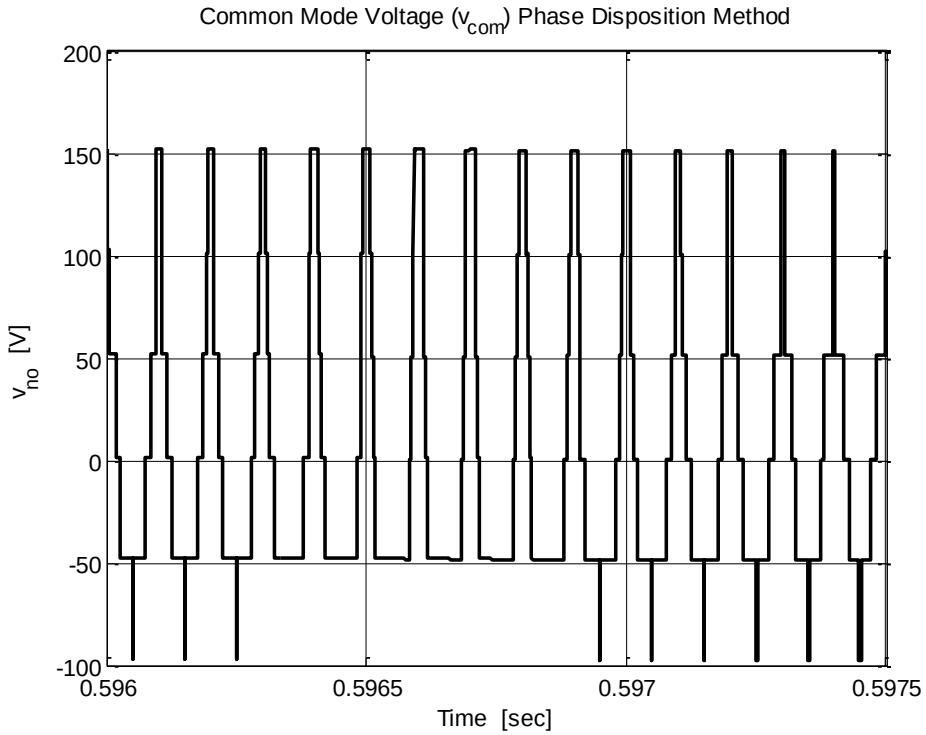

Figure 19: Common mode voltage (v_{com}) for the PD method: time range 0.596 sec to o0.5975 sec.

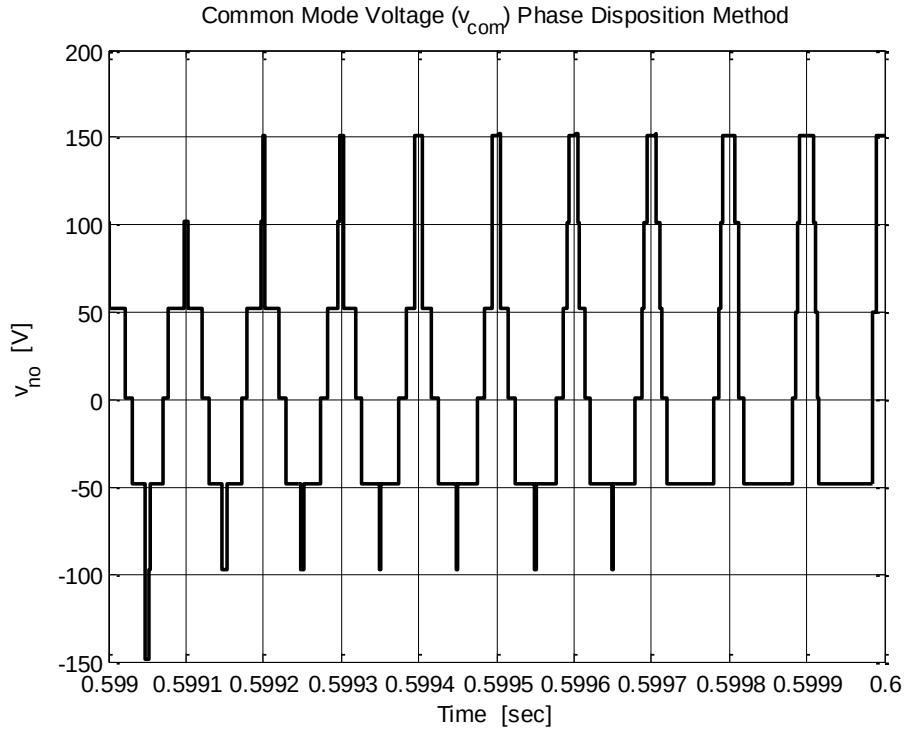

Figure 20: Common mode voltage (v_{com}) for the PD method: time range 0.599 sec to o0.6 sec.

7.3 Alternate Phase Opposition Disposition (APOD) PWM for 3-Level 5-Phase VSI

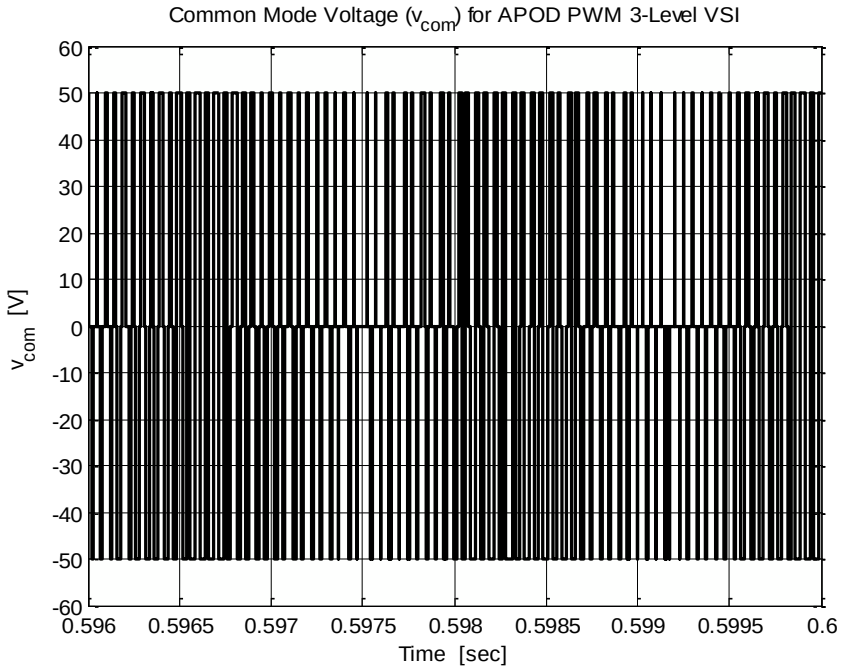

Figure 21: Common mode voltage (v_{com}) for the APOD: time range 0.596 sec to 0.6 sec.

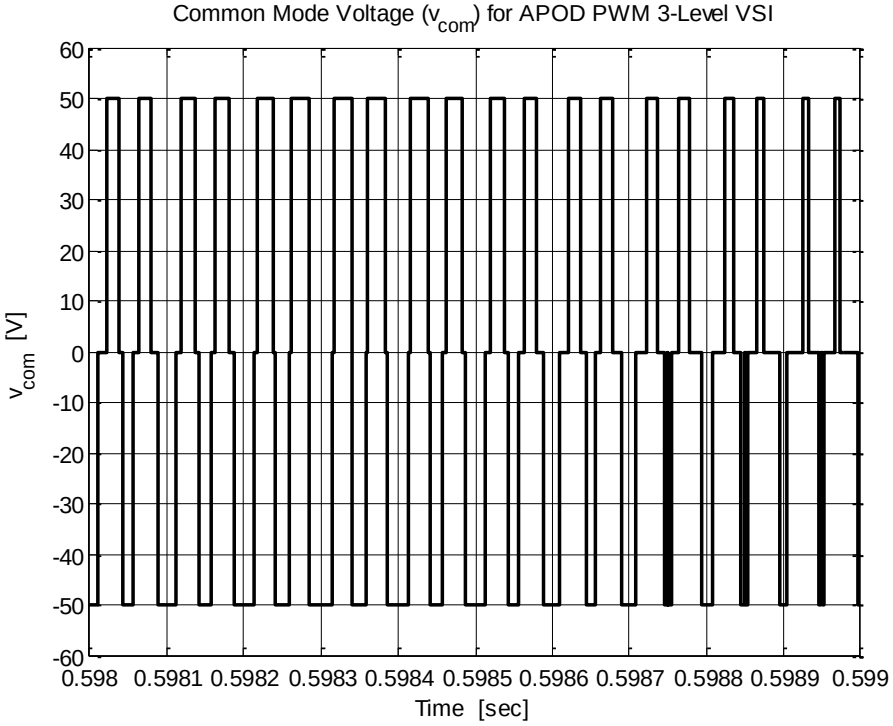

Figure 22: Common mode voltage (v_{com}) for the APOD: time range 0.598 sec to 0.599 sec.

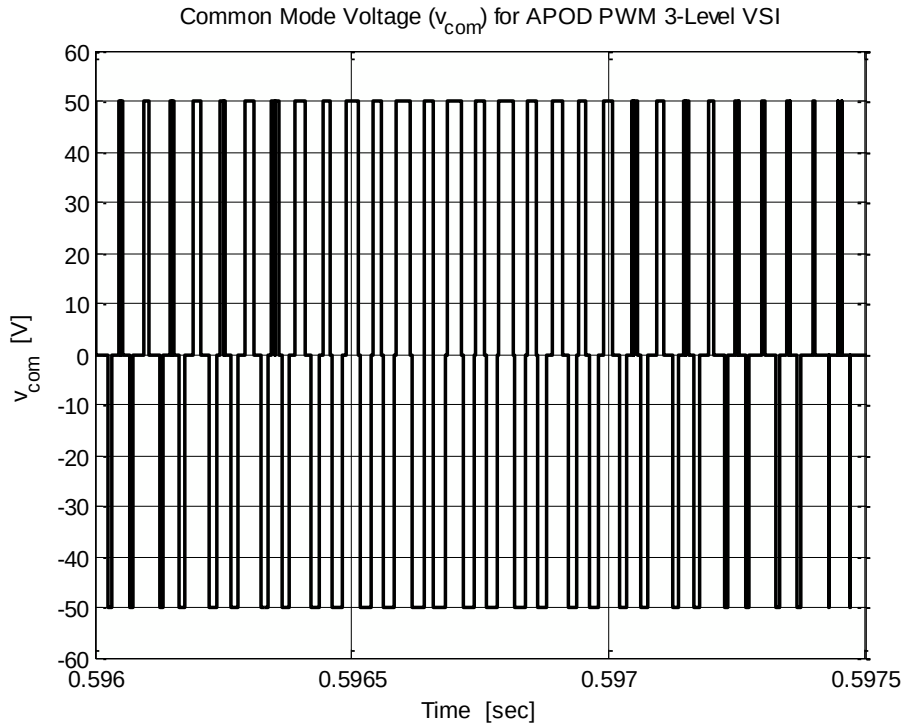

Figure 23: Common mode voltage (v_{com}) for the APOD: time range 0.596 sec to 0.5975 sec.

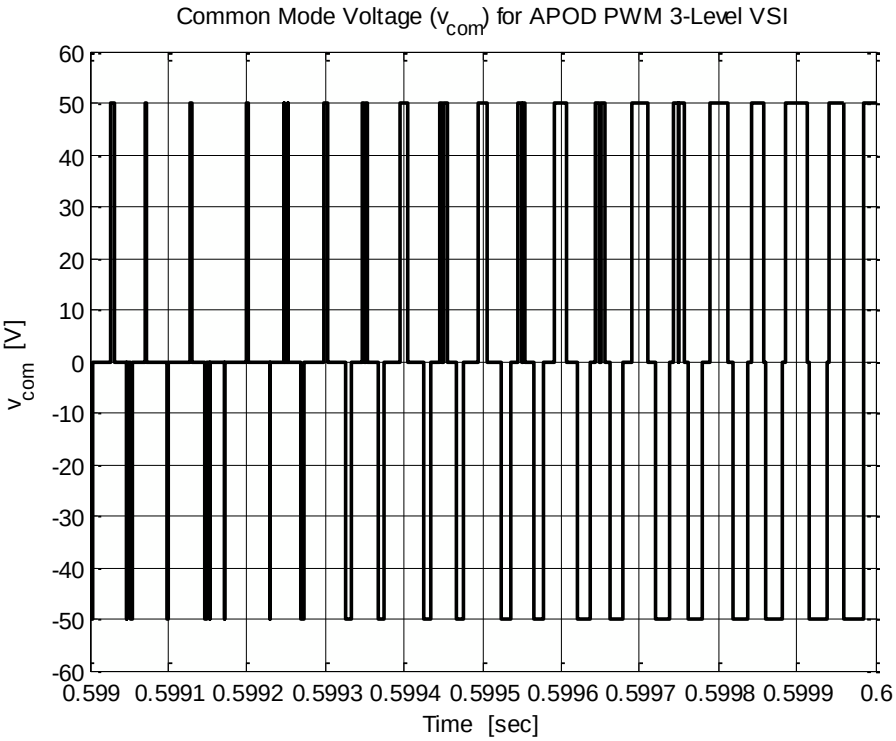

Figure 24: Common mode voltage (v_{com}) for the APOD: time range 0.599 sec to 0.6 sec.

7.4 Novel Carrier Based PWM (NCBPWM) Method for 3-Level 5-Phase VSI

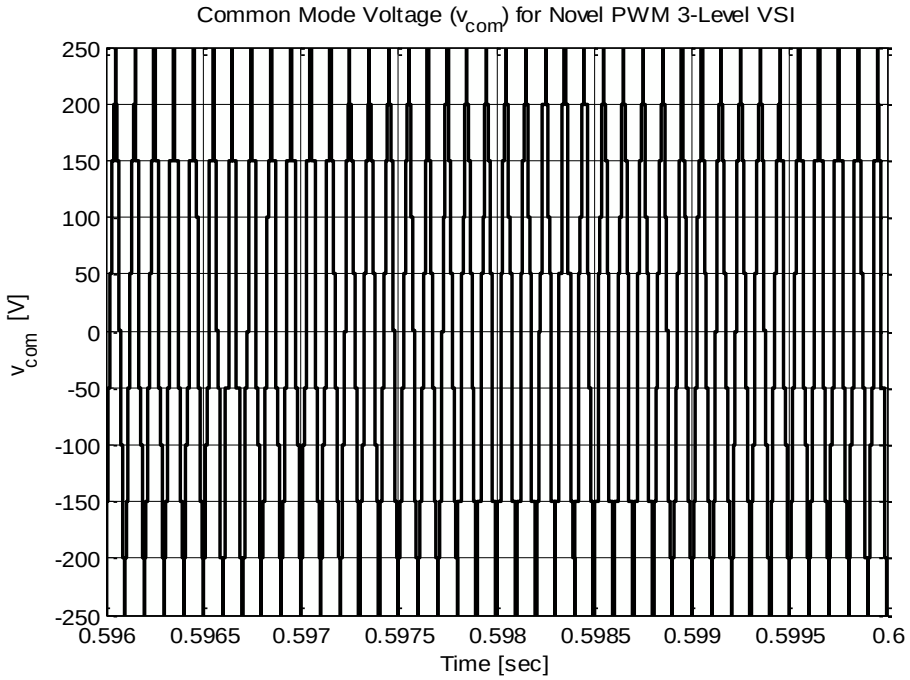

Figure 25: Common mode voltage (v_{com}) for the NCBPWM: time range 0.596 sec to 0.6 sec.

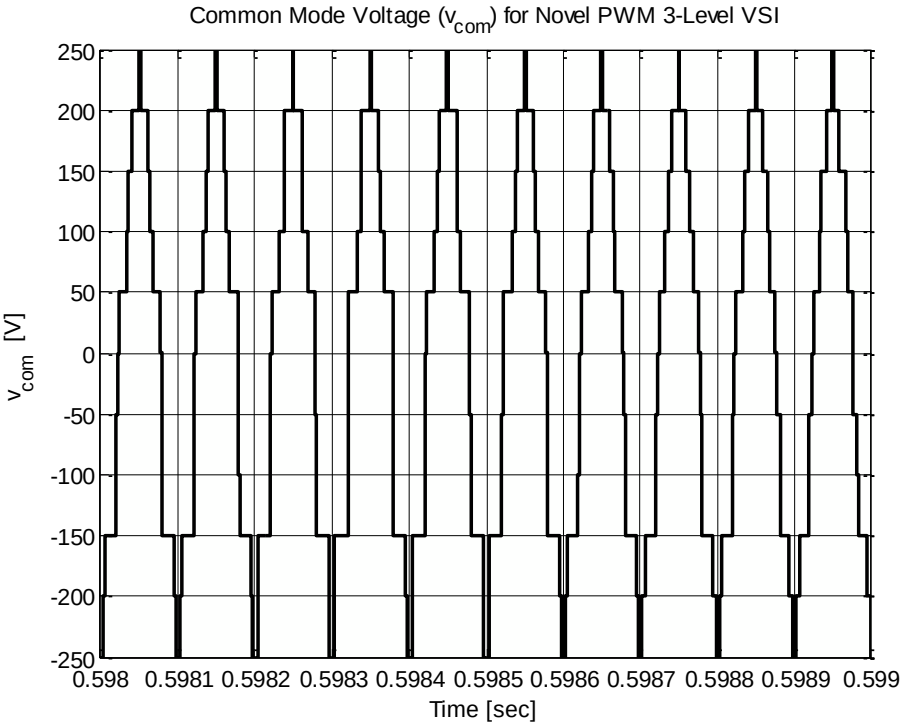

Figure 26: Common mode voltage (v_{com}) for the NCBPWM: time range 0.598 sec to 0.599 sec.

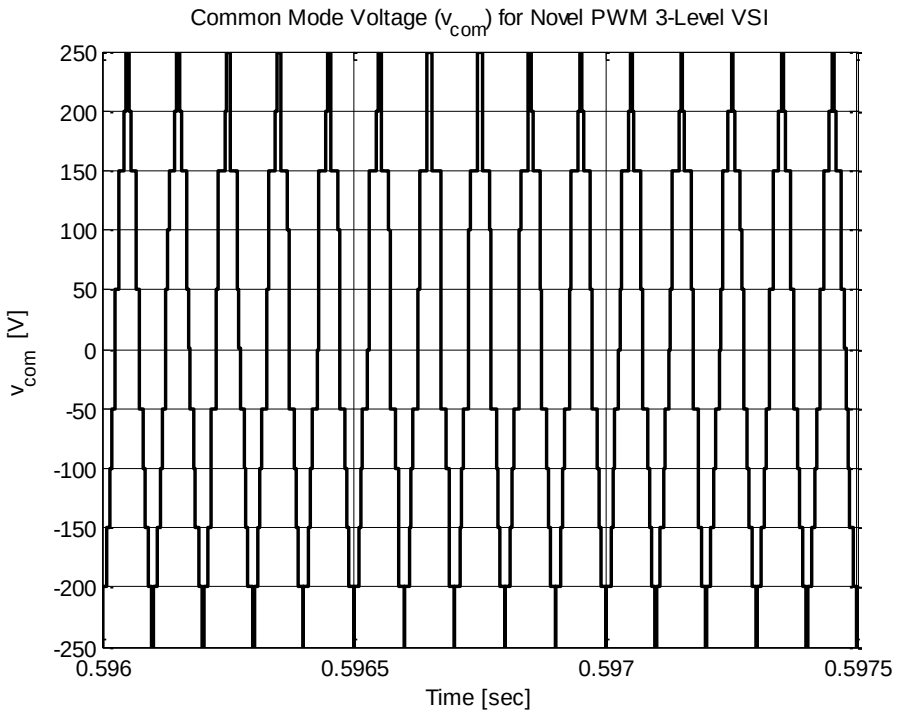

Figure 27: Common mode voltage (v_{com}) for the NCBPWM: time range 0.596 sec to 0.5975 sec.

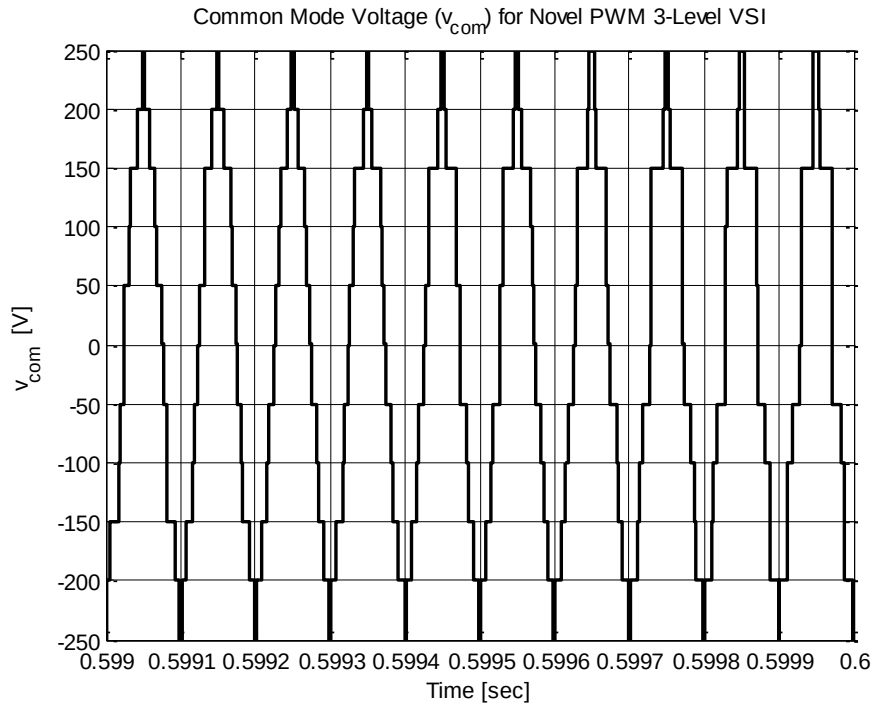

Figure 28: Common mode voltage (v_{com}) for the NCBPWM: time range 0.599 sec to 0.6 sec.

7.5 Phase Disposition (PD) Method for 5-Level VSI

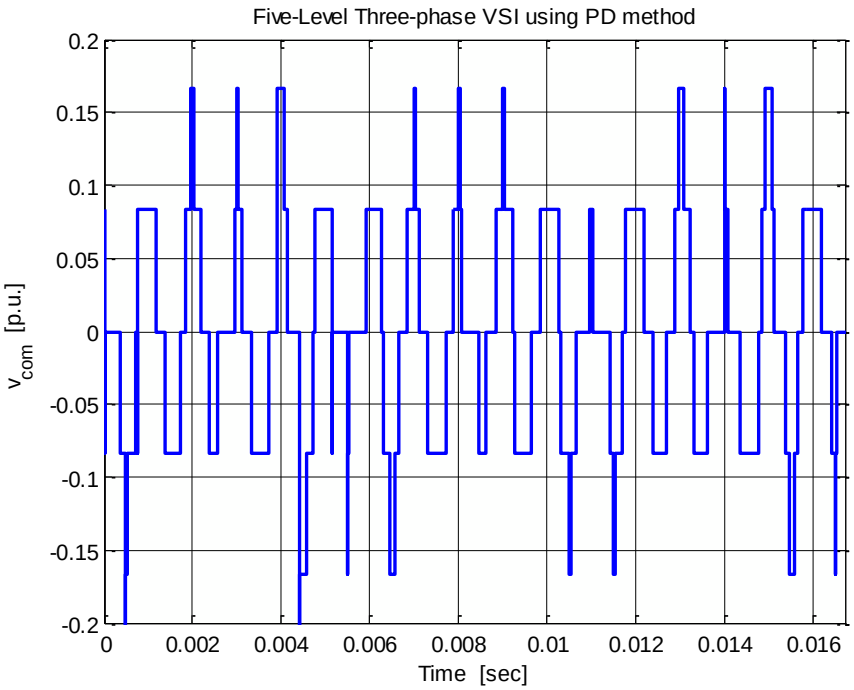

Figure 29: Common mode voltage (v_{com}) in the five-level three phase inverter for the PD method.

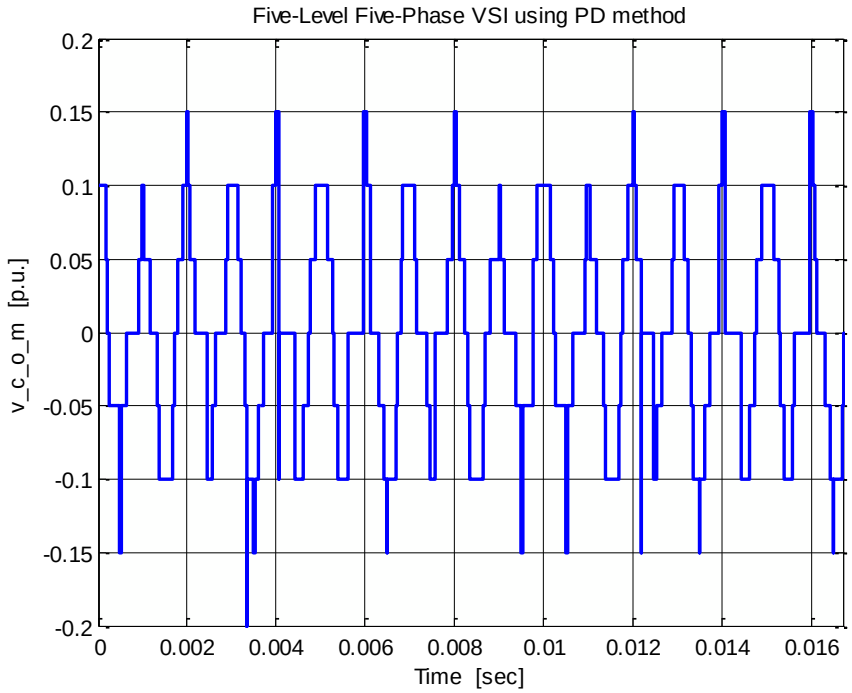

Figure 30: Common mode voltage (v_{com}) in the five-level five-phase inverter for the PD method.

7.6 Alternate Phase Opposition Disposition (APOD) Method for 5-Level VSI

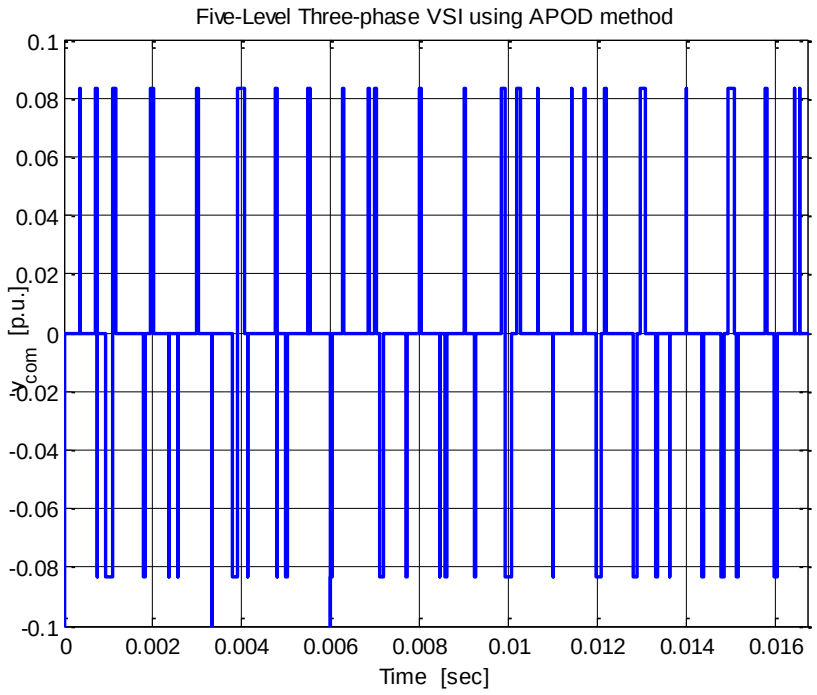

Figure 31: Common mode voltage (v_{com}) in the five-level three-phase inverter for the APOD method.

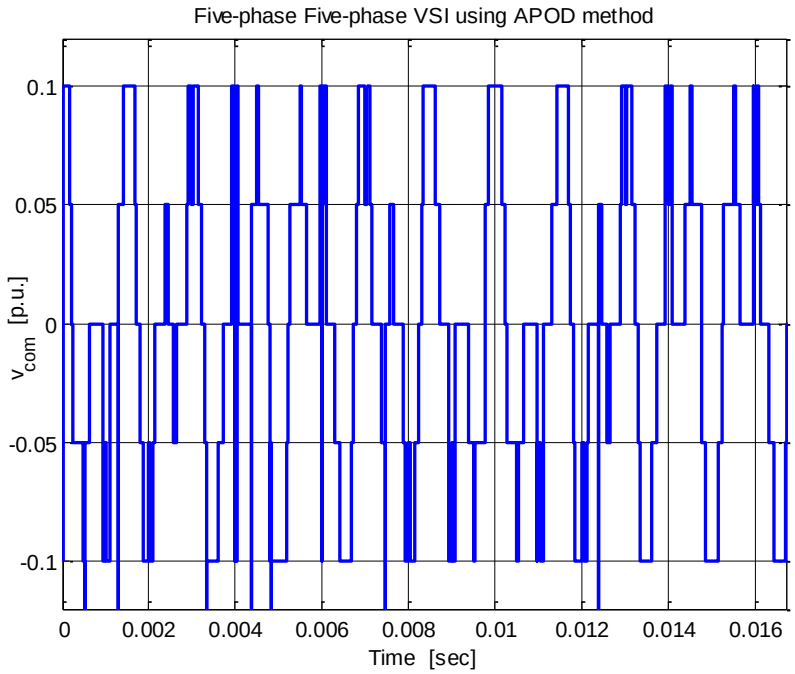

Figure 32: Common mode voltage (v_{com}) in the five-level five-phase inverter for the APOD method.

7.7 Novel Carrier Based PWM (NCBPWM) Method for 5-Level VSI

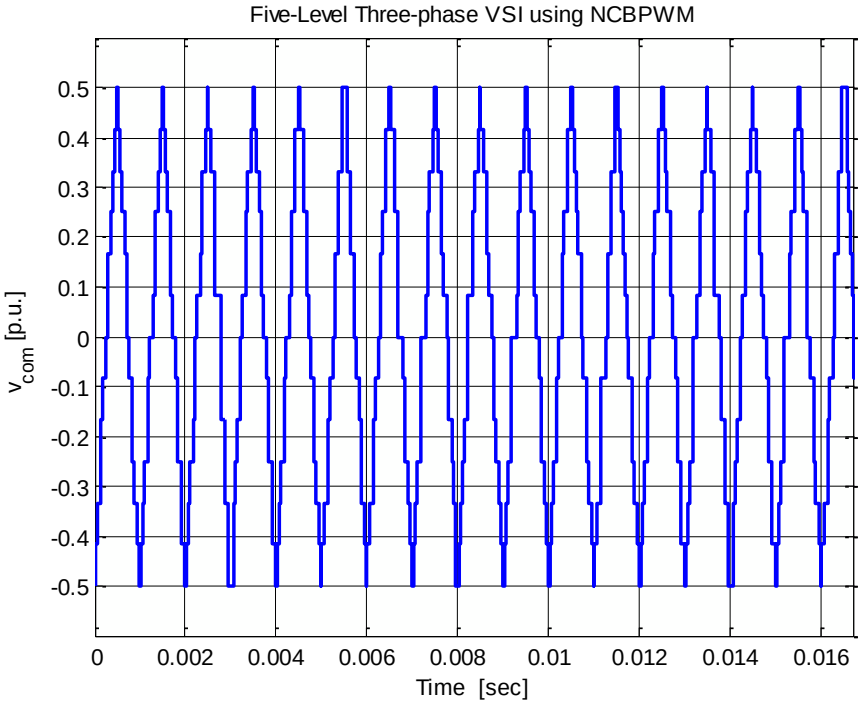

Figure 33: Common mode voltage (v_{com}) in the five-level three phase inverter for the NCBPWM.

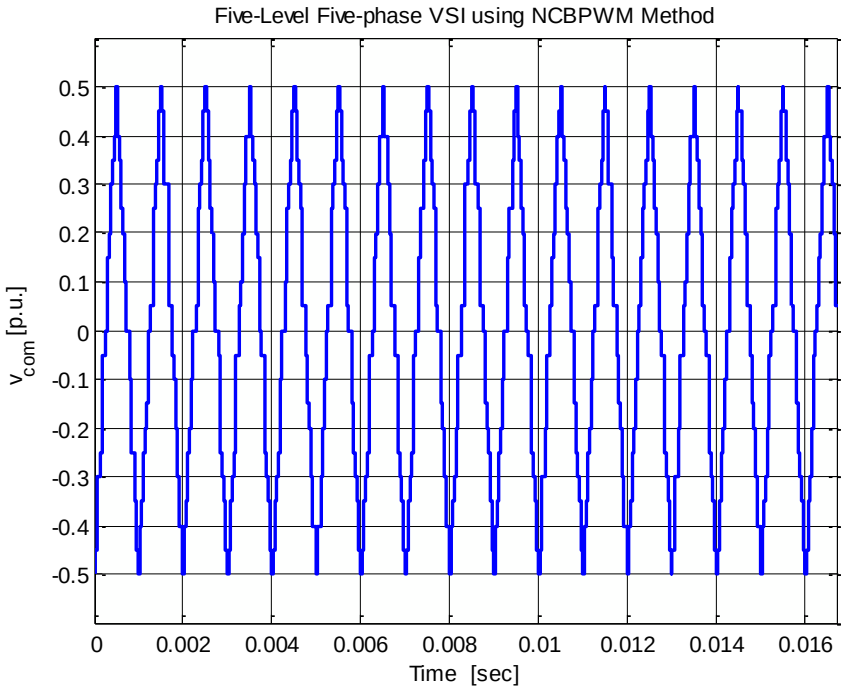

Figure 34: Common mode voltage (v_{com}) in the five-level five phase inverter for the NCBPWM.

7.8 Sinusoidal Pulse Width Modulation (SPWM) Method for 2-Level VSI

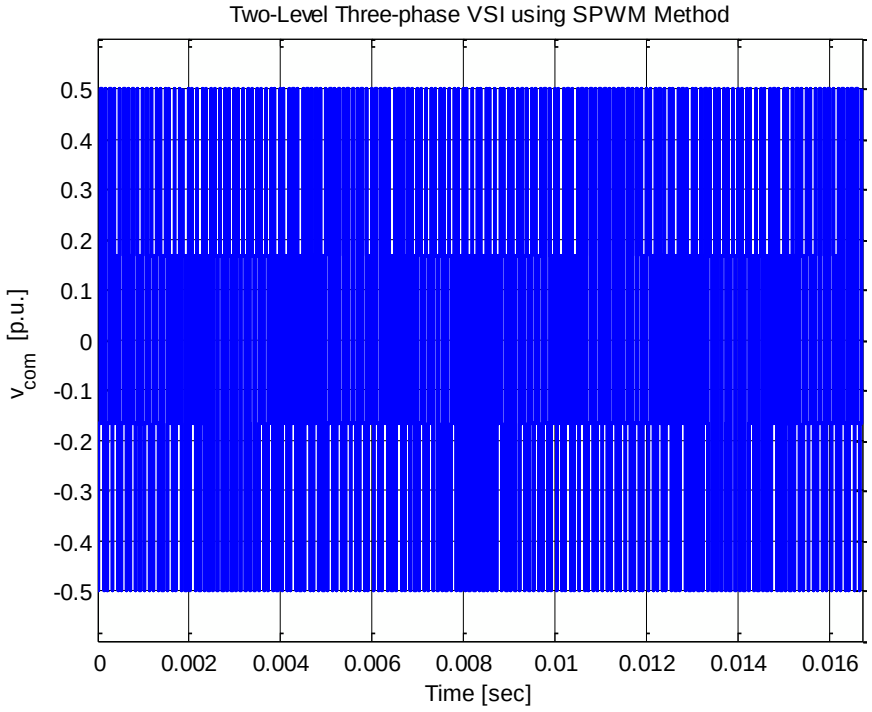

Figure 35: Common mode voltage (v_{com}) in the two-level three phase inverter for the SPWM ($T_s = 10\ kHz$).

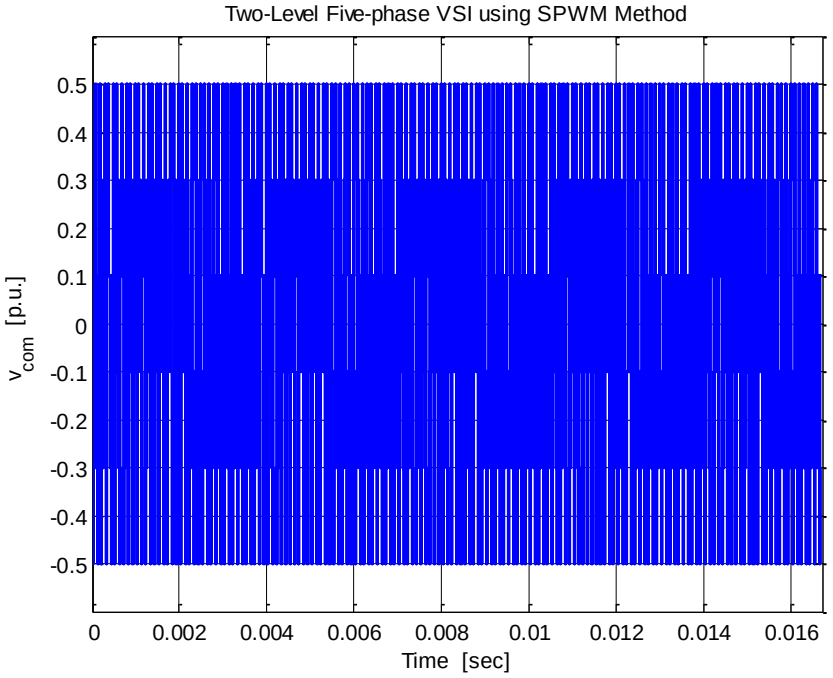

Figure 36: Common mode voltage (v_{com}) in the two-level five phase inverter for the SPWM ($T_s = 10\ kHz$).

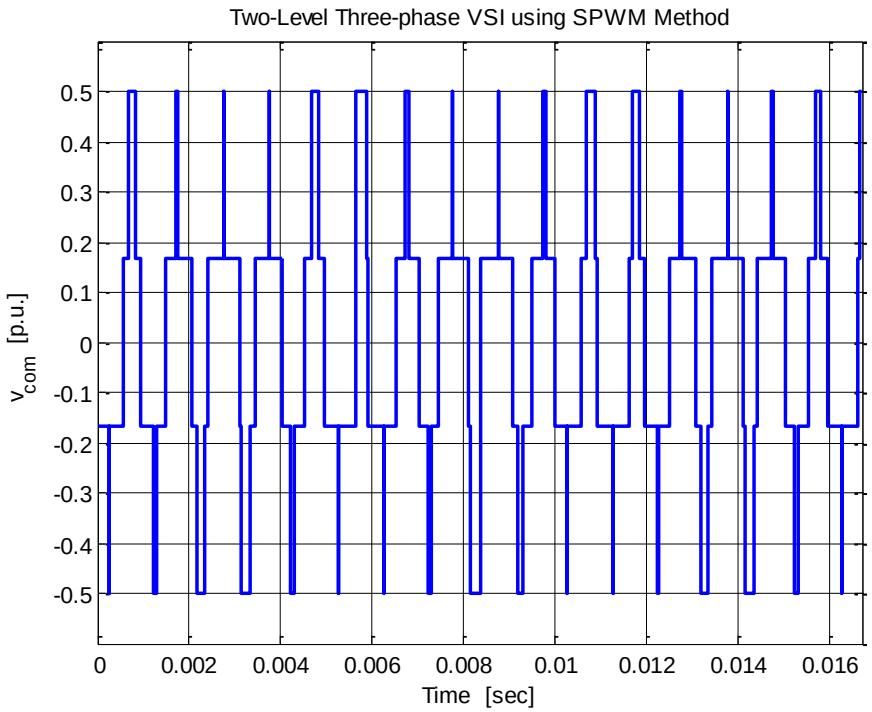

Figure 37: Common mode voltage (v_{com}) in the two-level three phase inverter for the SPWM ($T_s = 1\ kHz$).

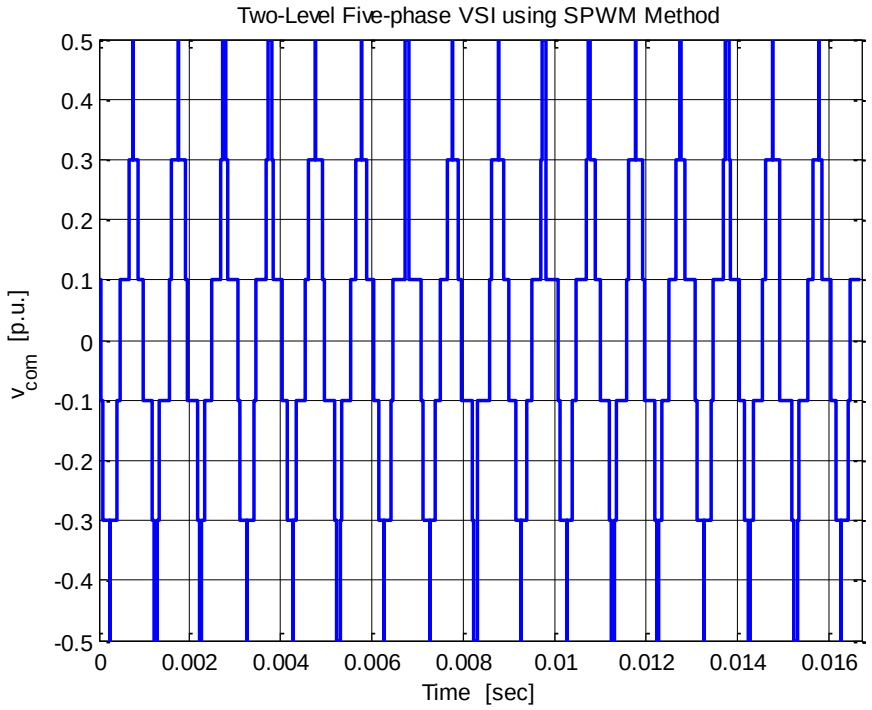

Figure 38: Common mode voltage (v_{com}) in the two-level five phase inverter for the SPWM ($T_s = 1\ kHz$).

8. CONCLUSION

The analysis of the common mode voltage in two-, three- and five-level diode-clamped three- and five-phase voltage source inverters has been presented. For the three-level and five-level inverter configurations, three modulation methods have been taken into consideration. From the above analysis, for 3-level and 5-level inverters, it is observed that the APOD modulation method presents the common mode voltage with the smallest number of the voltage levels in the common mode voltage followed by the PD method. In the NCBPWM method all voltage levels of the common mode voltage do exist. Whereas the two-level inverter has the highest step size, the step size decreases as the number of levels increases.

It has been found out that for the NCBPWM method, the transitions and number of occurrences of the levels in a switching cycle can be easily generalized using a mathematical expression as it has been presented in this report.

APPENDIX

TABLE A1: NUMBER OF VOLTAGE LEVELS IN COMMON MODE VOLTAGE FOR A 3-LEVEL 3-PHASE VSI USING PHASE DISPOSITION (PD) METHOD

S/N	t_{start}	t_{end}	$-3x_0$	$-2x_0$	$-x_0$	0	x_0	$2x_0$	$3x_0$	Total Levels	k	$t_{sim}=kT_s$	$6t_{sim}/T_s$
1	0	Ts	0	1	2	2	1	0	0	6	1	0.0001	6
2	0	2Ts	0	2	4	4	2	0	0	12	2	0.0002	12
3	0	3Ts	0	3	6	6	3	0	0	18	3	0.0003	18
4	0	4Ts	0	4	8	8	4	0	0	24	4	0.0004	24
5	0	5Ts	0	5	10	10	5	0	0	30	5	0.0005	30
6	0	6Ts	0	6	12	12	6	0	0	36	6	0.0006	36
7	0	7Ts	0	7	14	14	7	0	0	42	7	0.0007	42
8	0	8Ts	0	8	16	16	8	0	0	48	8	0.0008	48
9	0	9Ts	0	9	18	18	9	0	0	54	9	0.0009	54
10	0	10Ts	0	10	20	20	10	0	0	60	10	0.001	60
11	0	20Ts	0	14	34	40	26	7	0	121	20	0.002	120
12	0	30Ts	0	14	44	60	45	16	0	179	30	0.003	180
13	0	40Ts	0	14	54	80	65	26	0	239	40	0.004	240
14	0	50Ts	0	22	72	100	77	27	0	298	50	0.005	300
15	0	60Ts	0	31	91	120	87	27	0	356	60	0.006	360
16	0	70Ts	0	40	110	140	97	28	0	415	70	0.007	420
17	0	80Ts	0	40	120	160	117	38	0	475	80	0.008	480
18	0	90Ts	0	40	130	180	137	48	0	535	90	0.009	540
19	0	100Ts	0	43	143	200	155	55	0	596	100	0.01	600
20	0	166.7Ts	0	81	248	333	247	81	0	990	166.7	0.01667	1000

$$T_s = 100\ \mu s$$

$x_0 = \Delta_{\min} v_{\text{com}}$, which is $\frac{v_{dc}}{6}$ in this case

TABLE A2: NUMBER OF VOLTAGE LEVELS IN COMMON MODE VOLTAGE FOR A 3-LEVEL 5-PHASE VSI USING PHASE DISPOSITION (PD) METHOD

S/N	t_{start}	t_{end}	$-5x_0$	$-4x_0$	$-3x_0$	$-2x_0$	$-x_0$	0	x_0	$2x_0$	$3x_0$	$4x_0$	$5x_0$	Total Levels	k	$t_{sim}=kT_s$	$10t_{sim}/T_s$
1	0	T_s	0	0	0	1	2	2	2	2	1	0	0	10	1	0.0001	10
2	0	$2T_s$	0	0	0	2	4	4	4	4	2	0	0	20	2	0.0002	20
3	0	$3T_s$	0	0	0	3	6	6	6	6	3	0	0	30	3	0.0003	30
4	0	$4T_s$	0	0	0	4	8	8	8	8	4	0	0	40	4	0.0004	40
5	0	$5T_s$	0	0	0	5	10	10	10	10	5	0	0	50	5	0.0005	50
6	0	$6T_s$	0	0	0	6	12	12	12	12	6	0	0	60	6	0.0006	60
7	0	$7T_s$	0	0	0	7	14	14	14	14	7	0	0	70	7	0.0007	70
8	0	$8T_s$	0	0	0	8	16	16	16	16	8	0	0	80	8	0.0008	80
9	0	$9T_s$	0	0	1	10	18	18	18	18	8	0	0	91	9	0.0009	90
10	0	$10T_s$	0	0	2	12	20	20	20	19	8	0	0	101	10	0.001	100
11	0	$20T_s$	0	0	12	32	40	40	40	29	8	0	0	201	20	0.002	200
12	0	$30T_s$	0	0	17	47	60	60	60	43	13	0	0	300	30	0.003	300
13	0	$40T_s$	0	0	17	56	79	80	80	63	23	0	0	398	40	0.004	400
14	0	$50T_s$	0	0	25	74	99	100	100	74	24	0	0	496	50	0.005	500
15	0	$60T_s$	0	0	33	92	119	120	119	85	26	0	0	594	60	0.006	600
16	0	$70T_s$	0	0	33	102	139	140	139	105	36	0	0	694	70	0.007	700
17	0	$80T_s$	0	0	38	117	159	160	159	120	40	0	0	793	80	0.008	800
18	0	$90T_s$	0	0	48	137	179	180	179	130	40	0	0	893	90	0.009	900
19	0	$100T_s$	0	0	50	149	199	200	199	148	49	0	0	994	100	0.01	1000
20	0	$166.7T_s$	0	0	83	248	332	333	331	246	81	0	0	1654	166.67	0.01667	1667

$$T_s = 100\ \mu s$$

$x_0 = \Delta_{\min} v_{\text{com}}$, which is $\frac{v_{dc}}{10}$ in this case

TABLE A3: NUMBER OF VOLTAGE LEVELS IN COMMON MODE VOLTAGE FOR A 3-LEVEL 3-PHASE VSI USING ALTERNATE PHASE OPPOSITION DISPOSITION (APOD) METHOD

S/N	t_{start}	t_{end}	$-3x_0$	$-2x_0$	$-x_0$	0	x_0	$2x_0$	$3x_0$	Total Levels	k	$t_{sim}=kT_s$	$6t_{sim}/T_s$
1	0	T_s	0	0	1	3	2	0	0	6	1	0.0001	6
2	0	$2T_s$	0	0	2	6	4	0	0	12	2	0.0002	12
3	0	$3T_s$	0	0	3	9	6	0	0	18	3	0.0003	18
4	0	$4T_s$	0	0	4	12	8	0	0	24	4	0.0004	24
5	0	$5T_s$	0	0	5	15	10	0	0	30	5	0.0005	30
6	0	$6T_s$	0	0	6	18	12	0	0	36	6	0.0006	36
7	0	$7T_s$	0	0	7	21	14	0	0	42	7	0.0007	42
8	0	$8T_s$	0	0	8	24	16	0	0	48	8	0.0008	48
9	0	$9T_s$	0	0	9	27	18	0	0	54	9	0.0009	54
10	0	$10T_s$	0	0	10	30	20	0	0	60	10	0.001	60
11	0	$20T_s$	0	0	25	60	35	0	0	120	20	0.002	120
12	0	$30T_s$	0	0	44	89	45	0	0	178	30	0.003	180
13	0	$40T_s$	0	0	64	119	55	0	0	238	40	0.004	240
14	0	$50T_s$	0	0	77	149	72	0	0	298	50	0.005	300
15	0	$60T_s$	0	0	87	178	91	0	0	356	60	0.006	360
16	0	$70T_s$	0	0	97	208	111	0	0	416	70	0.007	420
17	0	$80T_s$	0	0	117	238	121	0	0	476	80	0.008	480
18	0	$90T_s$	0	0	136	267	131	0	0	534	90	0.009	540
19	0	$100T_s$	0	0	153	297	144	0	0	594	100	0.01	600
20	0	$166.7T_s$	0	0	247	495	248	0	0	990	166.67	0.01667	1000

$$T_s = 100\ \mu s$$

$x_0 = \Delta_{\min} v_{\text{com}}$, which is $\frac{v_{dc}}{6}$ in this case

TABLE A4: NUMBER OF VOLTAGE LEVELS IN COMMON MODE VOLTAGE FOR A 3-LEVEL 5-PHASE VSI USING ALTERNATE PHASE OPPOSITION DISPOSITION (APOD) METHOD

S/N	t_{start}	t_{end}	$-5x_0$	$-4x_0$	$-3x_0$	$-2x_0$	$-x_0$	0	x_0	$2x_0$	$3x_0$	$4x_0$	$5x_0$	Total Levels	k	$t_{sim}=kT_s$	$10t_{sim}/T_s$
1	0	Ts	0	0	0	0	2	5	3	0	0	0	0	10	1	0.0001	10
2	0	2Ts	0	0	0	0	4	10	6	0	0	0	0	20	2	0.0002	20
3	0	3Ts	0	0	0	0	6	15	9	0	0	0	0	30	3	0.0003	30
4	0	4Ts	0	0	0	0	8	20	12	0	0	0	0	40	4	0.0004	40
5	0	5Ts	0	0	0	0	10	25	15	0	0	0	0	50	5	0.0005	50
6	0	6Ts	0	0	0	0	12	30	18	0	0	0	0	60	6	0.0006	60
7	0	7Ts	0	0	0	0	14	35	21	0	0	0	0	70	7	0.0007	70
8	0	8Ts	0	0	0	0	16	40	24	0	0	0	0	80	8	0.0008	80
9	0	9Ts	0	0	0	0	20	45	25	0	0	0	0	90	9	0.0009	90
10	0	10Ts	0	0	0	0	23	50	27	0	0	0	0	100	10	0.001	100
11	0	20Ts	0	0	0	0	52	99	47	0	0	0	0	198	20	0.002	200
12	0	30Ts	0	0	0	0	76	148	72	0	0	0	0	296	30	0.003	300
13	0	40Ts	0	0	0	0	96	198	102	0	0	0	0	396	40	0.004	400
14	0	50Ts	0	0	0	0	124	248	124	0	0	0	0	496	50	0.005	500
15	0	60Ts	0	0	0	0	151	298	147	0	0	0	0	596	60	0.006	600
16	0	70Ts	0	0	0	0	171	347	176	0	0	0	0	694	70	0.007	700
17	0	80Ts	0	0	0	0	196	396	200	0	0	0	0	792	80	0.008	800
18	0	90Ts	0	0	0	0	226	446	220	0	0	0	0	892	90	0.009	900
19	0	100Ts	0	0	0	0	248	496	248	0	0	0	0	992	100	0.01	1000
20	0	166.7Ts	0	0	0	0	413	827	414	0	0	0	0	1654	166.7	0.01667	1667

$$T_s = 100\ \mu s$$

$x_0 = \Delta_{\min} v_{\text{com}}$, which is $\frac{v_{dc}}{10}$ in this case

TABLE A5: NUMBER OF VOLTAGE LEVELS IN COMMON MODE VOLTAGE FOR A 5-LEVEL 3-PHASE VSI USING PHASE DISPOSITION (PD) METHOD

S/N	t_{start}	t_{end}	$-6x_0$	$-5x_0$	$-4x_0$	$-3x_0$	$-2x_0$	$-x_0$	0	x_0	$2x_0$	$3x_0$	$4x_0$	$5x_0$	$6x_0$	Total Levels	k	$t_{sim}=kT_s$	$6t_{sim}/T_s$
1	0	Ts	0	0	0	0	1	2	2	1	0	0	0	0	0	6	1	0.0001	6
2	0	2Ts	0	0	0	0	2	4	4	2	0	0	0	0	0	12	2	0.0002	12
3	0	3Ts	0	0	0	0	3	6	6	3	0	0	0	0	0	18	3	0.0003	18
4	0	4Ts	0	0	0	0	4	8	8	4	0	0	0	0	0	24	4	0.0004	24
5	0	5Ts	0	0	0	0	5	10	10	5	0	0	0	0	0	30	5	0.0005	30
6	0	6Ts	0	0	0	0	6	12	12	6	0	0	0	0	0	36	6	0.0006	36
7	0	7Ts	0	0	0	0	7	14	14	7	0	0	0	0	0	42	7	0.0007	42
8	0	8Ts	0	0	0	0	8	16	16	8	0	0	0	0	0	48	8	0.0008	48
9	0	9Ts	0	0	0	0	9	18	18	9	0	0	0	0	0	54	9	0.0009	54
10	0	10Ts	0	0	0	0	10	20	20	10	0	0	0	0	0	60	10	0.001	60
11	0	20Ts	0	0	0	0	14	34	40	26	7	0	0	0	0	121	20	0.002	120
12	0	30Ts	0	0	0	0	14	44	60	46	17	0	0	0	0	181	30	0.003	180
13	0	40Ts	0	0	0	0	14	54	80	66	27	0	0	0	0	241	40	0.004	240
14	0	50Ts	0	0	0	0	22	72	100	78	28	0	0	0	0	300	50	0.005	300
15	0	60Ts	0	0	0	0	31	91	120	88	28	0	0	0	0	358	60	0.006	360
16	0	70Ts	0	0	0	0	40	110	140	98	29	0	0	0	0	417	70	0.007	420
17	0	80Ts	0	0	0	0	40	120	160	118	39	0	0	0	0	477	80	0.008	480
18	0	90Ts	0	0	0	0	40	130	180	138	49	0	0	0	0	537	90	0.009	540
19	0	100Ts	0	0	0	0	43	143	200	156	56	0	0	0	0	598	100	0.01	600
20	0	166.7Ts	0	0	0	0	82	249	334	248	82	0	0	0	0	995	166.7	0.01667	1000

$$T_s = 100\ \mu s$$

$x_0 = \Delta_{\min} v_{\text{com}}$, which is $\frac{v_{dc}}{12}$ in this case

TABLE A6: NUMBER OF VOLTAGE LEVELS IN COMMON MODE VOLTAGE FOR A 5-LEVEL 5-PHASE VSI USING PHASE DISPOSITION (PD) METHOD

S/N	t_{start}	t_{end}	-3 x_0	-2 x_0	- x_0	0	x_0	2 x_0	3 x_0	Total Levels	k	$t_{sim}=kT_s$	$10t_{sim}/T_s$
1	0	Ts	1	2	2	2	2	1	0	10	1	0.0001	10
2	0	2Ts	2	4	4	4	4	2	0	20	2	0.0002	20
3	0	3Ts	3	6	6	6	6	3	0	30	3	0.0003	30
4	0	4Ts	4	8	8	8	8	4	0	40	4	0.0004	40
5	0	5Ts	5	10	10	10	10	5	0	50	5	0.0005	50
6	0	6Ts	6	12	12	12	12	6	1	61	6	0.0006	60
7	0	7Ts	6	13	14	14	14	8	2	71	7	0.0007	70
8	0	8Ts	6	14	16	16	16	10	3	81	8	0.0008	80
9	0	9Ts	8	16	18	18	18	12	3	93	9	0.0009	90
10	0	10Ts	9	18	20	20	20	13	3	103	10	0.001	100
11	0	20Ts	10	29	40	41	40	31	12	203	20	0.002	200
12	0	30Ts	15	44	60	61	60	46	16	302	30	0.003	300
13	0	40Ts	23	62	80	81	80	57	18	401	40	0.004	400
14	0	50Ts	25	74	100	101	100	74	24	498	50	0.005	500
15	0	60Ts	27	86	120	121	120	90	31	595	60	0.006	600
16	0	70Ts	35	104	140	141	140	102	32	694	70	0.007	700
17	0	80Ts	40	119	160	161	160	116	37	793	80	0.008	800
18	0	90Ts	41	130	180	181	180	135	45	892	90	0.009	900
19	0	100Ts	49	148	200	201	200	148	48	994	100	0.01	1000
20	0	166.7Ts	80	246	333	334	333	246	80	1652	166.7	0.01667	1667

$$T_s = 100\ \mu s$$

$x_0 = \Delta_{\min} v_{\text{com}}$, which is $\frac{v_{dc}}{20}$ in this case

TABLE A7: NUMBER OF VOLTAGE LEVELS IN COMMON MODE VOLTAGE FOR A 5-LEVEL 3-PHASE VSI USING ALTERNATE PHASE OPPOSITION DISPOSITION (APOD) METHOD

S/N	t_{start}	t_{end}	$-6x_0$	$-5x_0$	$-4x_0$	$-3x_0$	$-2x_0$	$-x_0$	0	x_0	$2x_0$	$3x_0$	$4x_0$	$5x_0$	$6x_0$	Total Levels	k	$t_{sim}=kT_s$	$6t_{sim}/T_s$
1	0	Ts	0	0	0	0	0	1	3	2	0	0	0	0	0	6	1	0.0001	6
2	0	2Ts	0	0	0	0	0	2	6	4	0	0	0	0	0	12	2	0.0002	12
3	0	3Ts	0	0	0	0	0	3	9	6	0	0	0	0	0	18	3	0.0003	18
4	0	4Ts	0	0	0	0	0	4	12	8	0	0	0	0	0	24	4	0.0004	24
5	0	5Ts	0	0	0	0	0	5	15	10	0	0	0	0	0	30	5	0.0005	30
6	0	6Ts	0	0	0	0	0	6	18	12	0	0	0	0	0	36	6	0.0006	36
7	0	7Ts	0	0	0	0	0	7	21	14	0	0	0	0	0	42	7	0.0007	42
8	0	8Ts	0	0	0	0	0	8	24	16	0	0	0	0	0	48	8	0.0008	48
9	0	9Ts	0	0	0	0	0	9	27	18	0	0	0	0	0	54	9	0.0009	54
10	0	10Ts	0	0	0	0	0	10	30	20	0	0	0	0	0	60	10	0.001	60
11	0	20Ts	0	0	0	0	0	26	60	35	0	0	0	0	0	121	20	0.002	120
12	0	30Ts	0	0	0	0	0	46	90	45	0	0	0	0	0	181	30	0.003	180
13	0	40Ts	0	0	0	0	0	66	120	55	0	0	0	0	0	241	40	0.004	240
14	0	50Ts	0	0	0	0	0	77	150	73	0	0	0	0	0	300	50	0.005	300
15	0	60Ts	0	0	0	0	0	87	180	93	0	0	0	0	0	360	60	0.006	360
16	0	70Ts	0	0	0	0	0	98	210	113	0	0	0	0	0	421	70	0.007	420
17	0	80Ts	0	0	0	0	0	118	240	123	0	0	0	0	0	481	80	0.008	480
18	0	90Ts	0	0	0	0	0	138	270	133	0	0	0	0	0	541	90	0.009	540
19	0	100Ts	0	0	0	0	0	155	300	145	0	0	0	0	0	600	100	0.01	600
20	0	166.7Ts	0	0	0	0	0	248	498	250	0	0	0	0	0	996	166.7	0.01667	1000

$$T_s = 100\ \mu s$$

$x_0 = \Delta_{\min} v_{\text{com}}$, which is $\frac{v_{dc}}{12}$ in this case

TABLE A8: NUMBER OF VOLTAGE LEVELS IN COMMON MODE VOLTAGE FOR A 5-LEVEL 5-PHASE VSI USING ALTERNATE PHASE OPPOSITION DISPOSITION (APOD) METHOD

S/N	t_{start}	t_{end}	-2 x_0	- x_0	0	x_0	2 x_0	Total Levels	k	$t_{sim}=kT_s$	$10t_{sim}/T_s$
1	0	Ts	1	2	2	3	2	10	1	0.0001	10
2	0	2Ts	2	4	4	6	4	20	2	0.0002	20
3	0	3Ts	3	6	6	9	6	30	3	0.0003	30
4	0	4Ts	4	8	8	12	8	40	4	0.0004	40
5	0	5Ts	5	10	10	15	10	50	5	0.0005	50
6	0	6Ts	6	12	12	18	12	60	6	0.0006	60
7	0	7Ts	6	14	15	21	14	70	7	0.0007	70
8	0	8Ts	6	16	19	24	15	80	8	0.0008	80
9	0	9Ts	6	18	24	27	15	90	9	0.0009	90
10	0	10Ts	7	21	28	29	15	100	10	0.001	100
11	0	20Ts	27	51	49	49	24	200	20	0.002	200
12	0	30Ts	37	75	78	74	34	298	30	0.003	300
13	0	40Ts	46	95	99	104	54	398	40	0.004	400
14	0	50Ts	61	124	127	124	61	497	50	0.005	500
15	0	60Ts	75	153	155	145	68	596	60	0.006	600
16	0	70Ts	84	173	176	175	88	696	70	0.007	700
17	0	80Ts	94	198	205	199	98	794	80	0.008	800
18	0	90Ts	114	228	226	219	107	894	90	0.009	900
19	0	100Ts	123	248	254	248	122	995	100	0.01	1000
20	0	166.7Ts	203	414	423	412	202	1654	166.7	0.01667	1667

$$T_s = 100\ \mu s$$

$x_0 = \Delta_{\min} v_{\text{com}}$, which is $\frac{v_{dc}}{20}$ in this case

TABLE A9: NUMBER OF VOLTAGE LEVELS IN COMMON MODE VOLTAGE FOR A 2-LEVEL 3-PHASE VSI USING SINUSOIDAL PWM (SPWM) METHOD

S/N	t_{start}	t_{end}	$-3x_0$	$-x_0$	x_0	$3x_0$	Total Levels	k	$t_{sim}=kT_s$	$6t_{sim}/T_s$
1	0	Ts	1	2	2	1	6	1	0.0001	6
2	0	2Ts	2	4	4	2	12	2	0.0002	12
3	0	3Ts	3	6	6	3	18	3	0.0003	18
4	0	4Ts	4	8	8	4	24	4	0.0004	24
5	0	5Ts	5	10	10	5	30	5	0.0005	30
6	0	6Ts	6	12	12	6	36	6	0.0006	36
7	0	7Ts	7	14	14	7	42	7	0.0007	42
8	0	8Ts	8	16	16	8	48	8	0.0008	48
9	0	9Ts	9	18	18	9	54	9	0.0009	54
10	0	10Ts	10	20	20	10	60	10	0.001	60
11	0	20Ts	20	39	40	20	119	20	0.002	120
12	0	30Ts	30	59	60	30	179	30	0.003	180
13	0	40Ts	40	79	80	40	239	40	0.004	240
14	0	50Ts	50	100	100	50	300	50	0.005	300
15	0	60Ts	60	120	120	60	360	60	0.006	360
16	0	70Ts	70	139	140	70	419	70	0.007	420
17	0	80Ts	80	159	160	80	479	80	0.008	480
18	0	90Ts	90	179	180	90	539	90	0.009	540
19	0	100Ts	100	200	200	100	600	100	0.01	600
20	0	166.7Ts	167	333	333	167	1000	166.7	0.01667	1000

$$T_s = 100\ \mu s$$

$x_0 = \frac{1}{2}\Delta_{\min} v_{\text{com}}$, which is $\frac{v_{dc}}{6}$ in this case

TABLE A10: NUMBER OF VOLTAGE LEVELS IN COMMON MODE VOLTAGE FOR A 2-LEVEL 5-PHASE VSI USING SINUSOIDAL PWM (SPWM) METHOD

S/N	t_{start}	t_{end}	$-5x_0$	$-3x_0$	$-1x_0$	x_0	$3x_0$	$5x_0$	Total Levels	k	$t_{sim}=kT_s$	$10t_{sim}/T_s$
1	0	Ts	1	2	2	2	2	1	10	1	0.0001	10
2	0	2Ts	2	4	4	4	4	2	20	2	0.0002	20
3	0	3Ts	3	6	6	6	6	3	30	3	0.0003	30
4	0	4Ts	4	8	8	8	8	4	40	4	0.0004	40
5	0	5Ts	5	10	10	10	10	5	50	5	0.0005	50
6	0	6Ts	6	12	12	12	12	6	60	6	0.0006	60
7	0	7Ts	7	14	14	14	14	7	70	7	0.0007	70
8	0	8Ts	8	16	16	16	16	8	80	8	0.0008	80
9	0	9Ts	9	18	19	18	18	9	91	9	0.0009	90
10	0	10Ts	10	20	21	20	20	10	101	10	0.001	100
11	0	20Ts	20	40	41	40	40	20	201	20	0.002	200
12	0	30Ts	30	60	60	60	60	30	300	30	0.003	300
13	0	40Ts	40	80	80	80	80	40	400	40	0.004	400
14	0	50Ts	50	100	101	100	100	50	501	50	0.005	500
15	0	60Ts	60	120	120	120	120	60	600	60	0.006	600
16	0	70Ts	70	140	140	140	140	70	700	70	0.007	700
17	0	80Ts	80	160	161	160	160	80	801	80	0.008	800
18	0	90Ts	90	180	181	180	180	90	901	90	0.009	900
19	0	100Ts	100	200	200	200	200	100	1000	100	0.01	1000
20	0	166.7Ts	167	334	334	333	332	166	1666	166.7	0.01667	1666.7

$$T_s = 100\ \mu s$$

$x_0 = \frac{1}{2}\Delta_{\min} v_{\text{com}}$, which is $\frac{v_{dc}}{10}$ in this case

Chapter 3

COMMON MODE VOLTAGE IN DOUBLE ENDED DIODE-CLAMPED VOLTAGE SOURCE INVERTERS

1. INTRODUCTION

This report summarizes the work on the common mode voltage due to the use of multilevel multiphase inverters connected in a double ended (dual) configuration. In such a configuration, two converters are connected at the two ends of the stator winding of an *m*-phase machine. An example of such a configuration is shown in Fig. 1 for a five-phase system.

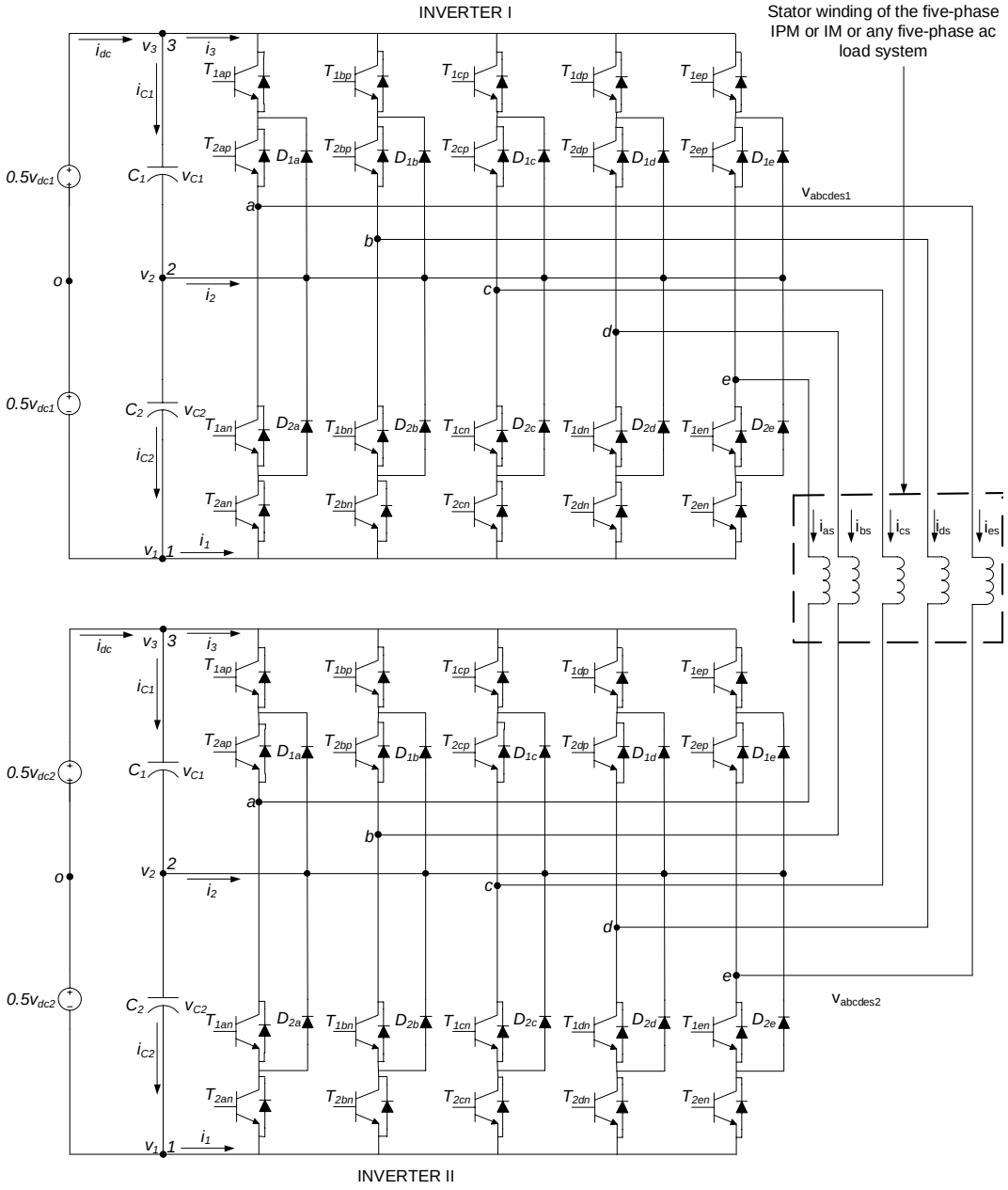

Figure 1 Configuration of the three-level diode-clamped five-phase dual-inverter system.

2. THEORY OF THE COMMON MODE VOLTAGE IN A DOUBLE ENDED SYSTEM

The expressions of the switched (pole) voltage, v_{io}, and common mode voltage, v_{com}, in the double ended (dual) inverter system are given as:

$$v_{io} = v_{io1} - v_{io2} \quad (1)$$

$$v_{com} = v_{com1} - v_{com2} \quad (2)$$

Where v_{io} $i = (a, b, c, d, e)$ is the pole (or switched voltage), and the subscripts 1 and 2 stand for inverter 1 and inverter 2 respectively.

3. LEVELS OF VOLTAGES IN THE COMMON MODE VOLTAGE.

Table 1 shows an example of the number of voltage levels in the common mode voltage $n_0 v_{\text{com}}$ and of the step size of the common mode voltage $\Delta_{\min} v_{\text{com}}$ for the 2, 3 and 5 level dual inverter configurations in the three-phase and five-phase systems. (Note that positive and negative values are counted separately.)

TABLE 1: Number of possible voltage levels in common mode voltage and the respective step size $\Delta_{\min} v_{\text{com}}$. (Note that positive and negative values are counted separately.)

Inverter Level (n)	Number of Phases (m)	Number of possible voltage levels in common mode voltage $n_0 v_{\text{com}}$	Step size $\Delta_{\min} v_{\text{com}}$
2	3	2 · 1 · 3 + 1 = 7 (incl. 0)	$\frac{v_{dc}}{3}$
2	5	2 · 1 · 5 + 1 = 11 (incl. 0)	$\frac{v_{dc}}{5}$
3	3	2 · 2 · 3 + 1 = 13 (incl. 0)	$\frac{v_{dc}}{6}$
3	5	2 · 2 · 5 + 1= 21 (incl. 0)	$\frac{v_{dc}}{10}$
5	3	2 · 4 · 3 + 1 = 25 (incl. 0)	$\frac{v_{dc}}{12}$
5	5	2 · 4 · 5 + 1 = 41 (incl. 0)	$\frac{v_{dc}}{20}$

In general,

- **As for the single inverter, the unit step size of the common mode voltage, $\Delta_{\min} v_{\text{com}}$ is $\Delta_{\min} v_{\text{com}} = v_{\text{dc}}/[(n\text{-}1)m]$;**
- **But the number of voltage levels in the common mode voltage is $n_0 v_{\text{com}} = 2(n\text{-}1)m + 1$** (which is approximately two times the number of a single-inverter system ((n-1)m).)

The list of voltage levels in the common mode voltage available in three phase and five-phase ac systems for the double ended 2-, 3- and 5-level inverters is presented in Table 2 as follows:

TABLE 2: List of levels in the three-phase and five-phase systems for 2, 3 and 5-level inverters

SN	2-Level		3-Level		5-Level	
	3-Phase	5-Phase	3-Phase	5-Phase	3-Phase	5-Phase
1	0	0	0	0	0	0
2	$\pm\frac{v_{dc}}{3}$	$\pm\frac{v_{dc}}{5}$	$\pm\frac{v_{dc}}{6}$	$\pm\frac{v_{dc}}{10}$	$\pm\frac{v_{dc}}{12}$	$\pm\frac{v_{dc}}{20}$
3	$\pm\frac{2v_{dc}}{3}$	$\pm\frac{2v_{dc}}{5}$	$\pm\frac{2v_{dc}}{6}$	$\pm\frac{2v_{dc}}{10}$	$\pm\frac{2v_{dc}}{12}$	$\pm\frac{2v_{dc}}{20}$
4	$\pm\frac{3v_{dc}}{3}$	$\pm\frac{3v_{dc}}{5}$	$\pm\frac{3v_{dc}}{6}$	$\pm\frac{3v_{dc}}{10}$	$\pm\frac{3v_{dc}}{12}$	$\pm\frac{3v_{dc}}{20}$
5	-	$\pm\frac{4v_{dc}}{5}$	$\pm\frac{4v_{dc}}{6}$	$\pm\frac{4v_{dc}}{10}$	$\pm\frac{4v_{dc}}{12}$	$\pm\frac{4v_{dc}}{20}$
6	-	$\pm\frac{5v_{dc}}{5}$	$\pm\frac{5v_{dc}}{6}$	$\pm\frac{5v_{dc}}{10}$	$\pm\frac{5v_{dc}}{12}$	$\pm\frac{5v_{dc}}{20}$
7	-	-	$\pm\frac{6v_{dc}}{6}$	$\pm\frac{6v_{dc}}{10}$	$\pm\frac{6v_{dc}}{12}$	$\pm\frac{6v_{dc}}{20}$
8	-	-	-	$\pm\frac{7v_{dc}}{10}$	$\pm\frac{7v_{dc}}{12}$	$\pm\frac{7v_{dc}}{20}$
9	-	-	-	$\pm\frac{8v_{dc}}{10}$	$\pm\frac{8v_{dc}}{12}$	$\pm\frac{8v_{dc}}{20}$
10	-	-	-	$\pm\frac{9v_{dc}}{10}$	$\pm\frac{9v_{dc}}{12}$	$\pm\frac{9v_{dc}}{20}$
11	-	-	-	$\pm\frac{10v_{dc}}{10}$	$\pm\frac{10v_{dc}}{12}$	$\pm\frac{10v_{dc}}{20}$
12	-	-	-	-	$\pm\frac{11v_{dc}}{12}$	$\pm\frac{11v_{dc}}{20}$
13	-	-	-	-	$\pm\frac{12v_{dc}}{12}$	$\pm\frac{12v_{dc}}{20}$
14	-	-	-	-	-	$\pm\frac{13v_{dc}}{20}$
15	-	-	-	-	-	$\pm\frac{14v_{dc}}{20}$
16	-	-	-	-	-	$\pm\frac{15v_{dc}}{20}$
17	-	-	-	-	-	$\pm\frac{16v_{dc}}{20}$
18	-	-	-	-	-	$\pm\frac{17v_{dc}}{20}$
19	-	-	-	-	-	$\pm\frac{18v_{dc}}{20}$
20	-	-	-	-	-	$\pm\frac{19v_{dc}}{20}$
21	-	-	-	-	-	$\pm\frac{20v_{dc}}{20}$

Table 3 and Table 4 is used to compare the three methods (PD, APOD and NCBPWM) by listing the levels of voltages that will show up in the common mode voltages when used for controlling the three- and five-level inverters, respectively.

TABLE 3: Levels of voltages that available in double ended *3-level* three-phase and five-phase inverter for different modulation techniques

SN	v_{com} Levels		PD		APOD		NCBPWM	
	3-PHASE	5-PHASE	3-PHASE	5-PHASE	3-PHASE	5-PHASE	3-PHASE	5-PHASE
1	0	0	YES	YES	YES	YES	YES	YES
2	$\pm\frac{v_{dc}}{6}$	$\pm\frac{v_{dc}}{10}$	YES	YES	NO	NO	YES	YES
3	$\pm\frac{2v_{dc}}{6}$	$\pm\frac{2v_{dc}}{10}$	NO	YES	YES	YES	NO	YES

Three-level three-phase voltage source inverter

Three-level five-phase voltage source inverter

TABLE 4: Levels of voltages that available in double ended *5-level* three-phase and five-phase inverter for different modulation techniques

SN	v_{com} Levels		PD		APOD		NCBPWM	
	3-PHASE	5-PHASE	3-PHASE	5-PHASE	3-PHASE	5-PHASE	3-PHASE	5-PHASE
1	0	0	YES	YES	YES	YES	YES	YES
2	$\pm\frac{v_{dc}}{12}$	$\pm\frac{v_{dc}}{20}$	YES	YES	NO	NO	YES	YES
3	$\pm\frac{2v_{dc}}{12}$	$\pm\frac{2v_{dc}}{20}$	YES	YES	YES	YES	YES	YES
4	$\pm\frac{3v_{dc}}{12}$	$\pm\frac{3v_{dc}}{20}$	NO	NO	NO	NO	NO	NO
5	$\pm\frac{4v_{dc}}{12}$	$\pm\frac{4v_{dc}}{20}$	NO	NO	NO	YES	NO	NO

Five-level three-phase voltage source inverter

Five-level five-phase voltage source inverter

For the *three-level inverters* of Table 3:

- it can be seen that the **APOD** has the step size of $\frac{2v_{dc}}{6}$ and $\frac{2v_{dc}}{10}$ for three- and five-phase systems respectively, which is, in both cases, **two times the unit step size $\Delta_{\mathbf{min}}v_{\mathbf{com}}$** of $\frac{v_{dc}}{6}$ and $\frac{v_{dc}}{10}$ respectively.
- In contrast, both the PD and NCBPWM methods have the step size of $\frac{v_{dc}}{6}$ and $\frac{v_{dc}}{10}$ for three- and five-phase systems, which is equal to the **unit step size $\Delta_{\mathbf{min}}v_{\mathbf{com}}$**, respectively.

For the *five-level inverters* of Table 4:

- It can be seen that the **APOD** has the step size of $\frac{2v_{dc}}{12}$ and $\frac{2v_{dc}}{20}$ for three- and five-phase systems respectively. Again, this is, in both cases, **two times the unit step size $\Delta_{\mathbf{min}}v_{\mathbf{com}}$** of $\frac{v_{dc}}{6}$ and $\frac{v_{dc}}{10}$ respectively.
- In contrast, both the **PD and NCBPWM** methods have the step size of $\frac{v_{dc}}{12}$ and $\frac{v_{dc}}{20}$ for three- and five-phase systems, which is equal to the **unit step size $\Delta_{\mathbf{min}}v_{\mathbf{com}}$**, respectively.

4. COUNTER FOR THE OCCURRENCES OF THE DIFFERENT POSSIBLE VOLTAGE LEVELS IN THE COMMON MODE VOLTAGE AND THE TRANSITIONS BETWEEN LEVELS

The same approach used in the counting of the levels for the single inverter system has been adopted and the results are shown in Table 5, Table 6 and Table 7 for three-, five- and two-level inverters, respectively.

- Number of levels:

  It can be seen that with the double ended configuration, the **number of levels of the common mode voltage that exist (out of those theoretically possible, Table 2) do decrease when compared to the single inverter system, especially for the NCBPWM method.**

- Number of transitions:
  - For the **APOD**, the number **occurrences of different levels of $v_{\mathbf{com}}$ are the same as those in the single inverter system.**
  - For the **PD and NCBPWM** methods, the **number of occurrences of the levels of $v_{\mathbf{com}}$ are twice as much**.

(Continued overleaf.)

- For a *single inverter system*, the total number of levels of v_{com} in a switching cycle is
  - $\mathbf{2(n-1)m}$ for **NCBPWM** control method (three- and five-level inverters).
  - $\mathbf{2m}$ for **SPWM** (two-level inverter)**, PD** and **APOD** (three- and five-level inverters) control methods.
- For a *double ended inverter system*, the total number of levels of v_{com} in a switching cycle is:
  - $\mathbf{2m}$ for **APOD** control method (three- and five-level inverters).
  - $\mathbf{4m}$ for **SPWM** (two-level inverter) and **PD** (three- and five-level inverters) control methods.
  - $\mathbf{4(n-1)m}$ for **NCBPWM** control method (three- and five-level inverters).

TABLE 5: Number of levels occurrences in a switching cycle in a double ended *three-level* inverter:

	3-Level		PD		APOD		NCBPWM	
SN	3-Phase	5-Phase	3-Phase	5-Phase	3-Phase	5-Phase	3-Phase	5-Phase
1	0	0	6	5	3	5	12	15
2	$\pm\frac{v_{dc}}{6}$	$\pm\frac{v_{dc}}{10}$	3+3=6	5+5=10	0	0	6+6=12	10+10=20
3	$\pm\frac{2v_{dc}}{6}$	$\pm\frac{2v_{dc}}{10}$	0	2.5+2.5=5	1.5+1.5=3	2.5+2.5=5	0	2.5+2.5=5
4	$\pm\frac{3v_{dc}}{6}$	$\pm\frac{3v_{dc}}{10}$	0	0	0	0	0	0
5	$\pm\frac{4v_{dc}}{6}$	$\pm\frac{4v_{dc}}{10}$	0	0	0	0	0	0
6	$\pm\frac{5v_{dc}}{6}$	$\pm\frac{5v_{dc}}{10}$	0	0	0	0	0	0
7	$\pm\frac{6v_{dc}}{6}$	$\pm\frac{6v_{dc}}{10}$	0	0	0	0	0	0
8	-	$\pm\frac{7v_{dc}}{10}$	-	0	-	0	-	0
9	-	$\pm\frac{8v_{dc}}{10}$	-	0	-	0	-	0
10	-	$\pm\frac{9v_{dc}}{10}$	-	0	-	0	-	0
11	-	$\pm\frac{10v_{dc}}{10}$	-	0	-	0	-	0
			$\sum 2\cdot2\cdot3 = 12$	$\sum 2\cdot2\cdot5 = 20$	$\sum 2\cdot3 = 6$	$\sum 2\cdot5 = 10$	$\sum 2\cdot 2\cdot2\cdot3 = 24$	$\sum 2\cdot2\cdot2\cdot5 = 40$

TABLE 6: Number of levels occurrences in a switching cycle in a double ended *five-level* inverter:

	5-Level		PD		APOD		NCBPWM	
SN	3-Phase	5-Phase	3-Phase	5-Phase	3-Phase	5-Phase	3-Phase	5-Phase
1	0	0	5.8	9.4	3	2.6	22.2	35
2	$\pm\frac{v_{dc}}{12}$	$\pm\frac{v_{dc}}{20}$	3+3=6	5+5=10	1.5+1.5=3	-	12 + 12 = 24	20 + 20 = 40
3	$\pm\frac{2v_{dc}}{12}$	$\pm\frac{2v_{dc}}{20}$	0.1+0.1=0.2	0.3+0.3=0.6	-	2.5+2.5=5	0.9 + 0.9 = 1.8	2.5 + 2.5 = 5
4	$\pm\frac{3v_{dc}}{12}$	$\pm\frac{3v_{dc}}{20}$	-	-	-	-	-	-
5	$\pm\frac{4v_{dc}}{12}$	$\pm\frac{4v_{dc}}{20}$	-	-	-	1.2+1.2=2.4	-	-
			$\sum 2\cdot2\cdot3 = 12$	$\sum 2\cdot2\cdot5 = 20$	$\sum 2\cdot3 = 6$	$\sum 2\cdot5 = 10$	$\sum 2\cdot2\cdot4\cdot3 = 48$	$\sum 2\cdot2\cdot4\cdot5 = 80$

From the tables 2 and 7 it can be seen that the step size remains the same ($\frac{v_{dc}}{3}$) as in a single inverter system since:

- $\pm\frac{x_1}{2m}\pm\frac{x_2}{2m} = \pm\frac{x_3}{m}$
- $x_1\ and\ x_2$ are odd and for the single inverter system the zero level does not exist.

TABLE 7: Number of levels occurrences in a switching cycle in a *two-level* inverter:

	2-Level		SPWM	
SN	3-Phase	5-Phase	3-Phase	5-Phase
1	0	0	6	10
2	$\pm\frac{v_{dc}}{3}$	$\pm\frac{v_{dc}}{5}$	3 + 3 = 6	5 + 5 = 10
3	$\pm\frac{2v_{dc}}{3}$	$\pm\frac{2v_{dc}}{5}$	-	0
4	$\pm\frac{3v_{dc}}{3}$	$\pm\frac{3v_{dc}}{5}$	-	0
5	-	$\pm\frac{4v_{dc}}{5}$	-	0
6	-	$\pm\frac{5v_{dc}}{5}$	-	0
			$\sum 2\cdot2\cdot3 = 12$	$\sum 2\cdot2\cdot5 = 20$

The results for the PD, APOD, NCBPWM and SPWM (for 2-level) methods have been obtained by running the simulation for different simulation times related to the switching period. When run at 166.7Ts, which is equivalent to one cycle of the fundamental waveform (60-Hz system), the average number of occurrences period was obtained. The tables showing the simulation results are attached in the Appendix B (Tables B1 through B8). The summary of these occurrences are shown in Tables 8 through 12.

TABLE 8: Summary of the total number of levels and comparison of the control methods in one cycle of the fundamental frequency for the double ended 3-level 3-phase inverter system.

Control Method	$-2x_0$	$-x_0$	0	x_0	$2x_0$	Total levels from simulation	*General expression for levels in a switching cycle*	*Total level (expected)*
PD	0	496	1000	496	0	1992	$\frac{12t_{sim}}{T_s}$	2000
APOD	247	0	500	0	248	995	$\frac{6t_{sim}}{T_s}$	1000
NCBPWM	0	997	1988	992	0	3977	$\frac{24t_{sim}}{T_s}$	4000

The total simulation time, $t_{sim} = \frac{1}{60}\ s$. The switching period, $T_s = \frac{1}{f_s} = \frac{1}{10\ kHz} = 100\ \mu s$, $x_0 = \frac{v_{dc}}{6}$

The step size, $\Delta_{\min} v_{com}$, is $\frac{v_{dc}}{6}$ for PD and NCBPWM methods whereas for APOD method, the step size is $\frac{2v_{dc}}{6}$.

TABLE 9: Summary of the total number of levels and comparison of the control methods in one cycle of the fundamental frequency for the double ended 3-level 5-phase inverter system.

Control Method	$-2x_0$	$-x_0$	0	x_0	$2x_0$	Total levels from simulation	*General expression for levels in a switching cycle*	*Total level (expected)*
PD	397	824	857	827	397	3302	$\frac{20t_{sim}}{T_s}$	3333
APOD	413	0	827	0	414	1654	$\frac{10t_{sim}}{T_s}$	1667
NCBPWM	404	1656	2506	1656	402	6624	$\frac{40t_{sim}}{T_s}$	6667

The total simulation time, $t_{sim} = \frac{1}{60}\ s$. The switching period, $T_s = \frac{1}{f_s} = \frac{1}{10\ kHz} = 100\ \mu s$, $x_0 = \frac{v_{dc}}{10}$.

The step size, $\Delta_{\min} v_{com}$, is $\frac{v_{dc}}{10}$ for PD and NCBPWM methods whreas for APOD method, the step size is $\frac{2v_{dc}}{10}$.

TABLE 10: Summary of the total number of levels and comparison of the control methods in one cycle of the fundamental frequency for the double ended 2-level 3- and 5-phase inverter systems.

Number of Phases	$-2x_0$	0	$2x_0$	Total levels from simulation	*General expression for levels in a switching cycle*	*Total level (expected)*
3	497	999	502	1998	$\frac{12t_{sim}}{T_s}$	2000
5	833	1663	830	3326	$\frac{20t_{sim}}{T_s}$	3333

The total simulation time, $t_{sim} = \frac{1}{60}\ s$. The switching period, $T_s = \frac{1}{f_s} = \frac{1}{10\ kHz} = 100\ \mu s$, $x_0 = \frac{v_{dc}}{10}$.

For three phase system, the step size, $\Delta_{\min} v_{\text{com}}$, is $\frac{v_{dc}}{3}$. Therefore, $x_0 = \frac{v_{dc}}{6}$.

For the five phase system, the step size, $\Delta_{\min} v_{\text{com}}$, is $\frac{v_{dc}}{5}$. Therefore, $x_0 = \frac{v_{dc}}{10}$.

TABLE 11: Summary of the total number of levels and comparison of the control methods in one cycle of the fundamental frequency for the double ended 5-level 3-phase inverter system.

Control Method	$-2x_0$	$-x_0$	0	x_0	$2x_0$	Total levels from simulation	*General expression for levels in a switching cycle*	*Total level (expected)*
PD	0	496	1000	496	0	1992	$\frac{12t_{sim}}{T_s}$	2000
APOD	247	0	500	0	248	995	$\frac{6t_{sim}}{T_s}$	1000
NCBPWM	0	997	1988	992	0	3977	$\frac{24t_{sim}}{T_s}$	4000

The total simulation time, $t_{sim} = \frac{1}{60}\ s$. The switching period, $T_s = \frac{1}{f_s} = \frac{1}{10\ kHz} = 100\ \mu s$, $x_0 = \frac{v_{dc}}{12}$.

The step size, $\Delta_{\min} v_{\text{com}}$, is $\frac{v_{dc}}{6}$ for PD and NCBPWM methods whereas for APOD method, the step size is $\frac{2v_{dc}}{6}$.

TABLE 12: Summary of the total number of levels and comparison of the control methods in one cycle of the fundamental frequency for the double ended 5-level 5-phase inverter system.

Control Method	$-4x_0$	$-3x_0$	$-2x_0$	$-x_0$	0	x_0	$2x_0$	$3x_0$	$4x_0$	Total levels from simulation	*General expression for levels in a switching cycle*	*Total level (expected)*
PD	-	-	51	829	1558	830	53	-	-	3321	$\frac{20t_{sim}}{T_s}$	3333
APOD	200	0	415	0	435	0	419	0	204	1673	$\frac{10t_{sim}}{T_s}$	1667
NCBPWM	-	-	407	3332	5849	3332	407	-	-	13327	$\frac{80t_{sim}}{T_s}$	13333

The total simulation time, $t_{sim} = \frac{1}{60}\ s$. The switching period, $T_s = \frac{1}{f_s} = \frac{1}{10\ kHz} = 100\ \mu s$, $x_0 = \frac{v_{dc}}{20}$.

The step size, $\Delta_{\min} v_{com}$, is $\frac{v_{dc}}{20}$ for PD and NCBPWM methods whereas for APOD method, the step size is $\frac{2v_{dc}}{20}$.

5. RESULTS WAVEFORMS

In the following Figs.2 through 29, the waveforms for the common mode voltages and the phase voltages are shown. For the three-phase inverters, the dc link voltage is 300 V, whereas for five-phase inverters, the dc link voltage is 500 V. the switching frequency is $f_{sw} = 10\ kHz$ and the total simulation time in all cases is $\frac{1}{60}\ s$ which represents one cycle of the fundamental voltage signal.

5.1 Phase Disposition Method for 3-Level 3-Phase VSI

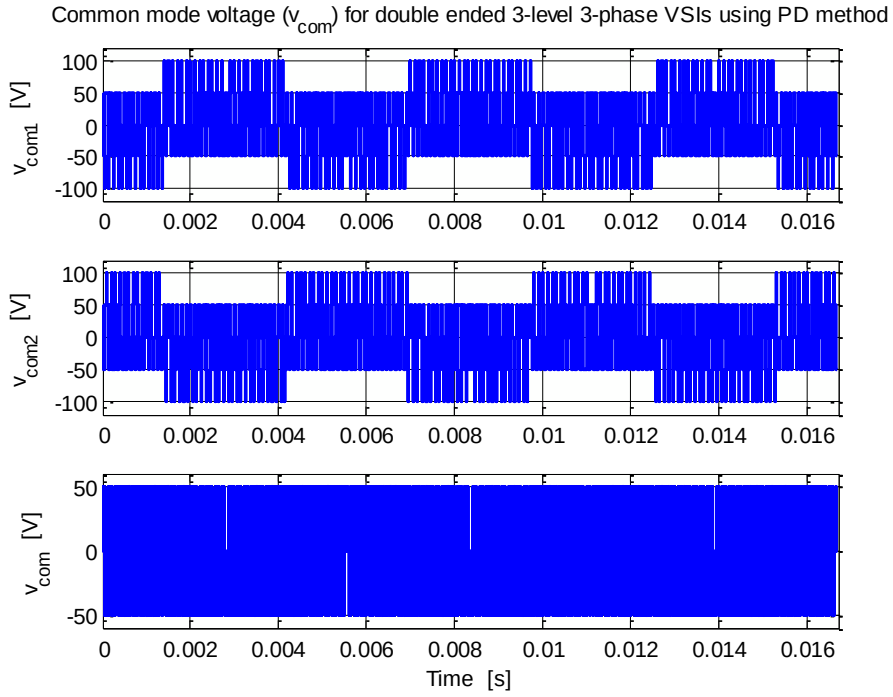

Figure 2: Common mode voltages (v_{com}) for the double ended 3-level 3-phase system using PD

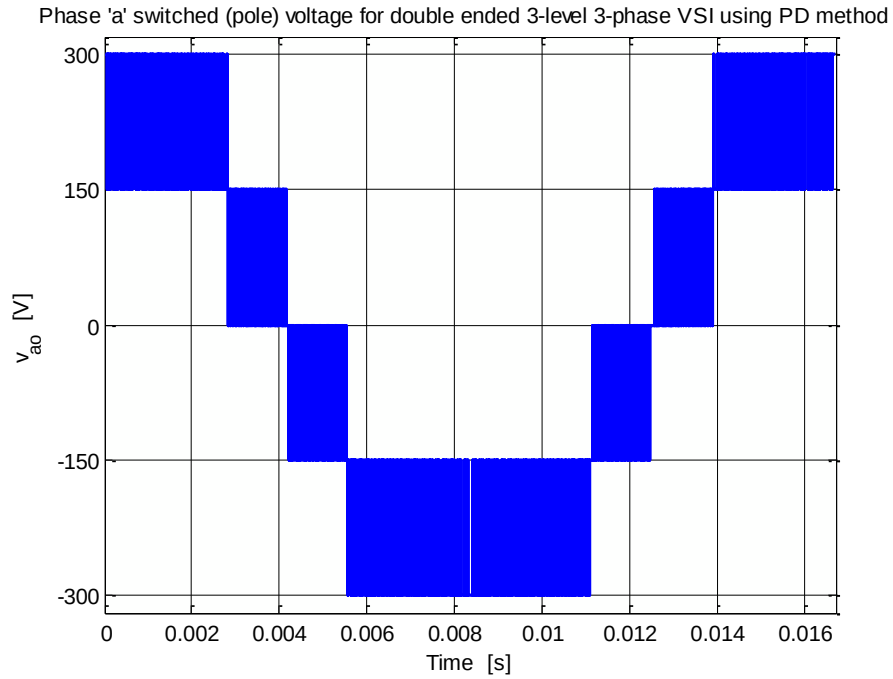

Figure 3: Resultant phase 'a' switched (pole) voltage (v_{ao}) for the double ended 3-level 3-phase system using PD

5.2 Alternate Phase Opposition Disposition (APOD) PWM for 3-Level 3-Phase VSI

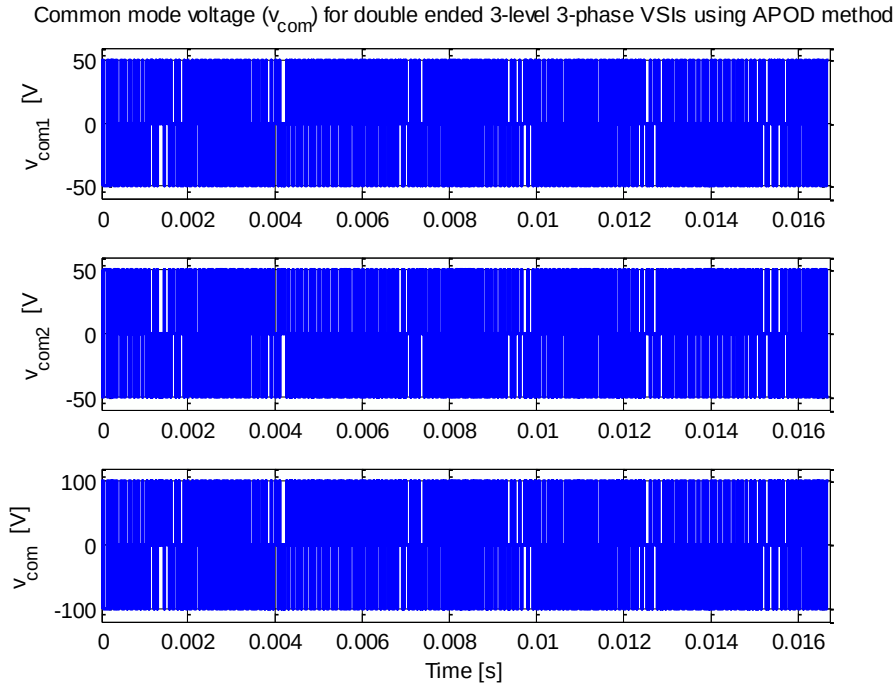

Figure 4: Common mode voltages (v_{com}) for the double ended 3-level 3-phase system using APOD

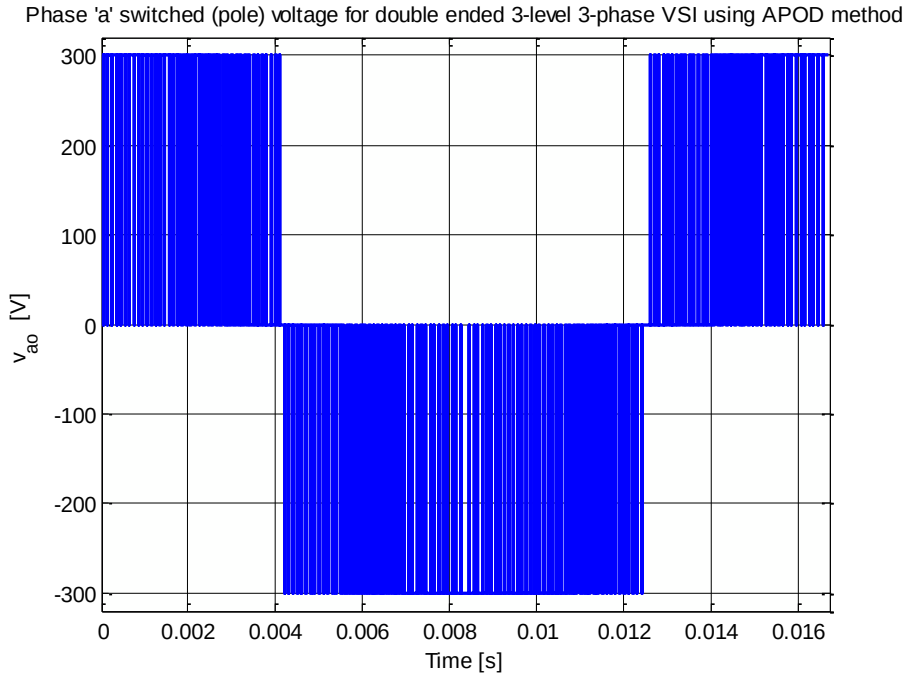

Figure 5: Resultant phase 'a' switched (pole) voltage (v_{ao}) for the double ended 3-level 3-phase system using APOD

5.3 Novel Carrier Based PWM (NCBPWM) Method for 3-Level 3-Phase VSI

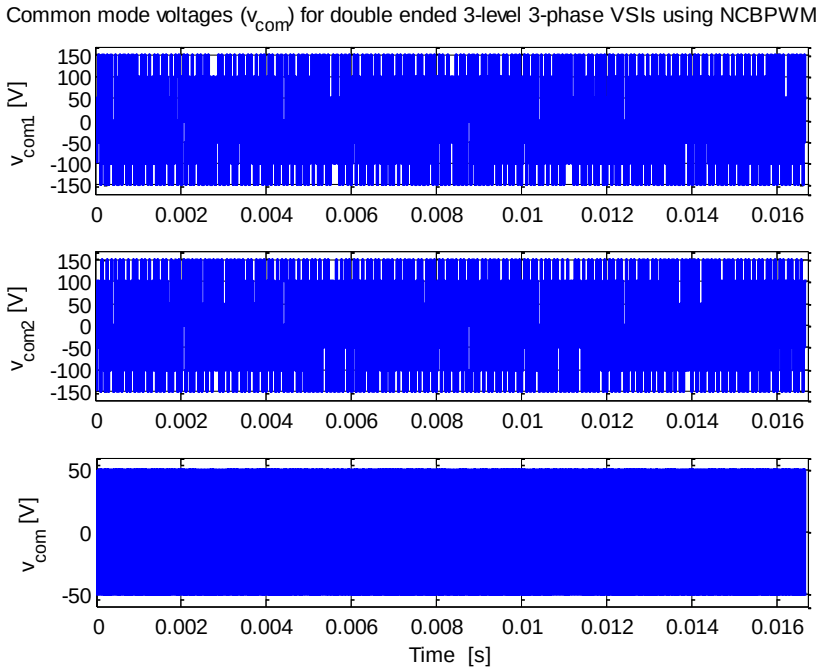

Figure 6: Common mode voltages (v_{com}) for the double ended 3-level 3-phase system using NCBPWM

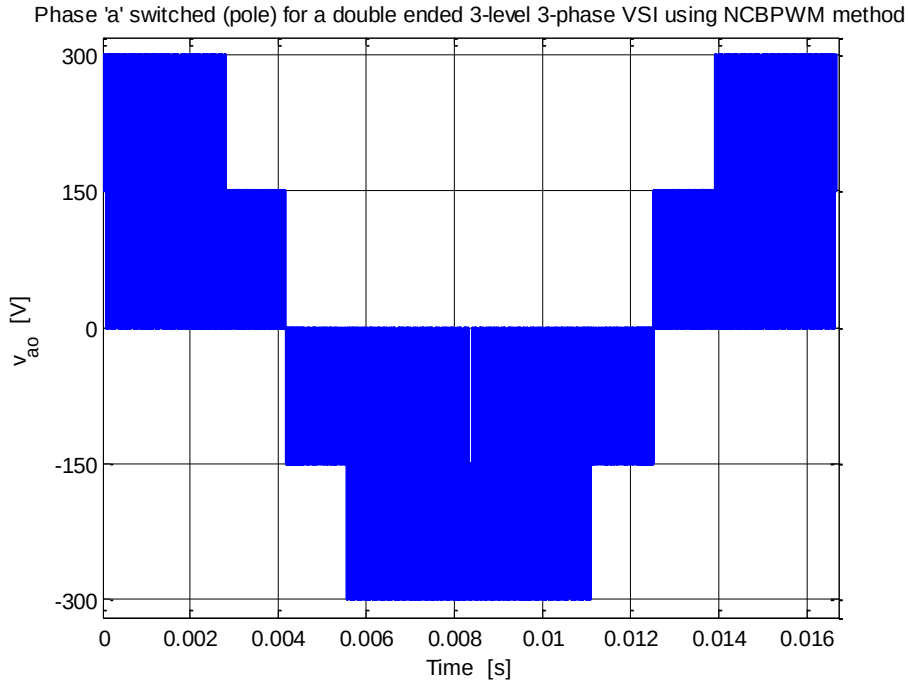

Figure 7: Resultant phase 'a' switched (pole) voltage (v_{ao}) for the double ended 3-level 3-phase system using NCBPWM

5.4 Phase Disposition Method for 3-Level 5-Phase VSI

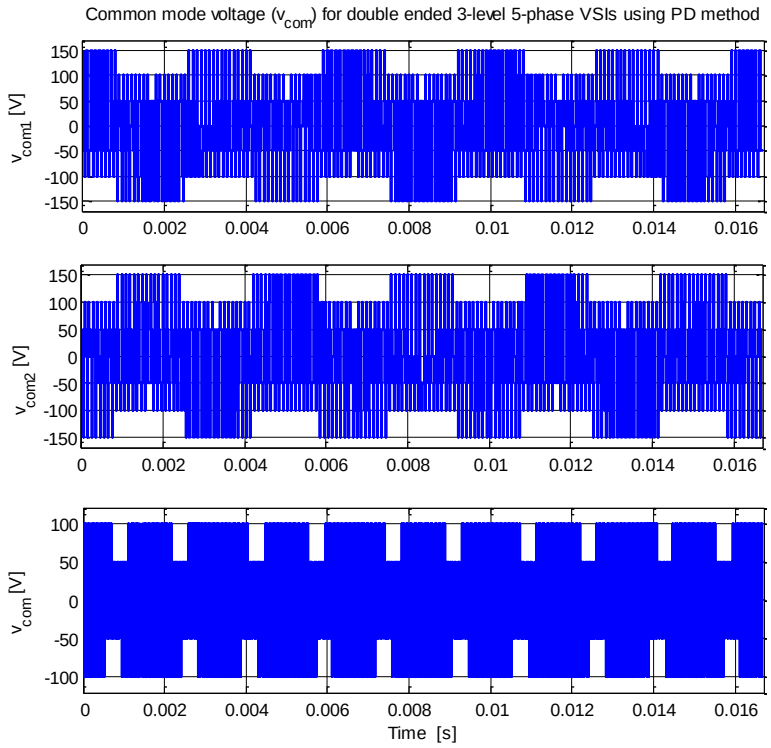

Figure 8: Common mode voltages (v_{com}) for the double ended 3-level 5-phase system using PD

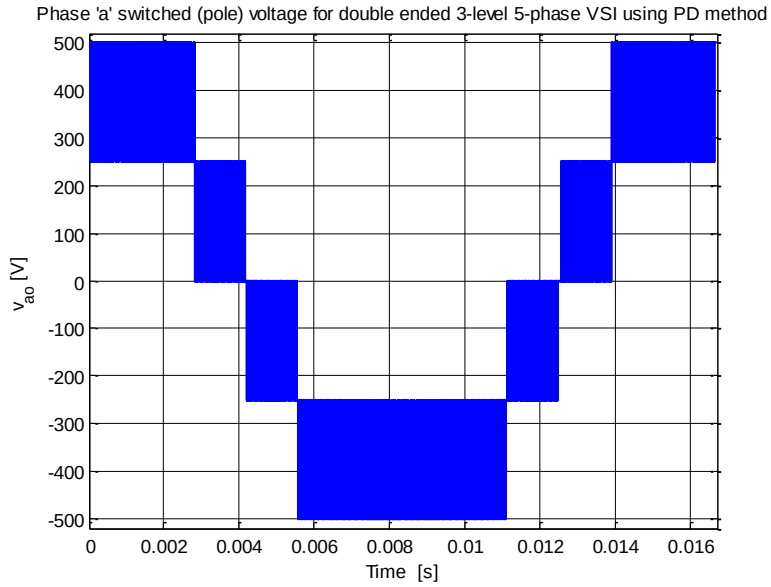

Figure 9: Resultant phase 'a' switched (pole) voltage (v_{ao}) for the double ended 3-level 5-phase system using PD

5.5 Alternate Phase Opposition Disposition (APOD) PWM for 3-Level 5-Phase VSI

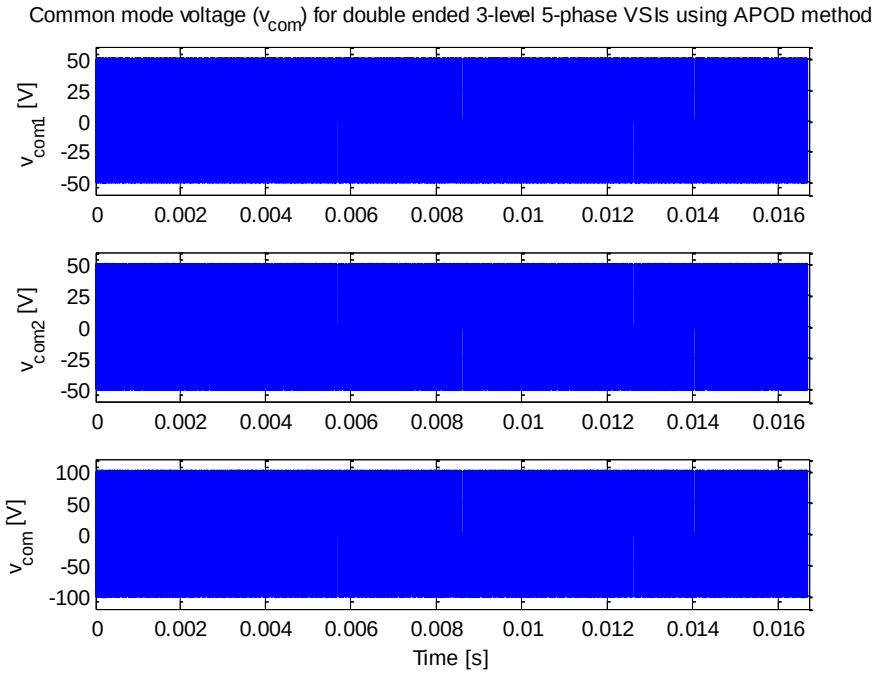

Figure 10: Common mode voltages (v_{com}) for the double ended 3-level 5-phase system using APOD

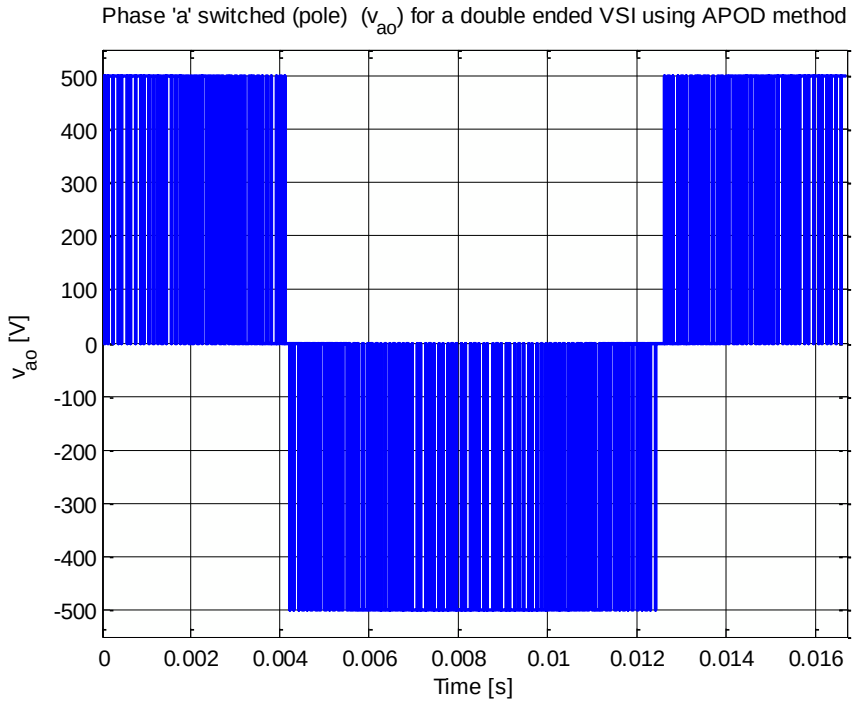

Figure 11: Resultant phase 'a' switched (pole) voltage (v_{ao}) for the double ended 3-level 5-phase system using APOD

5.6 Novel Carrier Based PWM (NCBPWM) Method for 3-Level 5-Phase VSI

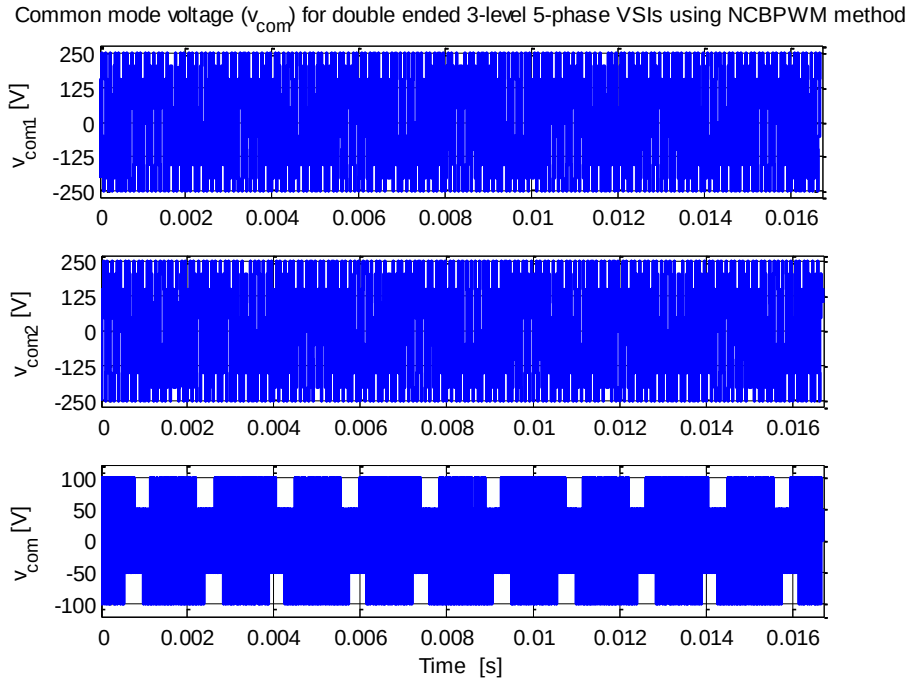

Figure 12: Common mode voltages (v_{com}) for the double ended 3-level 5-phase system using NCBPWM

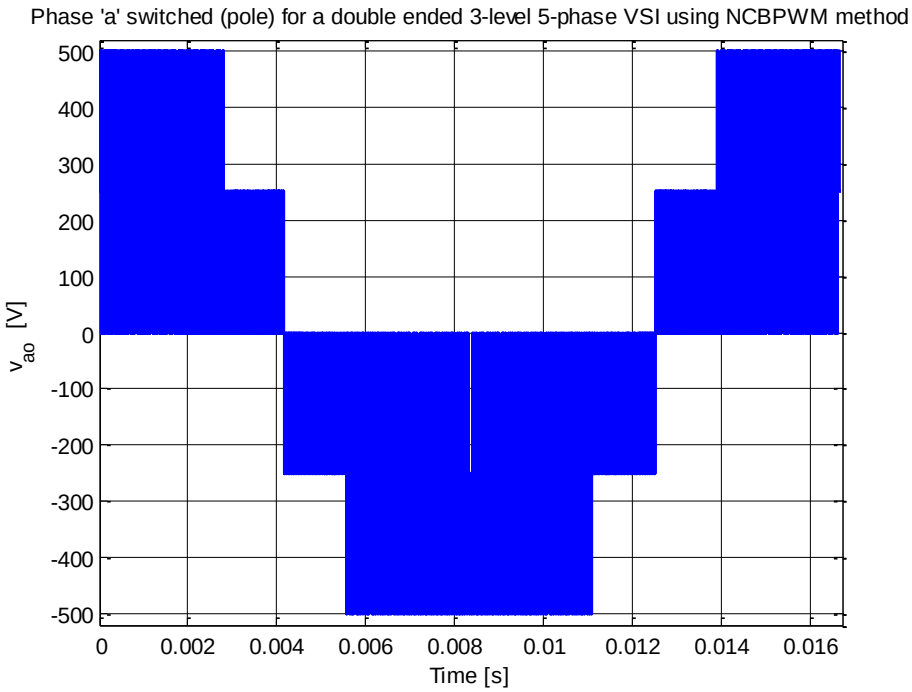

Figure 13: Resultant phase 'a' switched (pole) voltage (v_{ao}) for the double ended 3-level 5-phase system using NCBPWM

5.7 Sinusoidal PWM (SPWM) Method for 2-Level 3-Phase VSI

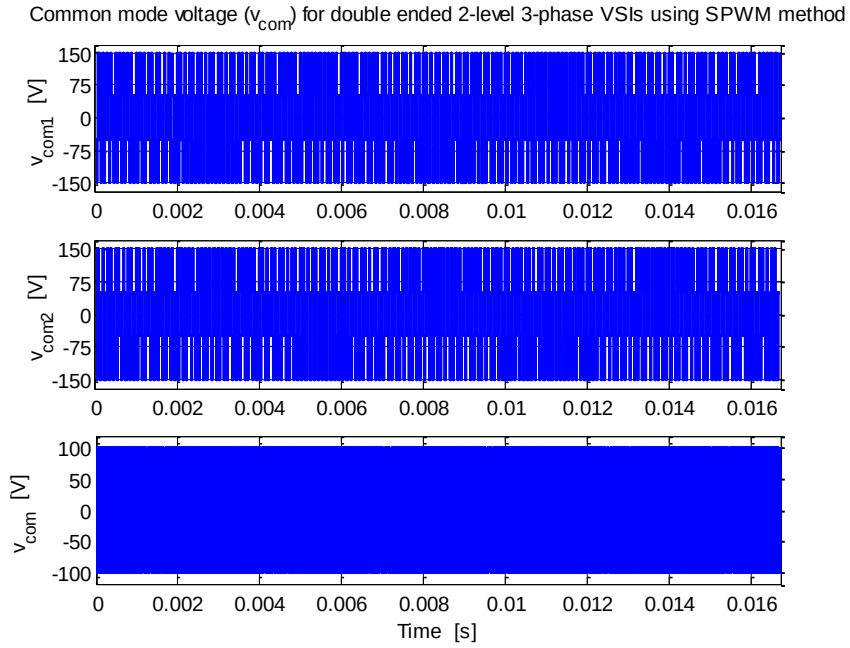

Figure 14: Common mode voltages (v_{com}) for the double ended 2-level 3-phase system using SPWM

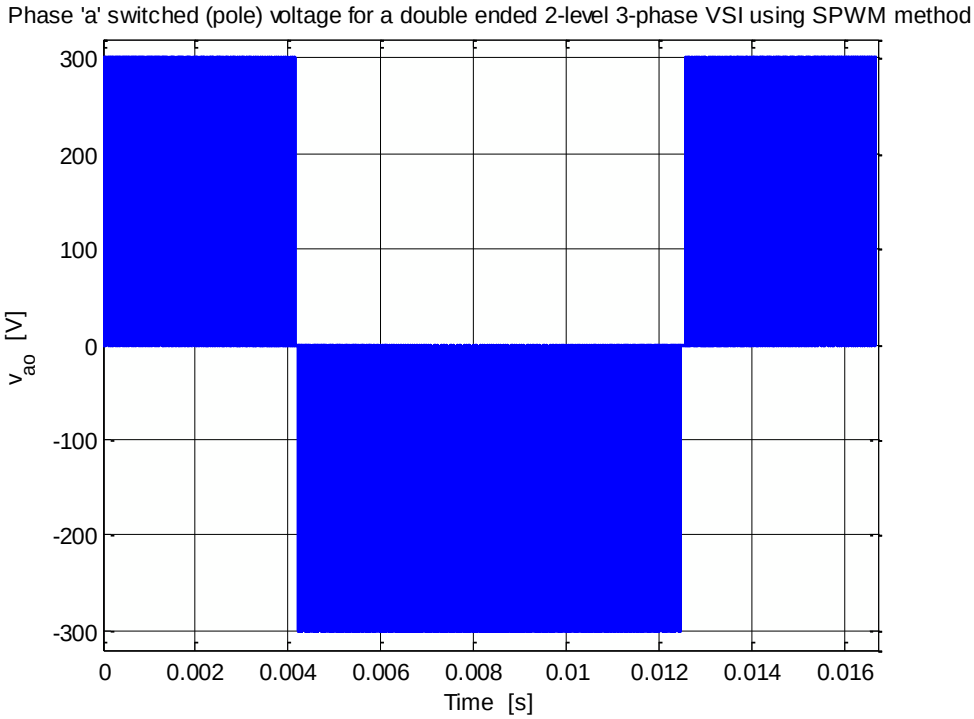

Figure 15: Resultant phase 'a' switched (pole) voltage (v_{ao}) for the double ended 2-level 3-phase system using SPWM

5.8 Sinusoidal PWM (SPWM) Method for 2-Level 3-Phase VSI

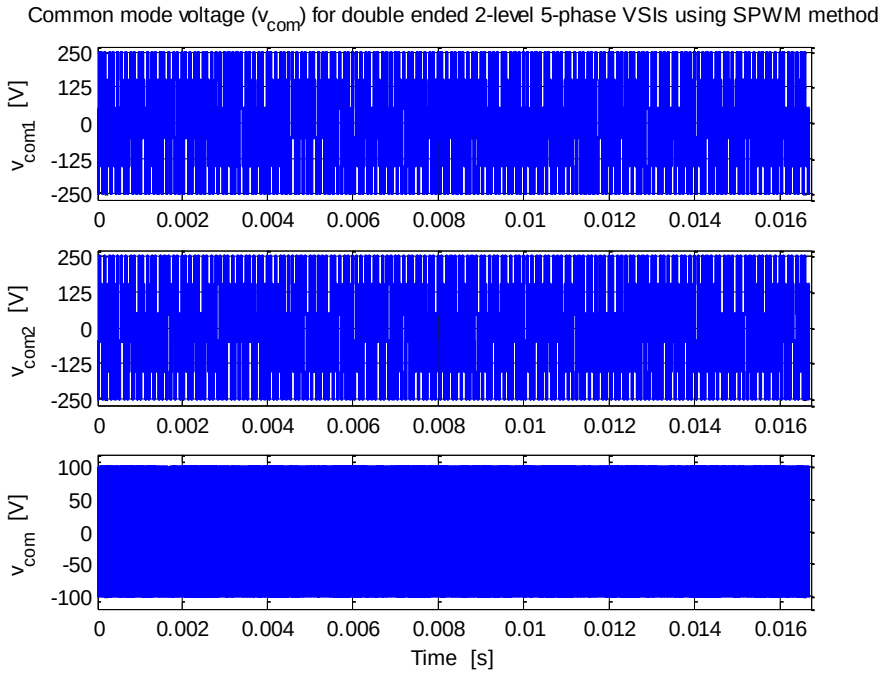

Figure 16: Common mode voltages (v_{com}) for the double ended 2-level 5-phase system using SPWM

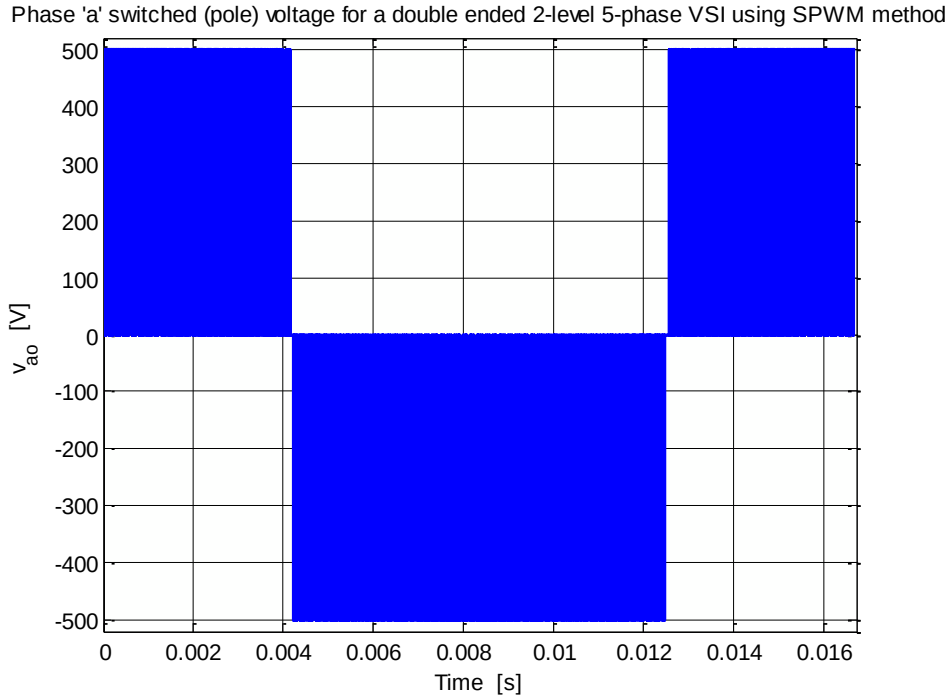

Figure 17: Resultant phase 'a' switched (pole) voltage (v_{ao}) for the double ended 2-level 5-phase system using SPWM

5.9 Phase Disposition Method for 5-Level 3-Phase VSI

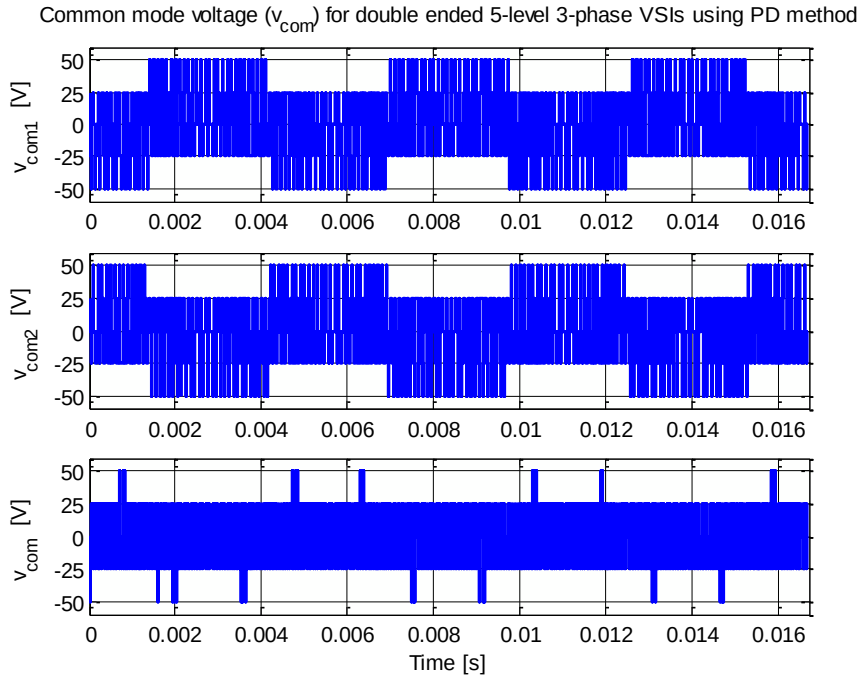

Figure 18: Common mode voltages (v_{com}) for the double ended 5-level 3-phase system using PD

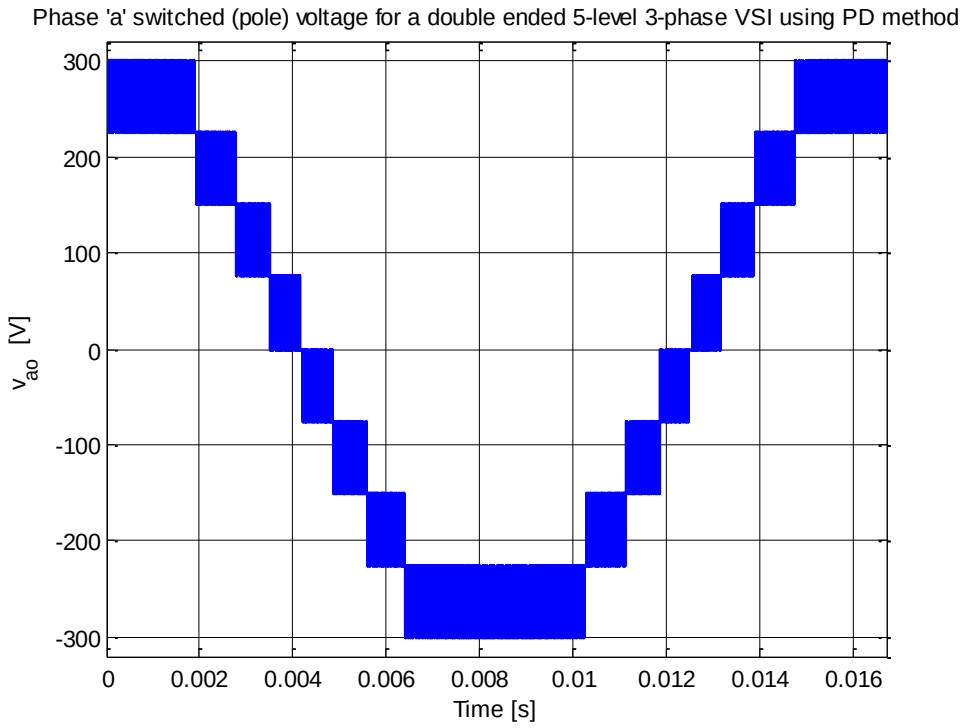

Figure 19: Resultant phase 'a' switched (pole) voltage (v_{ao}) for the double ended 5-level 3-phase system using PD

5.10 Alternate Phase Opposition Disposition (APOD) PWM for 5-Level 3-Phase VSI

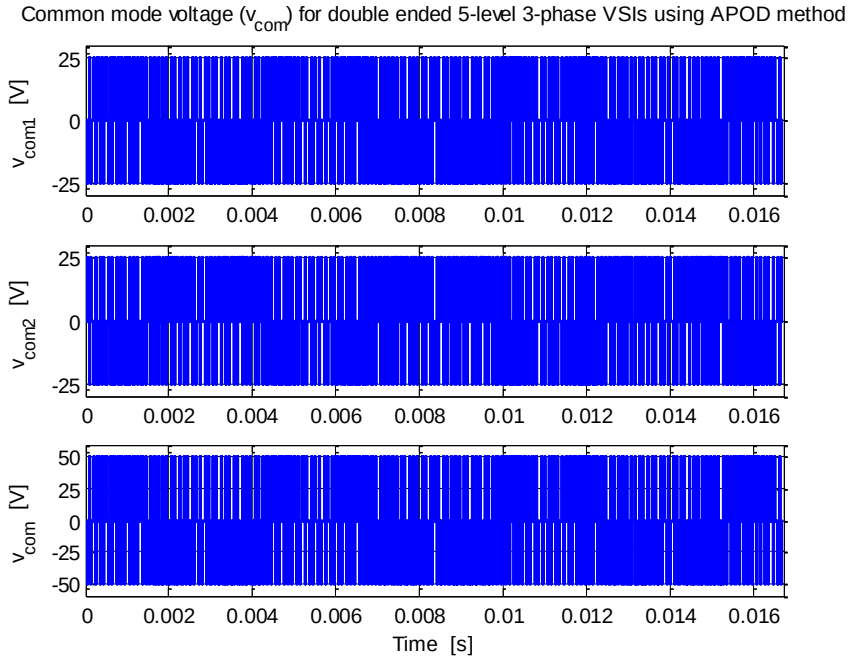

Figure 20: Common mode voltages (v_{com}) for the double ended 5-level 3-phase system using APOD

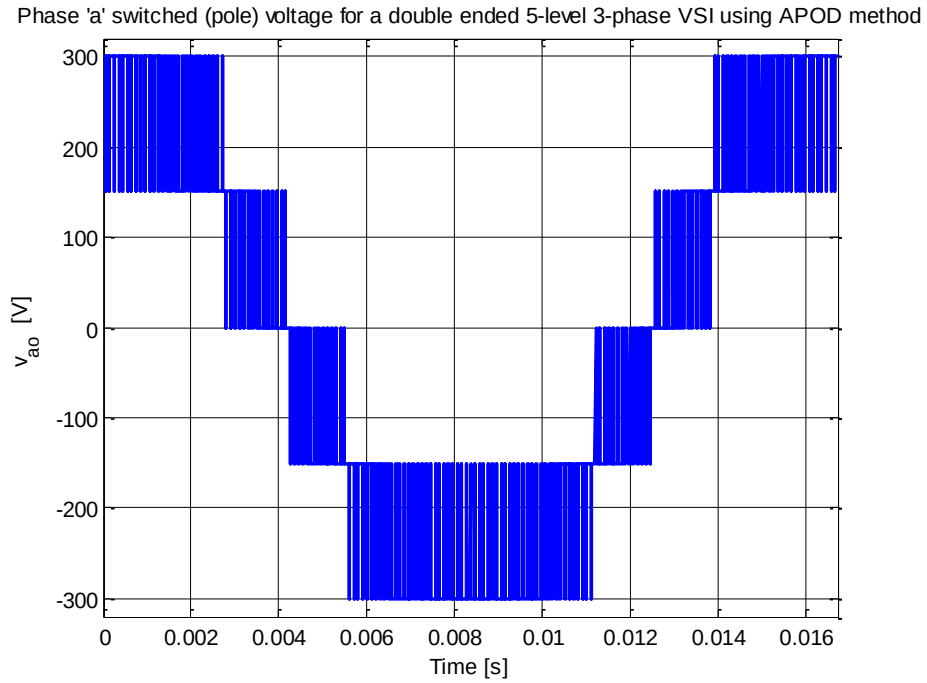

Figure 21: Resultant phase 'a' switched (pole) voltage (v_{ao}) for the double ended 5-level 3-phase system using APOD

5.11 Novel Carrier Based PWM (NCBPWM) Method for 5-Level 3-Phase VSI

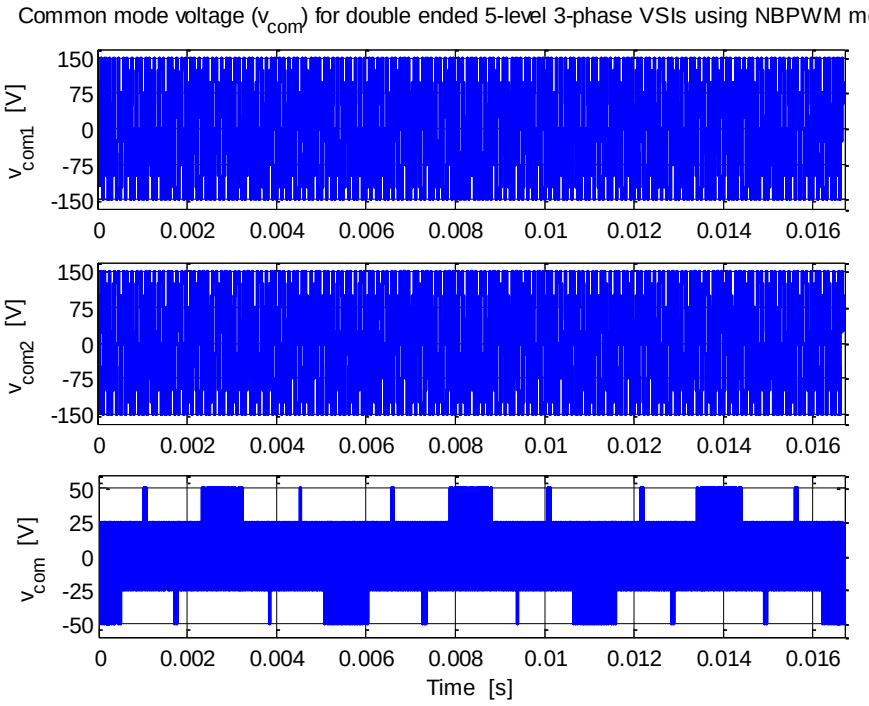

Figure 22: Common mode voltages (v_{com}) for the double ended 5-level 3-phase system using NCBPWM

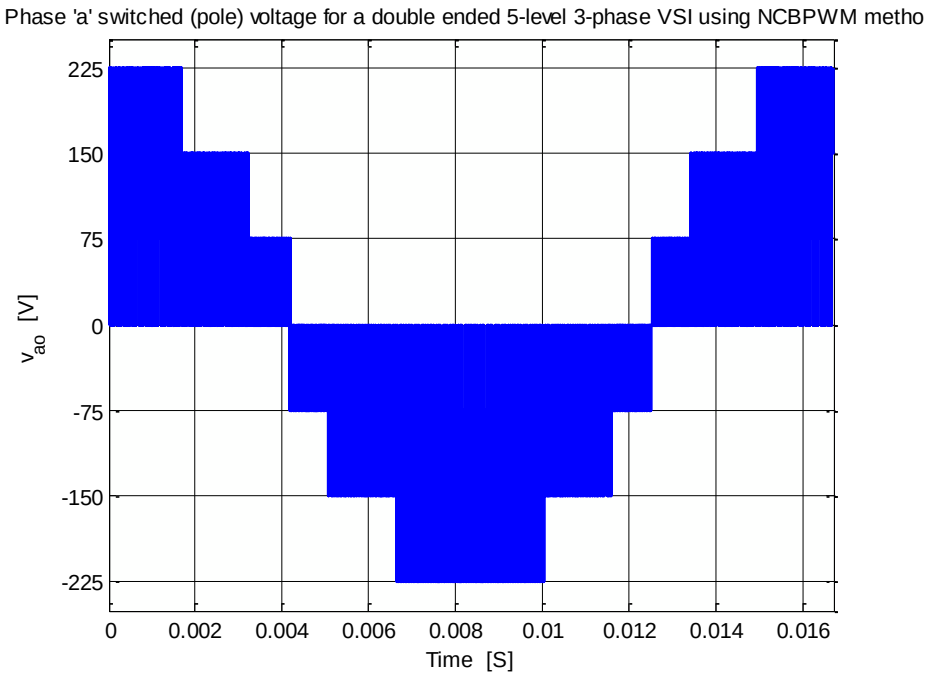

Figure 23: Resultant phase 'a' switched (pole) voltage (v_{ao}) for the double ended 5-level 3-phase system using NCBPWM

5.12 Phase Disposition Method for 5-Level 5-Phase VSI

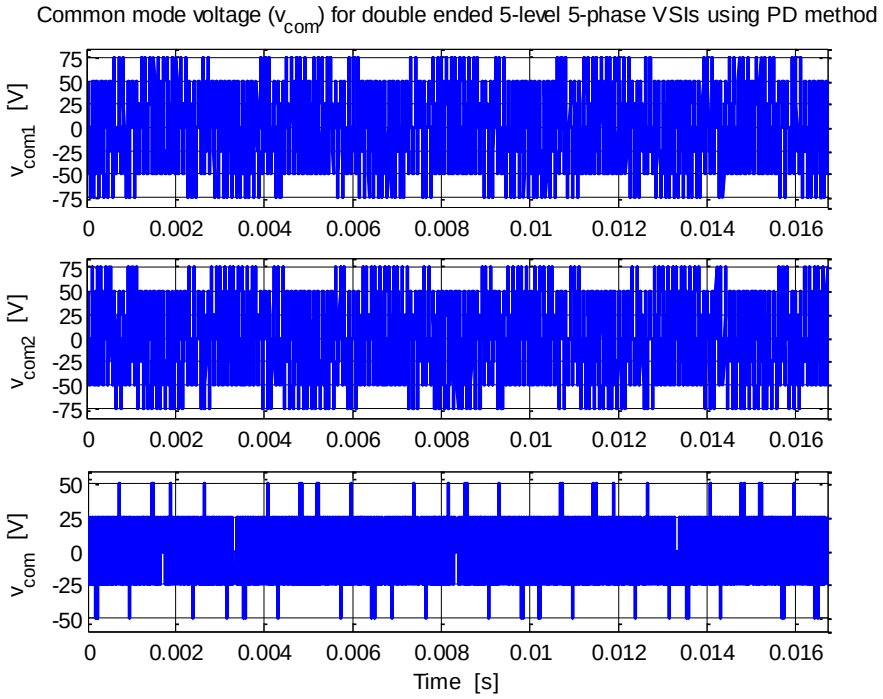

Figure 24: Common mode voltages (v_{com}) for the double ended 5-level 5-phase system using PD

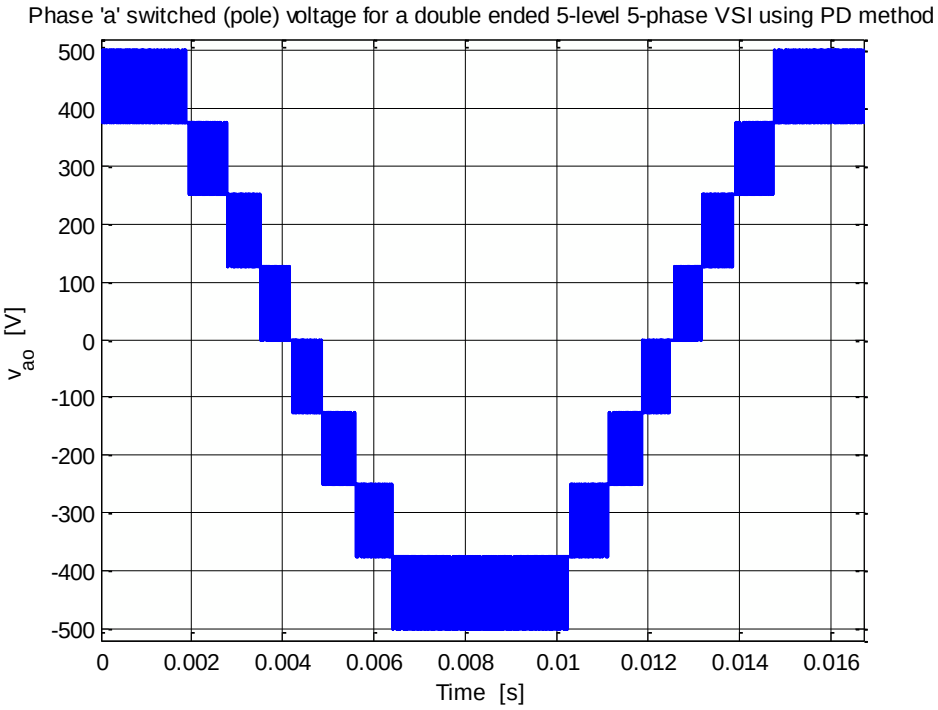

Figure 25: Resultant phase 'a' switched (pole) voltage (v_{ao}) for the double ended 5-level 5-phase system using PD

5.13 Alternate Phase Opposition Disposition (APOD) PWM for 5-Level 5-Phase VSI

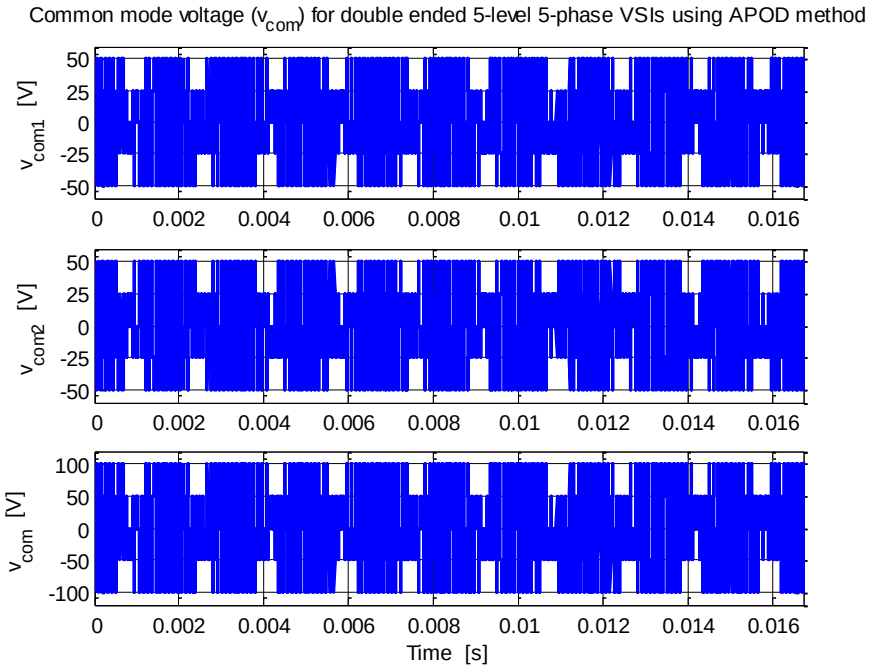

Figure 26: Common mode voltages (v_{com}) for the double ended 5-level 5-phase system using APOD

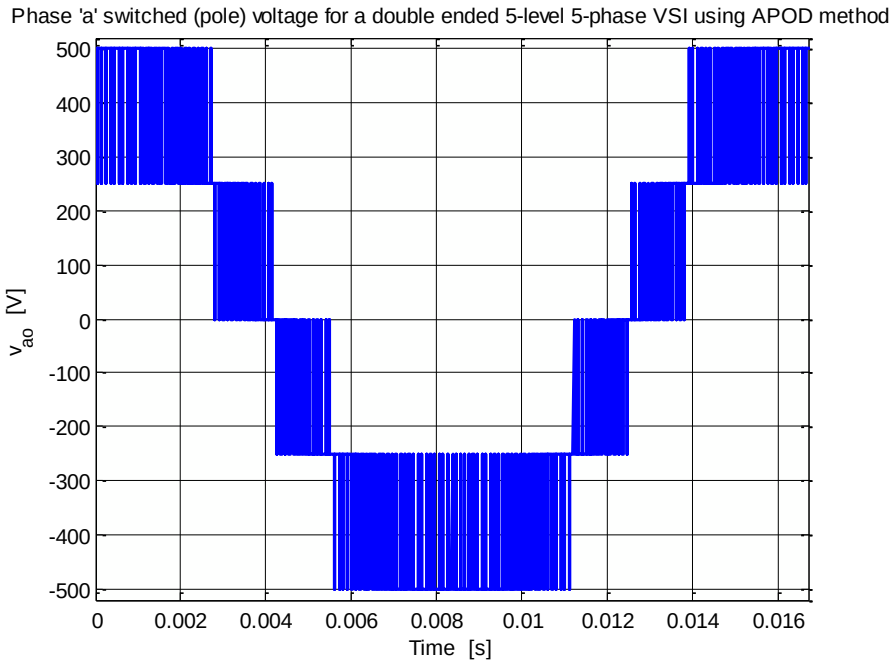

Figure 27: Resultant phase 'a' switched (pole) voltage (v_{ao}) for the double ended 5-level 5-phase system using APOD

5.14 Novel Carrier Based PWM (NCBPWM) Method for 5-Level 5-Phase VSI

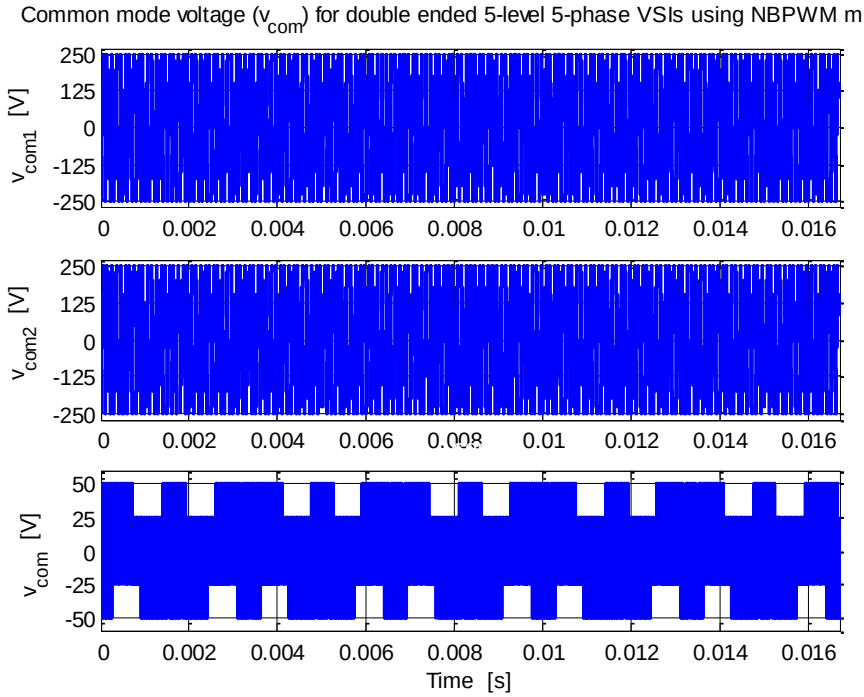

Figure 28: Common mode voltages (v_{com}) for the double ended 5-level 5-phase system using NCBPWM

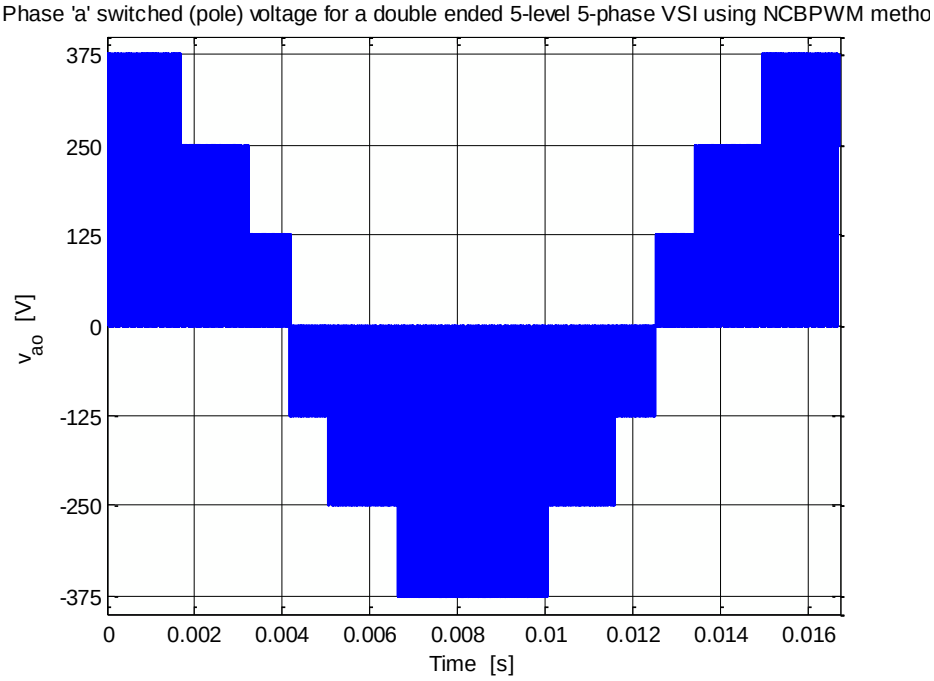

Figure 29: Resultant phase 'a' switched (pole) voltage (v_{ao}) for the double ended 5-level 5-phase system using NCBPWM

6. CONCLUSION

The analysis of the common mode voltage in the double ended (dual) two-, three- and five-level diode-clamped three- and five-phase inverter systems has been presented. Except for the NCBPWM, from the results it can be observed that for the same dc link voltage supply on both inverters, the theoretical maximum common mode output voltage is twice as much as that of the single inverter system, with the maximum and minimum voltage levels being v_{dc} and $-v_{dc}$, respectively. For the NCBPWM method the maximum and minimum voltage levels are $0.75v_{dc}$ and $-0.75v_{vdc}$, respectively.

For more details, see pages 2, 5, and 6.

APPENDIX

TABLE B1: NUMBER OF VOLTAGE LEVELS IN COMMON MODE VOLTAGE FOR A DOUBLE END 3-LEVEL 3-PHASE VSI USING PHASE DISPOSITION (PD) METHOD

S/N	t_{start}	t_{end}	$-x_0$	0	x_0	Total Levels	k	$t_{sim}=kT_s$	$12t_{sim}/T_s$
1	0	Ts	2	6	4	12	1	0.0001	12
2	0	2Ts	4	12	8	24	2	0.0002	24
3	0	3Ts	6	18	12	36	3	0.0003	36
4	0	4Ts	8	24	16	48	4	0.0004	48
5	0	5Ts	10	30	20	60	5	0.0005	60
6	0	6Ts	12	36	24	72	6	0.0006	72
7	0	7Ts	14	42	28	84	7	0.0007	84
8	0	8Ts	16	48	32	96	8	0.0008	96
9	0	9Ts	18	54	36	108	9	0.0009	108
10	0	10Ts	20	60	40	120	10	0.001	120
11	0	20Ts	52	120	68	240	20	0.002	240
12	0	30Ts	92	180	87	359	30	0.003	360
13	0	40Ts	132	240	107	479	40	0.004	480
14	0	50Ts	156	300	143	599	50	0.005	600
15	0	60Ts	175	360	183	718	60	0.006	720
16	0	70Ts	195	420	223	838	70	0.007	840
17	0	80Ts	235	480	243	958	80	0.008	960
18	0	90Ts	275	540	262	1287	90	0.009	1080
19	0	100Ts	310	600	287	1197	100	0.01	1200
20	0	166.7Ts	496	1000	496	1992	166.7	0.01667	2000

$$T_s = 100\ \mu s$$

$x_0 = \Delta_{\min} v_{\text{com}}$, which is $\frac{v_{dc}}{6}$ in this case

TABLE B2: NUMBER OF VOLTAGE LEVELS IN COMMON MODE VOLTAGE FOR A DOUBLE END 3-LEVEL 5-PHASE VSI USING PHASE DISPOSITION (PD) METHOD

S/N	t_{start}	t_{end}	$-2x_0$	$-x_0$	0	x_0	$2x_0$	Total Levels	k	$t_{sim}=kT_s$	$20t_{sim}/T_s$
1	0	Ts	2	4	4	6	4	20	1	0.0001	20
2	0	2Ts	4	8	8	12	8	40	2	0.0002	40
3	0	3Ts	6	12	12	18	12	60	3	0.0003	60
4	0	4Ts	8	16	16	24	16	80	4	0.0004	80
5	0	5Ts	10	20	20	30	20	100	5	0.0005	100
6	0	6Ts	11	24	25	36	24	120	6	0.0006	120
7	0	7Ts	11	28	31	42	28	140	7	0.0007	140
8	0	8Ts	11	32	40	48	29	160	8	0.0008	160
9	0	9Ts	11	39	50	51	29	180	9	0.0009	180
10	0	10Ts	14	45	57	55	29	200	10	0.001	200
11	0	20Ts	52	103	99	95	47	396	20	0.002	400
12	0	30Ts	72	152	158	145	67	594	30	0.003	600
13	0	40Ts	90	192	200	204	106	792	40	0.004	800
14	0	50Ts	119	247	257	248	119	990	50	0.005	1000
15	0	60Ts	147	302	314	293	134	1190	60	0.006	1200
16	0	70Ts	165	342	356	351	172	1386	70	0.007	1400
17	0	80Ts	185	392	415	400	192	1584	80	0.008	1600
18	0	90Ts	224	451	457	440	210	1782	90	0.009	1800
19	0	100Ts	238	495	514	495	238	1980	100	0.01	2000
20	0	166.7Ts	397	824	857	827	397	3302	166.7	0.01667	3333

$$T_s = 100\ \mu s$$

$x_0 = \Delta_{\min} v_{\text{com}}$, which is $\frac{v_{dc}}{10}$ in this case

TABLE B3: NUMBER OF VOLTAGE LEVELS IN COMMON MODE VOLTAGE FOR A DOUBLE END 3-LEVEL 3-PHASE VSI USING ALTERNATE PHASE OPPOSITION DISPOSITION (APOD) METHOD

S/N	t_{start}	t_{end}	$-2x_0$	$-x_0$	0	x_0	$2x_0$	Total Levels	k	$t_{sim}=kT_s$	$6t_{sim}/T_s$
1	0	Ts	1	0	3	0	2	6	1	0.0001	6
2	0	2Ts	2	0	6	0	4	12	2	0.0002	12
3	0	3Ts	3	0	9	0	6	18	3	0.0003	18
4	0	4Ts	4	0	12	0	8	24	4	0.0004	24
5	0	5Ts	5	0	15	0	10	30	5	0.0005	30
6	0	6Ts	6	0	18	0	12	36	6	0.0006	36
7	0	7Ts	7	0	21	0	14	42	7	0.0007	42
8	0	8Ts	8	0	24	0	16	48	8	0.0008	48
9	0	9Ts	9	0	27	0	18	54	9	0.0009	54
10	0	10Ts	10	0	30	0	20	60	10	0.001	60
11	0	20Ts	25	0	60	0	35	120	20	0.002	120
12	0	30Ts	44	0	90	0	45	179	30	0.003	180
13	0	40Ts	64	0	120	0	55	239	40	0.004	240
14	0	50Ts	77	0	150	0	72	299	50	0.005	300
15	0	60Ts	87	0	180	0	91	358	60	0.006	360
16	0	70Ts	97	0	210	0	111	418	70	0.007	420
17	0	80Ts	117	0	240	0	121	478	80	0.008	480
18	0	90Ts	136	0	270	0	131	537	90	0.009	540
19	0	100Ts	153	0	300	0	144	597	100	0.01	600
20	0	166.7Ts	247	0	500	0	248	995	166.7	0.01667	1000

$$T_s = 100\ \mu s$$

$x_0 = \Delta_{\min} v_{\text{com}}$, which is $\frac{v_{dc}}{6}$ in this case

TABLE B4: NUMBER OF VOLTAGE LEVELS IN COMMON MODE VOLTAGE FOR A DOUBLE END 3-LEVEL 5-PHASE VSI USING ALTERNATE PHASE OPPOSITION DISPOSITION (APOD) METHOD

S/N	t_{start}	t_{end}	$-2x_0$	$-x_0$	0	x_0	$2x_0$	Total Levels	k	$t_{sim}=kT_s$	$10t_{sim}/T_s$
1	0	Ts	2	0	5	0	3	10	1	0.0001	10
2	0	2Ts	4	0	10	0	6	20	2	0.0002	20
3	0	3Ts	6	0	15	0	9	30	3	0.0003	30
4	0	4Ts	8	0	20	0	12	40	4	0.0004	40
5	0	5Ts	10	0	25	0	15	50	5	0.0005	50
6	0	6Ts	12	0	30	0	18	60	6	0.0006	60
7	0	7Ts	14	0	35	0	21	70	7	0.0007	70
8	0	8Ts	16	0	40	0	24	80	8	0.0008	80
9	0	9Ts	20	0	45	0	25	90	9	0.0009	90
10	0	10Ts	23	0	50	0	27	100	10	0.001	100
11	0	20Ts	52	0	99	0	47	198	20	0.002	200
12	0	30Ts	76	0	148	0	72	296	30	0.003	300
13	0	40Ts	96	0	198	0	102	396	40	0.004	400
14	0	50Ts	124	0	248	0	124	496	50	0.005	500
15	0	60Ts	151	0	298	0	147	596	60	0.006	600
16	0	70Ts	171	0	347	0	176	694	70	0.007	700
17	0	80Ts	196	0	396	0	200	792	80	0.008	800
18	0	90Ts	226	0	446	0	220	892	90	0.009	900
19	0	100Ts	248	0	496	0	248	992	100	0.01	1000
20	0	166.7Ts	413	0	827	0	414	1654	166.7	0.01667	1667

$$T_s = 100\ \mu s$$

$x_0 = \Delta_{\min} v_{\text{com}}$, which is $\frac{v_{dc}}{10}$ in this case

TABLE B5: NUMBER OF VOLTAGE LEVELS IN COMMON MODE VOLTAGE FOR A DOUBLE END 3-LEVEL 3-PHASE VSI USING NOVEL CARRIER BASED PWM (NCBPWM) METHOD

S/N	t_{start}	t_{end}	$-x_0$	0	x_0	Total Levels	k	$t_{sim}=kT_s$	$24t_{sim}/T_s$
1	0	Ts	4	12	8	24	1	0.0001	24
2	0	2Ts	8	24	16	48	2	0.0002	48
3	0	3Ts	12	36	24	72	3	0.0003	72
4	0	4Ts	16	48	32	96	4	0.0004	96
5	0	5Ts	20	60	40	120	5	0.0005	120
6	0	6Ts	24	72	48	144	6	0.0006	144
7	0	7Ts	28	84	56	168	7	0.0007	168
8	0	8Ts	32	96	64	192	8	0.0008	192
9	0	9Ts	36	108	72	216	9	0.0009	216
10	0	10Ts	40	120	80	240	10	0.001	240
11	0	20Ts	106	240	134	480	20	0.002	480
12	0	30Ts	186	360	174	720	30	0.003	720
13	0	40Ts	266	480	214	960	40	0.004	960
14	0	50Ts	309	596	287	1192	50	0.005	1200
15	0	60Ts	349	714	365	1428	60	0.006	1440
16	0	70Ts	392	834	442	1668	70	0.007	1680
17	0	80Ts	472	954	482	1908	80	0.008	1920
18	0	90Ts	551	1073	522	2146	90	0.009	2160
19	0	100Ts	620	1193	573	2386	100	0.01	2400
20	0	166.7Ts	997	1988	992	3977	166.7	0.01667	4000

$$T_s = 100\ \mu s$$

$x_0 = \frac{1}{2}\Delta_{\min} v_{\text{com}}$, which is $\frac{v_{dc}}{6}$ in this case

TABLE B6: NUMBER OF VOLTAGE LEVELS IN COMMON MODE VOLTAGE FOR A DOUBLE END 3-LEVEL 5-PHASE VSI USING NOVEL CARRIER BASED PWM (NCBPWM) METHOD

S/N	t_{start}	t_{end}	$-2x_0$	$-x_0$	0	x_0	$2x_0$	Total Levels	k	$t_{sim}=kT_s$	$40t_{sim}/T_s$
1	0	Ts	2	8	14	12	4	40	1	0.0001	40
2	0	2Ts	4	16	28	24	8	80	2	0.0002	80
3	0	3Ts	6	24	42	36	12	120	3	0.0003	120
4	0	4Ts	8	32	56	48	16	160	4	0.0004	160
5	0	5Ts	10	40	70	60	20	200	5	0.0005	200
6	0	6Ts	12	48	84	72	24	240	6	0.0006	240
7	0	7Ts	14	56	98	84	28	280	7	0.0007	280
8	0	8Ts	16	64	112	96	32	320	8	0.0008	320
9	0	9Ts	18	72	126	108	36	360	9	0.0009	360
10	0	10Ts	20	80	140	120	40	400	10	0.001	400
11	0	20Ts	53	204	296	192	48	793	20	0.002	800
12	0	30Ts	73	304	456	292	68	1193	30	0.003	1200
13	0	40Ts	91	384	597	411	108	1591	40	0.004	1600
14	0	50Ts	121	497	752	497	121	1988	50	0.005	2000
15	0	60Ts	151	609	908	583	134	2385	60	0.006	2400
16	0	70Ts	169	689	1048	701	174	2781	70	0.007	2800
17	0	80Ts	189	789	1208	801	194	3181	80	0.008	3200
18	0	90Ts	229	908	1349	881	212	3579	90	0.009	3600
19	0	100Ts	242	994	1504	994	242	3976	100	0.01	4000
20	0	166.7Ts	404	1656	2506	1656	402	6624	166.7	0.01667	6667

$$T_s = 100\ \mu s$$

$x_0 = \frac{1}{2}\Delta_{\min} v_{\text{com}}$, which is $\frac{v_{dc}}{10}$ in this case

TABLE B7: NUMBER OF VOLTAGE LEVELS IN COMMON MODE VOLTAGE FOR A DOUBLE END 2-LEVEL 3-PHASE VSI USING SINUSOIDAL PWM (SPWM) METHOD

S/N	t_{start}	t_{end}	$-2x_0$	0	$2x_0$	Total Levels	k	$t_{sim}=kT_s$	$12t_{sim}/T_s$
1	0	Ts	2	6	4	12	1	0.0001	12
2	0	2Ts	4	12	8	24	2	0.0002	24
3	0	3Ts	6	18	12	36	3	0.0003	36
4	0	4Ts	8	24	16	48	4	0.0004	48
5	0	5Ts	10	30	20	60	5	0.0005	60
6	0	6Ts	12	36	24	72	6	0.0006	72
7	0	7Ts	14	42	28	84	7	0.0007	84
8	0	8Ts	16	48	32	96	8	0.0008	96
9	0	9Ts	18	54	36	108	9	0.0009	108
10	0	10Ts	20	60	40	120	10	0.001	120
11	0	20Ts	51	120	69	240	20	0.002	240
12	0	30Ts	91	180	89	360	30	0.003	360
13	0	40Ts	131	240	109	480	40	0.004	480
14	0	50Ts	154	300	146	600	50	0.005	600
15	0	60Ts	174	360	186	720	60	0.006	720
16	0	70Ts	194	420	226	840	70	0.007	840
17	0	80Ts	234	480	246	960	80	0.008	960
18	0	90Ts	274	540	266	1080	90	0.009	1080
19	0	100Ts	309	600	291	1200	100	0.01	1200
20	0	166.7Ts	497	999	502	1998	166.7	0.01667	2000

$$T_s = 100\ \mu s$$

$x_0 = \frac{1}{2}\Delta_{\min} v_{\text{com}}$, which is $\frac{v_{dc}}{6}$ in this case

TABLE B8: NUMBER OF VOLTAGE LEVELS IN COMMON MODE VOLTAGE FOR A DOUBLE END 2-LEVEL 5-PHASE VSI USING SINUSOIDAL PWM (SPWM) METHOD

S/N	t_{start}	t_{end}	$-2x_0$	0	$2x_0$	Total Levels	k	$t_{sim}=kT_s$	$20t_{sim}/T_s$
1	0	Ts	4	10	6	20	1	0.0001	20
2	0	2Ts	8	20	12	40	2	0.0002	40
3	0	3Ts	12	30	18	60	3	0.0003	60
4	0	4Ts	16	40	24	80	4	0.0004	80
5	0	5Ts	20	50	30	100	5	0.0005	100
6	0	6Ts	24	60	36	120	6	0.0006	120
7	0	7Ts	28	70	42	140	7	0.0007	140
8	0	8Ts	32	80	48	160	8	0.0008	160
9	0	9Ts	37	90	53	180	9	0.0009	180
10	0	10Ts	43	100	57	200	10	0.001	200
11	0	20Ts	103	200	97	400	20	0.002	400
12	0	30Ts	152	299	147	598	30	0.003	600
13	0	40Ts	192	399	207	798	40	0.004	800
14	0	50Ts	250	499	249	998	50	0.005	1000
15	0	60Ts	307	599	292	1198	60	0.006	1200
16	0	70Ts	347	699	352	1398	70	0.007	1400
17	0	80Ts	397	798	401	1596	80	0.008	1600
18	0	90Ts	457	898	441	1796	90	0.009	1800
19	0	100Ts	499	998	499	1996	100	0.01	2000
20	0	166.7Ts	833	1663	830	3326	166.7	0.01667	3333.3333

$$T_s = 100\ \mu s$$

$x_0 = \frac{1}{2}\Delta_{\min} v_{\text{com}}$, which is $\frac{v_{dc}}{10}$ in this case

Chapter 4

MANUSCRIPTS SUBMITTED FOR JOURNAL AND/OR CONFERENCE PUBLICATIONS

1. **IEEE TRANSACTIONS IAS/PELS SPECIAL ISSUE 2012: "ON THE COMMON MODE VOLTAGE IN MULTILEVEL MULTIPHASE SINGLE- AND DOUBLE-ENDED DIODE-CLAMPED VOLTAGE SOURCE INVERTER SYSTEMS"**

On the Common Mode Voltage in Multilevel Multiphase Single- and Double-Ended Diode-Clamped Voltage Source Inverter Systems

***Abstract*–Common mode voltage (CMV) in voltage source inverters (VSIs) has been well defined and is frequently referred to in the literature. The way it is analyzed is still mostly a matter of the different authors' foci. This paper proposes a metric for its analysis and applies this to thoroughly study the CMV properties intrinsic to the topologies of multilevel, multiphase, single- (SE) as well as double-ended (DE) diode-clamped VSI drive systems. Thereby, the CMV in VSIs is quantified by the number of possible levels and the step sizes between different levels, as well as the respective frequencies of occurrence. The first two are given by the number of levels and the number of phases of the inverter. Depending on the modulation (control) schemes, all possibly available or a few of these levels are present in the CMV. For a given DE system, there are approximately twice as many possible different voltage levels in the CMV and the maximum amplitude of the CMV is approximately twice as large as for the corresponding SE configuration. For both systems, the step size of the CMV is inversely proportional and the number of possible levels in the CMV proportional to the number of inverter levels and phases. It is also shown that not only the inverters with an odd number of levels can produce a zero CMV level in an SE configuration but also those with an even number of inverter levels and an even number of phases. For the DE configuration, all combinations of inverter levels and phases are able to produce the zero CMV voltage level.**

I. Introduction

Many different topologies of multilevel multiphase inverters have been proposed. In this paper, only diode-clamped multilevel voltage source inverters (VSI) are considered. Fig. 1 shows exemplarily one leg of the configuration of a three-level diode-clamped *m*-phase VSI (where *m* is the number of phases). Independent of the number of phases, the number of switching devices is the same in each leg.

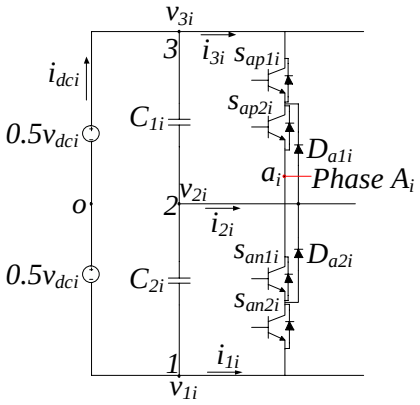

Fig. 1. One leg (leg *i*) of a three-level diode clamped *m*-phase voltage source inverter.

The common mode voltage (CMV) in single-ended (SE) two-level inverter systems has been discussed at length (see below, Sec. III). There is also an increasing amount of literature on CMV in multilevel and also some in double-ended (DE) three-phase VSI systems (see below, Sec. III and IV). However, in these papers, the CMV is mostly discussed as an element of a proposed control or modulation scheme. This paper reviews the literature on CMV in multilevel multiphase VSI systems and provides a fundamental analysis and discussion of the CMV properties intrinsic to the topologies of multilevel, multiphase, SE as well as DE diode-clamped VSI drive systems. Criteria are proposed to quantify the CMV that might occur in the system, providing an important starting point for such fundamental analysis. This metric comprises both parameters that allow quantifying the CMV properties of a given topology and such that can serve to evaluate the CMV properties of a certain modulation scheme in a quantitative way. Relative improvements with newly proposed topologies and/or schemes can thereby also be evaluated.

Providing the starting point for the analysis, the proposed CMV quantification and its justification is presented in the following section (Sec. II). This metric is then applied to first analyze SE (Sec. III) and then DE (Sec. IV) multilevel multiphase VSI systems. In the second part of the paper, the literature on CMV in multilevel multiphase VSI systems is reviewed. In view of the proposed method of quantification, it becomes even clearer that the literature discusses the CMV mostly as an element of a proposed control or modulation scheme, or–notably with two-level inverter systems–as part of a newly developed filter. The proposed criteria provide a suitable tool for an improved quantification of the merits of newly proposed systems regarding the CMV reduction.

II. Proposed Common Mode Voltage Quantification

A. Motivation: High-Frequency CMV and Inverter-Induced Bearing Currents

VSI drives are known to provide a high-frequency (HF) CMV at the output of the inverter that also appears–if no additional measures such as CMV filters are used–as a CMV at the input terminals of the connected electrical machine. As a matter of fact, an *m*-phase electrical machine supplied from a balanced *m*-phase sinusoidal voltage source will have the sum of its phase voltages equal to zero which is not the case with a machine fed from a VSI. This voltage may cause additional electromagnetic interference (EMI), additional charging of the motor cables, additional losses, as well as inverter-induced bearing currents. Such bearing currents may increase the aging rate of the bearings and hence lead to their premature failures [1] [2] [3] [4]. (Note that these bearing currents occur in addition to the "conventional" (low frequency) bearing currents that have been known for a long time [5].)

B. Classification of Mitigation Techniques

Because of the parasitic effects of the CMV on the drive and the CMV being inherent to VSIs, different methods have been investigated to reduce or eliminate the CMV, almost since VSIs have started to be more widely used. Two different approaches can be distinguished to achieve this goal,

1. Filters that do not eliminate the HF CMV at the inverter output but return it to its source, thereby eliminating its occurrence at the terminals of the electric machine,
2. Specially developed modulation and/or control schemes that aim to reduce the number of switching incidences that also entail a change of the CMV and/or the states that result in a rather high level of CMV.

C. Proposed CMV Quantification

The CMV typically changes with every switching event of the inverter. Considering the parasitic effect of inverter-induced bearing currents, the amplitude of the CMV influences both

1. The amplitude of the parasitic common mode (CM) current that, in turn, excites the so-called HF circulating bearing currents, and
2. The amplitude of the CMV that might appear across the bearings of the drive system and result in discharge bearing currents.

The work of different researchers suggests that the bearing degradation due to inverter-induced bearing currents increases with the number of current pulses a bearing is submitted to [6] [7] [8] [9] [10] [11].

Based on these fundamental relationships, the proposed quantification includes the following parameters.

1a. The number of different voltage levels that can occur theoretically $n_o v_{com}$,
1b. the number of different voltage levels that occur when a certain control scheme is used $n_o v_{com\_ctrl}$, and
1c. the frequencies of occurrence at which these different levels occur, $f\_n_o v_{com,i}$;
2a. The unit step size $\Delta_{min} v_{com}$,
2b. the step sizes that do occur Δv_{com} (which are integer multiples of $\Delta_{min} v_{com}$ and in most cases equal to $\Delta_{min} v_{com}$), and
2b. the frequencies of occurrence at which these different step sizes occur, $f\_\Delta v_{com,i}$.
3. The theoretical maximum value of the CMV, with the magnitude $|v_{com,max}|$, appearing as $\pm\, v_{com,max}$.

The parameters $|v_{com,max}|$, $n_o v_{com}$ and $\Delta_{min} v_{com}$ are related by

$$|v_{com,max}| = ((n_o v_{com} - 1) \cdot \Delta_{min} v_{com})/2 \,, \tag{1}$$

and, because of symmetry, it is $v_{com,max} = |v_{com,max}|$ and $v_{com,min} = -|v_{com,max}|$.

The three parameters $|v_{com,max}|$, $n_o v_{com}$ and $\Delta_{min} v_{com}$ are intrinsic to the topology, whereas the parameters $f\_n_o v_{com,i}$ and $f\_\Delta v_{com,i}$ are determined by the applied modulation or control scheme. Often, not all possible levels of the CMV $n_o v_{com,i}$ occur when a certain modulation scheme is used. A lot of the literature on the reduction of CMV has focused on eliminating the occurrence of high CMV levels in the output voltage (see below, Sec. V).

III. Common Mode Voltage Analysis 1: Single-Ended Inverter Drives

A. Pole (Switched) Voltage

In the following analysis, we generalize the equations that have been given for up to three-phase three-level inverters [12], [13], for *m*-phase *n*-level inverters. In an SE VSI drive system, only one *n*-level *m*-phase inverter is used. For the theoretical analysis of the CMV, it is appropriate to review the definitions of the phase switched (pole) voltage and the switching function. The switched voltage is the inverter voltage between the phase *'i'* of the leg and the mid-point of the dc source (*o*) as indicated in Fig. 1. The phase switched voltage for any inverter with *n* number of levels is given by

$$v_{io,SE} = \frac{[2S_{i,SE} - (n-1)]v_{dc}}{2(n-1)}, \tag{2}$$

where $S_{i,SE}$ represents the switching state of the inverter leg of the SE system and i is the phase ($i = a, b, c, \ldots, m$). For an n-level VSI, the switching state of the inverter leg of the SE system $S_{i,SE}$ is given by

$$S_{i,SE} = 0, 1, 2, 3, \ldots, n-1. \tag{3}$$

Table I shows the available switching functions $S_{i,SE}$ and their corresponding switched phase voltages $v_{io,SE}$ for an SE inverter drive system. The entries of the table are obtained from (2) and (3) respectively. Note that the values for $v_{io,SE}$ are given in fractions of the dc source voltage v_{dc}.

TABLE I: SWITCHING FUNCTIONS AND POLE VOLTAGES OF AN n-PHASE SE INVERTER DRIVE SYSTEM

Inverter levels	$S_{i,SE}$ | $v_{io,SE}$ in fractions of v_{dc}.							
2	0 | -½	1 | ½						
3	0 | -½	1 | 0	2 | ½					
4	0 | -½	1 | -⅔	2 | -⅓	3 | ½				
5	0 | -½	1 | -¼	2 | 0	3 | ¼	4 | ½			
6	0 | -½	1 | -3/10	2 | -1/10	3 | 1/10	4 | 3/10	5 | ½		
7	0 | -½	1 | -⅓	2 | -1/6	3 | 0	4 | 1/6	5 | ⅓	6 | ½	

An illustration of these relationships, using a three- and a five-phase system is given in the Appendix.

B. Step Sizes and Number of CMV Levels

In analogy to the three-phase system [3], [14], [15], [16], the expression of the CMV, v_{com}, for m-phase VSIs is given by *[Check again if there is truly no ref to an m-phase system? Or, at least a five phase system?]*

$$v_{com} = \frac{1}{m}\sum_{i=1}^{m} v_{io}. \tag{4}$$

For any n-level m-phase inverter, the step size of the switched voltage $\Delta v_{io,SE}$ is given by

$$\Delta v_{io,SE} = \frac{v_{dc}}{n-1}. \tag{5}$$

The minimum step size of the CMV in an n-level m-phase SE VSI $\Delta_{min}v_{com,SE}$ can be derived using (4) and (5)

$$\Delta_{min}v_{com,SE} = \frac{\Delta v_{io,SE}}{m} = \frac{v_{dc}}{m(n-1)}. \tag{6}$$

The number of theoretically possible different levels in the CMV, $n_o v_{com,SE}$, is derived from the minimum step size $\Delta_{min}v_{com,SE}$,

$$n_o v_{com,SE} = \frac{v_{dc}}{\Delta_{min}v_{com,SE}} + 1 = m(n-1) + 1. \tag{7}$$

The minimum step size of the CMV $\Delta_{min}v_{com,SE}$ decreases inversely proportionally and the number of theoretically possible different levels in the CMV $n_o v_{com,SE}$ increases linearly with the number of inverter levels n and the number of phases m. This implies a reduction in the magnitude of the rate of change of the CMV which is advantageous as far as inverter-induced bearing currents are concerned.

To illustrate the findings, Tables II and III show the values of $\Delta_{min}v_{com,SE}$ and $n_o v_{com}$ as a function of the number of phases, m, and the number of inverter levels, n, for up to ten inverter levels and ten phases. These tables have been generated using (6) and (7) respectively.

TABLE II: MINIMUM STEP SIZE OF CMV OF A SE VSI SYSTEM AS A FUNCTION OF NUMBER OF PHASES, m, AND OF INVERTER LEVELS, n

	Step size in the CMV, $\Delta_{min}v_{com}$, as a fraction of v_{dc}								
m	$n = 2$	$n = 3$	$n = 4$	$n = 5$	$n = 6$	$n = 7$	$n = 8$	$n = 9$	$n = 10$
3	1/3	1/6	1/9	1/12	1/15	1/18	1/21	1/24	1/27
4	1/4	1/8	1/12	1/16	1/20	1/24	1/28	1/32	1/36
5	1/5	1/10	1/15	1/20	1/25	1/30	1/35	1/40	1/45
6	1/6	1/12	1/18	1/24	1/30	1/36	1/42	1/48	1/54
7	1/7	1/14	1/21	1/28	1/35	1/42	1/49	1/56	1/63
8	1/8	1/16	1/24	1/32	1/40	1/48	1/56	1/64	1/72
9	1/9	1/18	1/27	1/36	1/45	1/54	1/63	1/72	1/81
10	1/10	1/20	1/30	1/40	1/50	1/60	1/70	1/80	1/90

TABLE III: NUMBER OF THEORETICALLY POSSIBLE DIFFERENT CMV LEVELS OF A SE VSI SYSTEM AS A FUNCTION OF NUMBER OF PHASES, *m*, AND INVERTER LEVELS, *n*

	Number of levels in the CMV, $n_o v_{com}$								
m	*n* = 2	*n* = 3	*n* = 4	*n* = 5	*n* = 6	*n* = 7	*n* = 8	*n* = 9	*n* = 10
3	4	7	10	13	16	19	22	25	28
4	5	9	13	17	21	25	29	33	37
5	6	11	16	21	26	31	36	41	46
6	7	13	19	25	31	37	43	49	55
7	8	15	22	29	36	43	50	57	64
8	9	17	25	33	41	49	57	65	73
9	10	19	28	37	46	55	64	73	82
10	11	21	31	41	51	61	71	81	91

Exemplarily, Table IV shows the different possible CMV voltage levels of two-, three- and five-level SE VSI configurations for three-phase and five-phase systems.

TABLE IV: CMV LEVELS IN 3- AND 5-PHASE AND 2-, 3- AND 5-LEVEL VSI SYSTEMS, AS A FRACTION OF V_{DC}.

Switching	2-Level		3-Level		5-Level	
function	3-Phase	5-Phase	3-Phase	5-Phase	3-Phase	5-Phase
1	±1/6	±1/10	0	0	0	0
2	±3/6	±3/10	±1/6	±1/10	±1/12	±1/20
3	-	±5/10	±2/6	±2/10	±2/12	±2/20
4	-	-	±3/6	±3/10	±3/12	±3/20
5	-	-	-	±4/10	±4/12	±4/20
6	-	-	-	±5/10	±5/12	±5/20
7	-	-	-	-	±6/12	±6/20
8	-	-	-	-	-	±7/20
9	-	-	-	-	-	±8/20
10	-	-	-	-	-	±9/20
11	-	-	-	-	-	±10/20

The maximum CMV for an SE *n*-level *m*-phase VSI is derived from (1), (6), and (7)

$$|v_{com,max,SE}| = (m(n-1)+1-1)\frac{v_{dc}}{m(n-1)}\frac{1}{2} = \frac{v_{dc}}{2}. \tag{8}$$

C. Even and Odd Number of Inverter Levels and Phases

In the literature, it has been stated that the use of odd number of inverter levels not only allows to generate zero-voltage levels in the switched phase voltage $v_{io,SE}$, but also some switching states that result in zero CMV. In this subsection, the four possible combinations of even and odd number of inverter levels and phases are analyzed in order to identify if generalizations can be made.

For an odd number of levels n_{odd}, the term $(n-1)$ in the numerator of (2) is always even. Therefore, a zero CMV level will be produced when $2S_i = (n-1)$. As for an even number of levels n_{even}, the term $(n-1)$ in the numerator of (2) is always odd. Since $2S_i$ is always even and cannot equal $(n-1)$. It is thus not possible to obtain a non-zero-voltage level in the inverter output phase and CM voltages. Since for n_{even}, the absolute value of the numerator of (2), i.e. $[2S_i-(n-1)]$, is also odd. This gives different results for the existence or non-existence of zero-voltage levels in the CMV for even and odd phase numbers, $m_{even}$and m_{odd}. The existence (or non-existence) of the zero-voltage levels in the phase and CMV of a VSI depend on the combination of the number of inverter levels *n* and phases *m* and can be classified as described in the following.

C-1) Odd number of phases (m_{odd}) and odd number of inverter levels (n_{odd}): There exists a zero-voltage level in both the switched phase output and in the CMV. For example, when $n = 3$, $m = 3$, $S_i = 3$, $v_{io} = 0$. Also, when $[S_{abc}] = [1\ 0\ 2]$, $v_{ao} = 0$, $v_{bo} = -\frac{v_{dc}}{2}$ and $v_{co} = \frac{v_{dc}}{2}$, giving $v_{com} = 0$.

C-2) Even number of phases (m_{even}) and odd number of inverter levels (n_{odd}): There exists a zero-voltage level in both the switched phase output and in the CMV. For example, when $n = 3$, $m = 4$, $S_i = 1$, $v_{io} = 0$. Also, when $[S_{abcd}] = [1\ 0\ 2\ 1]$, $v_{ao} = 0$, $v_{bo} = -\frac{v_{dc}}{2}$, $v_{co} = \frac{v_{dc}}{2}$ and $v_{do} = 0$, giving $v_{com} = 0$.

C-3) Odd number of phases (m_{odd}) and even number of inverter levels (n_{even}): A zero-voltage level does not exist; neither in the switched phase output nor in the CMV, as it has been claimed in the literature [16], [17].

C-4) Even number of phases (m_{even}) and even number of inverter levels (n_{even}): Although there are no states that would produce a zero-voltage level in the phase output voltages v_{io}, there are possibilities of obtaining a zero-voltage level in the CMV. For example when $n = 4$, $m = 4$ and the inverter switching state is $[S_{abcd}] = [3\ 2\ 1\ 0]$, $v_{ao} = \frac{v_{dc}}{2}$, $v_{bo} = \frac{v_{dc}}{6}$, $v_{co} = -\frac{v_{dc}}{6}$ and $v_{do} = -\frac{v_{dc}}{2}$, giving v_{com}.

IV. Common Mode Voltage Analysis 2: Double-Ended Inverter Drives

A. Pole (Switched) Voltage

In a double-ended (also "dual") VSI drive system, two inverters are each connected at either end of the stator winding of the electric machine. An illustration for such as system is depicted in Fig. 2.

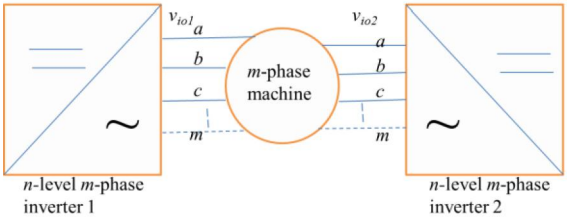

Figure 2. Schematic diagram of a DE inverter drive system. *[This is just a quick sketch. We will polish the quality.]*

The expressions of the phase switched voltage, $v_{io,DE}$, and the CMV, v_{com}, in the DE VSI system are given as [18]

$$v_{io,DE} = v_{io1} - v_{io2}, \tag{9}$$

$$v_{com} = v_{com1} - v_{com2}, \tag{10}$$

where $v_{io,DE}$, with $i = a, b, c, d, e, \ldots$, is the pole (or switched phase) voltage, and the subscripts '1' and '2' denote "inverter 1" and "inverter 2" respectively; the individual CM voltages v_{com1} and v_{com2} are obtained using (4), applied to the two SE inverters respectively.

In the following analysis, it is assumed that the two inverters connected in the DE configuration have the same number of levels n and phases m, as well as the same dc source voltages (i.e. $v_{dc1} = v_{dc2} = v_{dc}$).

If the switching function for a DE inverter drive is defined as $S_{i,DE}$, then, in analogy to (2) and (3), we derive the switching function for a DE VSI system

$$S_{iDE} = 0, 1, \cdots, 2(n-1) \tag{11}$$

and the overall voltage across the stator phase winding of the machine

$$v_{ioDE} = \frac{[S_{iDE} - (n-1)]v_{dc}}{n-1}. \tag{12}$$

Table V shows the available switching functions $S_{i,DE}$ and their corresponding switched phase voltages $v_{io,DE}$ for a DE inverter drive system with two identical VSIs. The entries of the table are obtained from (11) and (12). Note that the values for $v_{io,DE}$ are given in fractions of the inverter dc link voltage v_{dc}.

TABLE V: Switching functions and pole voltages of an n-phase DE VSI system

Inverter levels	$S_{i,DE}$ | $v_{io,SE}$ in fractions of v_{dc}.											
2	0 | -1	1 | 0	2 | 1									
3	0 | -1	1 | -½	2 | 0	3 | ½	4 | 1							
4	0 | -1	1 | -⅔	2 | -⅓	3 | 0	4 | ⅓	5 | ⅔	6 | 1					
5	0 | -1	1 | -¾	2 | -½	3 | -¼	4 | 0	5 | ¼	6 | ½	7 | ¾	8 | 1			
6	0 | -1	1 | -4/5	2 | -3/5	3 | -2/5	4 | -1/5	5 | 0	6 | 1/5	7 | 2/5	8 | 3/5	9 | 4/5	10 | 1	
7	0 | -1	1 | -5/6	2 | -⅔	3 | -½	4 | -⅓	5 | -1/6	6 | 0	7 | 1/6	8 | ⅓	9 | ½	10 | ⅔	11 | 5/6	12 | 1

B. Step Sizes and Number of CMV Levels

As with the SE system, the step size of the phase switched voltage $\Delta v_{io,DE}$ of any n-level m-phase DE VSI system is given by

$$\Delta v_{io,DE} = \frac{v_{dc}}{2(n-1)}. \tag{13}$$

The minimum step size of the CMV $\Delta_{min} v_{com,DE}$ is equal to the minimum step size of the CMV in the case of a SE VSI system,

$$\Delta_{min} v_{com,DE} = \frac{\Delta v_{io,DE}}{m} = \frac{v_{dc}}{m(n-1)}. \tag{14}$$

The number of theoretically possible different levels in the CMV, $n_o v_{com,DE}$, is derived from the minimum step size $\Delta_{min} v_{com,DE,}$ similar to the case of the SE system, but considering that two times the inverter dc link voltage v_{dc} is available,

$$n_o v_{com,DE} = \frac{2v_{dc}}{\Delta_{min} v_{com,SE}} + 1 = 2m(n-1) + 1. \tag{15}$$

For a relatively high number of inverter levels n, there are approximately twice as many theoretically possible different levels in the CMV in a DE VSI system than in a SE VSI system.

For a DE n-level VSI system, the number of pole voltage levels is found to be

$$n_o v_{ioDE} = 2n - 1. \tag{16}$$

From (16) it can be observed that the number of pole voltage levels $n_o v_{io,DE}$ is always odd. In contrast to the SE system in which the parity (odd or even) of the levels n and phases m affects the existence (or non-existence) of switching states that produce zero v_{io} and zero CMV, there is always (at least one) switching combination for the DE system that produces $v_{io} = 0$ and $v_{com} = 0$, regardless of the numbers of inverter levels n and phases m.

As with the SE VSI system, the step size of the CMV $\Delta_{min} v_{com,DE}$ decreases inversely proportionally and the number of voltage levels in the CMV $n_o v_{com,DE}$ increases linearly with the number of inverter levels n and the number of phases m, implying again a reduction in the magnitude of the rate of change of the CMV.

Exemplarily, Table VI shows the different possible voltage levels in the CMV for the two-, three- and five-level VSI configurations for three-phase and five-phase systems.

TABLE VI: DOUBLE-ENDED INVERTER SYSTEMS: CMV LEVELS IN 3 AND 5-PHASE SYSTEMS FOR 2, 3 AND 5-LEVEL SYSTEMS.

	2-Level		3-Level		5-Level	
SN	3-Phase	5-Phase	3-Phase	5-Phase	3-Phase	5-Phase
1	0	0	0	0	0	0
2	±1/3	±1/5	±1/6	±1/10	±1/12	±1/20
3	±2/3	±2/5	±2/6	±2/10	±2/12	±2/20
4	±3/3	±3/5	±3/6	±3/10	±3/12	±3/20
5	-	±4/5	±4/6	±4/10	±4/12	±4/20
6	-	±5/5	±5/6	±5/10	±5/12	±5/20
7	-	-	±6/6	±6/10	±6/12	±6/20
8	-	-	-	±7/10	±7/12	±7/20
9	-	-	-	±8/10	±8/12	±8/20
10	-	-	-	±9/10	±9/12	±9/20
11	-	-	-	±10/10	±10/12	±10/20
12	-	-	-	-	±11/12	±11/20
13	-	-	-	-	±12/12	±12/20
14	-	-	-	-	-	±13/20
15	-	-	-	-	-	±14/20
16	-	-	-	-	-	±15/20
17	-	-	-	-	-	±16/20
18	-	-	-	-	-	±17/20
19	-	-	-	-	-	±18/20
20	-	-	-	-	-	±19/20
21	-	-	-	-	-	±20/20

The maximum CMV for a DE n-level m-phase VSI system, is derived from (1), (14), and (15)

$$|v_{com,max,DE}| = (2m(n-1) + 1 - 1)\frac{v_{dc}}{m(n-1)}\frac{1}{2} = v_{dc}. \tag{17}$$

It is twice the value of the CMV of a DE VSI system.

C. Analysis: Comparison of DE and SE VSI Systems

The theoretical minimum step size of the CMV in the SE and in the DE VSI systems, $\Delta_{min} v_{com,SE}$ and $\Delta_{min} v_{com,DE}$, are the same, see (6) and (14). It decreases inversely proportionally with the number of inverter levels n and the number of phases m.

The numbers of possible levels in the CMV voltage $n_o v_{com,SE}$ and $n_o v_{com,DE}$ are compared from (7) and (16),

$$n_0 v_{comDE} = 2n_0 v_{comSE} - 1, \tag{18}$$

which, for a higher number of inverter levels n becomes

$$n_0 v_{comDE} \approx 2n_0 v_{comSE}. \tag{19}$$

For both systems, it increases proportionally with the number of inverter levels n and the number of phases m.

The maximum CMV for the DE, $|v_{com,max,DE}|$, is twice as large as the one of the SE system, $|v_{com,max,SE}|$, see (8) and (17),

$$|v_{com,max,DE}| = 2\,|v_{com,max,SE}|. \tag{20}$$

At this point, it is noted again that all these three investigated parameters are intrinsic to the topology of the VSI system. However, the number of CMV levels (out of all possible levels) that do occur in the drive system, as well as their frequencies of occurrence, will eventually depend on the applied modulation or control scheme.

V. LITERATURE REVIEW ON COMMON MODE VOLTAGE REDUCTION

A. CMV Reduction in Two-Level SE VSI Systems

In two-level VSIs, several methods have been suggested to reduce/eliminate the CMV (e.g. [19] [14] [20] [21] [22] [23] [24]). These techniques can mainly be grouped into three categories, namely (i) filters (e.g. [22] [23]),

(ii) modulation and control (e.g. [14] [24] [25] [26]), and (iii) filters, modulation and control (e.g. [19] [20] [21]). Examples for such work are described in the following.

By adding an external capacitance to the CM output of the VSI (modifying the equivalent electro-static circuit of an adjustable speed drive system) [22] the CMV at the motor terminals can be highly attenuated. A so called auxiliary zero state synthesizer [27] is introduced to substantially reduce the generated CMV and thus the CM current by several orders of magnitude: Modifications are made on the inverter topology as well as the modulation strategy to achieve the desired goals. The zero (null) states responsible for the maximum levels of the CMV to occur ($\pm \frac{1}{2} v_{dc}$) are avoided in the modulation strategy. As a result the CM current is also attenuated. In [23], a CM transformer and normal-mode filters are used together to reduce the EMI resulting from both the CM and normal-mode currents.

Using a modified SVPWM [14], a modulation strategy which reduced the CMV to a constant value of $-v_{dc}/6$ was proposed. This was achieved by allowing any fluctuation of the CMV by switching only even or only odd states. Using SVPWM method [24], a technique using three adjacent active space vectors to synthesize the output voltage is presented. It avoids using the zero space vectors and thus thereby reduces the peak-to-peak values of the CMV in one PWM cycle. Several techniques on reducing the CMV to the peak-to-peak value of $\frac{1}{3} v_{dc}$ are compared and found out that the dead time and sector transitions cause the actual peak-to-peak value at those instances to be equal to v_{dc} [25]. This is well addressed by proposing a SVPWM modulation technique which takes into consideration the dead time compensation and spikes in CMV at sector transitions and reflected wave compensation. A modulation technique is introduced in [26] to modify the one presented in [25] by extending the range of the modulation index by correctly compensating for the voltage-second distortion caused by the reflected wave compensation. These methods held the peak-to-peak value of the CMV to one third of the dc link voltage ($\frac{1}{3} v_{dc}$).

In [19], the CMV is eliminated by adding a fourth leg to the bridge of a three-phase inverter and modifying the modulation strategy to achieve a three-phase star-output neutral-to-ground voltage. In addition, the four-phase LC filter is also included for the purpose of creating the line-to-line voltages across the load. A modified SVPWM was used in this strategy. An active common-noise canceler (ACC) capable of reducing the ground current and conducted EMI is proposed [20]. This ACC superimposes a compensating voltage of the same magnitude and opposite polarity to that of the common-mode voltage and thus cancelling its effect. A common-mode transformer is necessary for this strategy. In [21], a reactor, *RC* and *RLC* filters (at the motor terminals and inverter output terminals) are compared. Also their positions in the circuit are a focus on the analysis, whereby the *RLC* at the inverter output is favored to the other two filters (i.e. reactor and *RC*).

At this point, it is worth mentioning that two two-level VSIs in a DE configuration constitute a multilevel system. Therefore, their discussion is part of the section on multilevel inverters.

B. CMV Reduction in Multilevel Inverter Systems

Multilevel inverter systems can be classified into two categories (i) single multilevel inverter drives (SMIDs) and (ii) double-ended inverter drives (DEIDs). SMIDs refer to drive systems containing only one multilevel VSI connected to the stator winding of an electrical machine. The number of levels in the output voltage is greater than or equal to three. DEIDs configurations consists of two VSIs connected at either side of the open stator winding of the electrical machine. Individual inverters can be of any level, but have to be of the same number of phases as the electrical machine. On contrast to the work on two-level VSIs, where many filters have been proposed, most work on reducing or eliminating the CMV of multi-level inverters has focused on the modulation and/or control scheme used.

B-1) SMIDs: Using SVPWM for a three-level diode-clamped PWM inverter, a passive EMI filter which is connected to the ungrounded motor neutral point and uses the stator windings as part of the filter has been proposed in [28]. This can be extended to any number levels.

In [29], the CMV is eliminated by using a reduced CM hysteresis current regulation technique. It employs the difference between the line current errors and the matching of the generated inverter switched states to the reduced states of an ((n+1)/2)-level inverter that ensure zero CMVs. In [13], three sinusoidal PWM (SPWM) methods, namely, phase disposition (PD), phase opposition disposition (POD) and alternate phase opposition disposition (APOD) are employed for multilevel inverter control. It is stated that, for a three-phase inverter, the minimum step size of the CMV is $\pm \frac{1}{3} v_{dc}$ with the SPWM technique. In PD-SPWM, the CMV of a five-level three-phase VSI is reduced to the step of $\pm 1/12\ v_{dc}$ at the crossing of each reference wave with the rising edge of the carrier signal. It further states that the APOD and POD modulation techniques are able to reduce the CMV levels to $1/12\ v_{dc}$ as compared to PD which reduces it to $\pm 1/6\ v_{dc}$.

Tests on a medium voltage multilevel VSI drive using SVPWM are presented in [3]. A three-phase three-level neutral-point-clamped (NPC) VSI induction motor drive is used to investigate the CMV. It was shown that at low frequency operation or low modulation index (inner hexagon), the peaks of the resulting CMV were equal to $\pm v_{dc}$, whereas the peaks were equal to $\pm \frac{2}{3} v_{dc}$, for HF operation (outer hexagon). Several solutions for motor

shaft voltage and bearing currents proposed are such as reducing/eliminating the $\pm v_{com}$ (e.g. using simple double-triangle modulator, solidly grounding the motor neutral etc.), eliminating/reducing coupling from motor stator winding to shaft, eliminating motor shaft voltage by grounding the shaft and eliminating/reducing the motor neutral voltage by redesigning the common-mode circuitry.

In [16], inverters with odd number of levels are considered. By only switching among certain states, zero CMV is generated. Both SPWM and SVPWM are used in the proposed modified schemes that entail zero CMV. For higher number of levels ($n \geq 7$), a modulation strategy for multilevel inverters is proposed in [30] using a selection of the voltage vectors that generate zero CMV at low switching frequency in which the total harmonic distortion, the number of commutations and the linearity are studied. The method works for the number of levels greater than or equal to seven since at lower number of levels the quality of the line currents is significantly affected.

In [12] a new plane called the "zero CM plane" is introduced in which medium space vectors are used to eliminate the CMV in the three-level diode clamped three-phase voltage source inverter. An $(n + 1)/2$ level imaginary inverter is discussed in [17]. In this technique, the line voltages of an $(n + 1)/2$ level inverter are used as the phase voltages of an n-level inverter and it works only for odd number of levels. The line voltages of an imaginary inverter are used as the phase voltages of the real inverter and it can be implemented using both SVM and SPWM techniques. A selective carrier based PD modulation technique is used and the CMV is eliminated. Integration of dual-random (random switching frequency and random pulse placement) and reduced CM PWM techniques for controlling a three-phase three-level NPC inverter drive are discussed in [31]. In [32] a cascaded multilevel inverter and neutral point clamped inverter for medium voltage PWM adjustable speed drive systems are analyzed. Modulation strategies to reduce the CMV are also suggested. The configuration for the cascaded inverter in this analysis makes use of the transformers whose secondary windings have uneven voltage stresses and thus requiring attention during the design stage.

B-2) DEIDs: In [33] a modulation scheme to eliminate the CMV generated by the two individual inverters in the double-ended inverter configuration is proposed. In [34], a dual five-level inverter open-end-winding induction motor drive structure for the three-phase system is used for the simultaneous elimination of the CMV and *dc*-link capacitor voltage imbalance using SPWM and the states that generate zero CMV on the space voltage vectors. The same approach is applied in [35] for a three-level open-end winding induction motor drive and in [15]. More work on CMV reduction/elimination in DEID configurations is discussed in [36] [37] [38] [18]. In [36], an 8-level inverter is realized by having a four level inverter (from three two-level inverters in cascade) on one side of the stator winding and a two-level inverter on the other side. A SPWM strategy is employed which reduces the switching events as well as the CMV which can be completely eliminated if the voltage vectors selected for the reference vector avoid the states producing it. Using modified SVPWM method by selecting a combination of voltage vectors with zero CMV [37], the CMV is eliminated in the double-ended configuration of the dual two-level inverter fed induction motor drive.

C. CMV Reduction in Multiphase Inverters Systems

Although multiphase machines have received greater attention for the last century, at this point the authors are not aware of any work which has addressed the reduction/elimination of CMV in multiphase drives. Most of the available literature is on the modulation and/or control techniques. The analysis presented on the *n*-level three-phase drive systems can be extended to *n*-level *m*-phase drive systems. In light of this, the presented general analysis will provide an important building block and a technique for further research on the CMV in multiphase inverter systems.

VI. SUMMARY

While the occurrence of CMV in VSIs is frequently referred to in the literature, the way it is analyzed is still mostly a matter of the different authors' foci. In this paper, we propose a metric for a systematic analysis of this CMV and apply it to thoroughly study the CMV properties intrinsic to the topologies of *n*-level, *m*-phase and SE as well as DE diode-clamped VSI drive systems. Thereby, the CMV in VSIs is quantified by the number of possible levels and the step sizes between different levels, as well as the respective frequencies of occurrence. The first two are given by the number of levels and the number of phases of the inverter and intrinsic to its topology. Depending on the modulation (control) schemes, all possibly available or a few of these levels are present in the CMV.

For a given DE system, there are approximately twice as many possible different voltage levels in the CMV and the maximum amplitude of the CMV is approximately twice as large as for the corresponding SE configuration. For both systems, the step size of the CMV is inversely proportional and the number of possible levels in the CMV proportional to the number of inverter levels and phases.

We also showed that not only the inverters with an odd number of levels can produce a zero CMV level in an SE configuration but also those with an even number of inverter levels and an even number of phases. For the DE configuration, all combinations of inverter levels and phases are able to produce the zero CMV voltage level.

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APPENDIX

A. Illustration: Pole Voltages in Three-Level Three-Phase and Five-Phase SE Inverter Drive Systems

The CMVs for three- and five-phase SE VSI systems are given respectively by

$$v_{com} = \frac{1}{3}(v_{ao} + v_{bo} + v_{co}), \tag{26}$$

$$v_{com} = \frac{1}{5}(v_{ao} + v_{bo} + v_{co} + v_{do} + v_{eo}). \tag{27}$$

For three-level inverters, the governing equation for the switched voltage is [12], [13]:

$$v_{io} = \frac{(S_{i,SE}-1)v_{dc}}{2}, \tag{28}$$

where $S_{i,SE}$ can take the values of 2, 1 and 0. The three different possible levels of the switched phase voltage are: v_{io} = ½ v_{dc}/2 ($S_{i,SE}$ = 2), v_{io} = 0 ($S_{i,SE}$ = 3), and v_{io} = - ½ v_{dc} ($S_{i,SE}$ = 0). Considering the one leg of the inverter representing phase 'a', as depicted in Fig. 1, when the switches S_{ap1} and S_{ap2} are on, then S_a = 2 and v_{ao} = ½ v_{dc}; when the switches S_{ap2} and S_{an1} are on, then S_a = 1 and v_{ao} = 0; when the switches S_{an1} and S_{an2} are on, then S_a = 0 and v_{ao} = - ½ v_{dc}.

For the five-level inverters, the governing equation for the switched voltage is

$$v_{io} = \frac{(S_{iSE}-2)v_{dc}}{4}, \tag{29}$$

where $S_{i,SE}$ can take the values of 4, 3, 2, 1 and 0. The five different possible levels of the switched phase voltage are: v_{io} = ½ v_{dc} ($S_{i,SE}$ = 4,); v_{io} = ¼ v_{dc} ($S_{i,SE}$ = 3), v_{io} = 0 ($S_{i,SE}$ = 2), v_{io} = - ¼ v_{dc} ($S_{i,SE}$ = 1) and when v_{io} = - ½ v_{dc} ($S_{i,SE}$ = 0). When the switches S_{ap1} and S_{ap2} are on, then S_a = 2 and v_{ao} = ½ v_{dc}; when the switches S_{ap2} and S_{an1} are on, then S_a = 1 and v_{ao} = 0; when the switches S_{an1} and S_{an2} are on, then S_a = 0 and v_{ao} = ½ v_{dc}.

The combination of the switches when the inverter is controlled will give different levels of the CMV depending on the individual inverter phase output voltages v_{io}, the maximum and minimum levels of the CMV (i.e. ½ v_{dc} and - ½ v_{dc}) occurring when all the output voltages are equal to ½ v_{dc} and - ½ v_{dc}, respectively.

2. IEEE ECCE 2012 CONFERENCE (WITH SUBSEQUENT SUBMISSION TO IEEE TRANSACTIONS IAS): "ON THE INFLUENCE OF DIFFERENT PWM TECHNIQUES ON THE OCCURRENCE OF THE DIFFERENT COMMON MODE VOLTAGE LEVELS IN MULTILEVEL MULTIPHASE SINGLE AND DOUBLE-ENDED DIODE-CLAMPED VSI SYSTEMS"

[Paper to be submitted to ECCE 2012; the main body of the digest will be pulled from the draft of the full paper. The introduction and the review for the digest will be written later. Those for the full paper will only be written once the result of the review outcome of the special issue paper is known.]

On the Influence of Different PWM Techniques on the Occurrence of the Different Common Mode Voltage Levels in Multilevel Multiphase Single and Double-Ended Diode-Clamped VSI Systems

I. INTRODUCTION [1 PAGE]

A. Emerging of Multiphase Multilevel VSI Systems

[Similar to Special Issue Paper; to add later]

B. Motivation: Parasitic Effects of the Common Mode Voltage

[Similar to Special Issue Paper; to add later]

Say, that the "CMV reduction" has found wide interest, but the "degree of reduction" should be quantified. Make distinction between the characteristics intrinsic to the system and the role of the control/modulation scheme.

II. REVIEW: COMMON MODE VOLTAGE QUANTIFICATION [1/3 PAGE]

[Review from Special Issue Paper; if accepted. Otherwise, Part from Special Issue Paper.]

The total number of theoretically possible CMV levels ($n_o v_{com}$) in an *n*-level *m*-phase SE and DE inverter is given by (1) and (2) respectively [*Ref: IASPELS Special Issue Paper*]

$$n_o v_{com,SE} = m\ n-1\ +1, \quad (1)$$

$$n_o v_{com,DE} = 2m\ n-1\ +1. \quad (2)$$

For a SE system, the maximum and minimum levels are $\frac{1}{2}v_{dc}$ and $-\frac{1}{2}v_{dc}$, respectively; whereas for a DE system, the respective maximum and minimum levels are v_{dc} and $-v_{dc}$.

The minimum step size $\Delta_{min} v_{com}$ for an *n*-level *m*-phase SE as well as DE inverter system is given by [*Ref: IASPELS Special Issue Paper*]

$$\Delta_{min} v_{com,SE} = \Delta_{min} v_{com,DE} = \frac{v_{dc}}{m\ n-1}. \quad (3)$$

Note that possible occurring step sizes Δv_{com} can be $h\Delta_{min} v_{com}$, where $h = 0, 1, 2 \ldots n_o v_{com} - 1$.

III. OVERVIEW OF INVESTIGATED VSI SYSTEMS AND CONTROL SCHEMES [1/2 PAGE]

A. VSI Systems

The inverter topology considered in this analysis is the diode-clamped configuration, for both the SE and DE drive systems. A schematic representation of an *n*-level *m*-phase diode clamped voltage source inverter is shown in Fig. 1. In SE inverter drives, one inverter is used to supply the machine, as shown in Fig. 2. In DE drives, two inverters are connected at either end of the stator winding of the electrical machine. The configuration for such a system is shown in Fig. 3. [Draw "nice" figures only for final paper.]

Figure 1: Schematic diagram of *n*-level *m*-phase voltage source inverter [To be inserted later.]

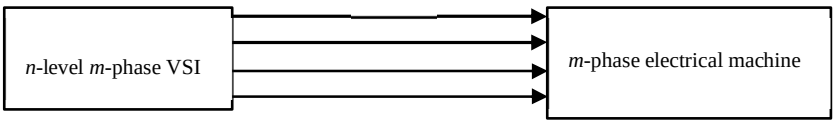

Figure 2: Configuration of the single-inverter drive system.

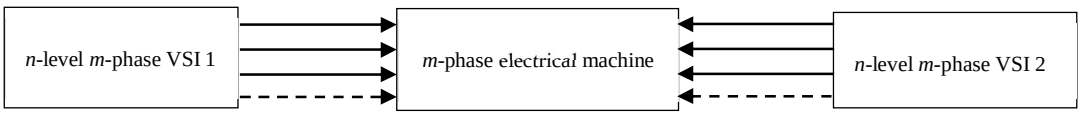

Figure 3: Configuration of the double-inverter drive system.

Example cases are studied for two-level, three-level and five-level three- and five-phase inverter systems. [January 2012: Review how much of the results can be generalized?]

B. Control Schemes

Four different control methods for multilevel multiphase systems have been chosen for the analysis:

1-3. Three carrier disposition methods, each requiring one reference modulation signal for each inverter leg and (n-1) high frequency triangular signals, and

4. A "new carrier based PWM" method (NCBPWM) that only requires one carrier signal and n modulation signals for each inverter leg, as presented in [*reference(s)*].

In the carrier disposition methods, the high frequency carrier triangular waveforms are shifted vertically. The three alternative carrier disposition sinusoidal PWM (SPWM) strategies can be classified as follows [*reference(s)*]:

1. Phase disposition sinusoidal PWM (PD-SPWM): all carrier signals are in phase.
2. Phase opposition disposition sinusoidal PWM (POD-SPWM): all carrier signals above the zero reference are in phase and in opposition with those below the zero reference.
3. Alternate phase opposition disposition sinusoidal PWM (APOD-SPWM): all carrier signals are alternatively in opposition disposition.

Note that for a three-level inverter, the APOD and POD are the same. The three different modulation methods are illustrated in Figs. 11 to 12 in the Appendix.

4. The fourth method, NCBPWM ensures the balancing of the capacitor voltage as well as zero neutral point voltage for odd number of inverter levels. With one high frequency carrier signal compared to n modulation signals (derived from the reference signal), the required switching functions are generated to control the multilevel multiphase inverter. The generation of the switching functions is as depicted in Fig. 4 for a three-level m-phase voltage source inverter [*reference(s)*].

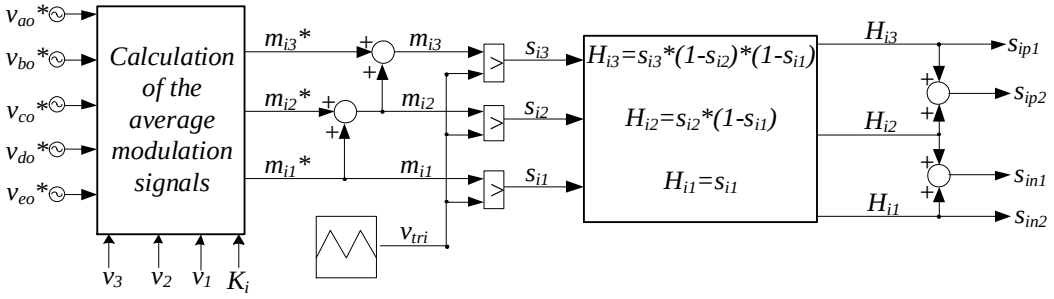

Figure 4: Principle of the NCBPWM modulation method for the three-level diode-clamped m- phase VSI.

5. For the sake of completeness, and for comparison, the two-level multiphase inverter using the conventional sinusoidal PWM (2LSPWM) control is also included in the analysis.

IV. Method of Analysis [1/2 page]

A. Occurring CMV Levels and Their Frequencies of Occurrence

To determine which CMV levels (out of the theoretically possible levels) do exist when different control techniques are used, a comparator was implemented to compare the actual CMV waveform against the different theoretically possible CMV levels. The frequency of occurrence of a particular voltage level $v_{com,i}$ is denoted $f\_v_{com,i}$, the total number of occurring voltage levels $n_o v_{com}\_ctrl$, where $n_o v_{com}\_ctrl \leq n_o v_{com}$. Fig. 5 [Draw "nice" figures only for final paper.] shows how the counter for the determination of the occurrence/existence of a particular CMV level in a given control method was implemented.

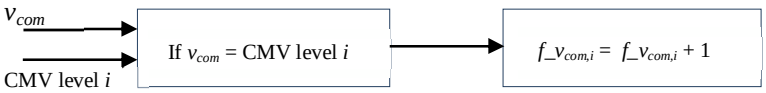

Figure 5: Counter to determine the frequency of occurrence of the particular i^{th} voltage level in the CMV; $n_o v_{com}$ of such counters were implemented, one for each possible CMV level.

B. Number of CMV Level Transitions

A second counter was implemented to record the different step sizes of the CMV Δv_{com} and their respective number of occurrences $f\_\Delta v_{com}$. To determine the frequencies of transitions from one CMV level to another by the step size Δv_{com}, the CMV waveform was compared to integer multiples of the minimum step size $\Delta_{min} v_{com}$. Fig. 6 [Draw "nice" figures only for final paper.] shows the determination of the number of transitions with step size Δv_{com} from one level to another.

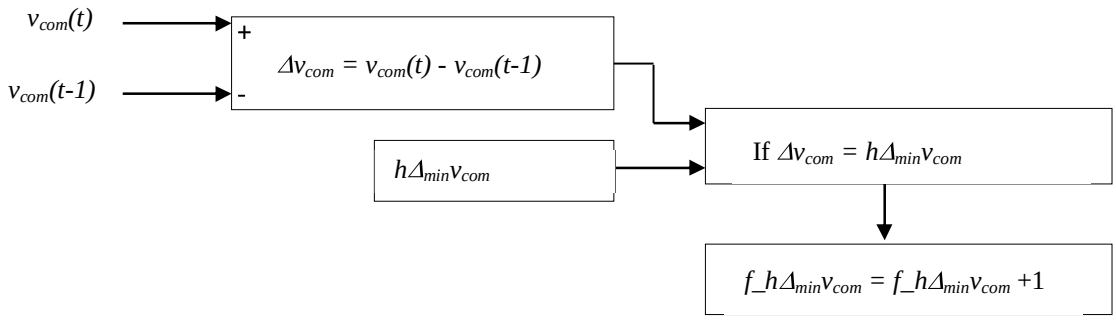

Figure 6: Counter for determination of the number of transitions from one CMV level to another; (note that only levels Δv_{com} up to the maximum difference of occurring CMV levels is included).

C. Determination of Average Values per Switching Period

Because the switching sequences of the pole voltages within one switching period depends on the operating point of the machine, average values of the numbers of occurrence of the different CMV levels and transitions have to be determined. If $n_o v_{com}\_ctrl_{Tm}$ is the number of CMV levels that occur within one fundamental period T_m, and f_m and f_s are the fundamental and switching frequencies respectively, the average number of CMV levels per switching period is $n_o v_{com}\_ctrl_{Ts}$

$$n_o v_{com}\_ctrl_{T_s} = n_o v_{com}\_ctrl_{T_m} \frac{f_m}{f_s}. \quad (4)$$

The same approach is chosen to obtain the average frequencies of occurrence of a given CMV level $v_{com,i}$ per switching sequence, i.e.

$$f\_n_o v_{com,i,Ts} = f\_n_o v_{com,i,Tm} \frac{f_m}{f_s}. \quad (4)$$

In this context, we also define the simulation time $t_{sim,pu}$ in per-units as the ratio of the simulation time t_{sim} and the switching period T_s,

$$t_{sim,pu} = t_{sim}/T_s \quad (5)$$

D Experimental Set Up

The experimental setup used for the experimental analysis is shown in Fig. Exp1. It consists of a three-level five-phase VSI drive. It is controlled using the four methods analyzed in this paper. In Fig. Exp1 (a), a SE set up is shown, whereas the respective set up for the DE configuration is shown in Fig. Exp1 (b). The setup is composed of two identical 10 kVA three-level diode-clamped five-phase VSIs and a 5-hp, 60 Hz, 4-pole five-phase induction machine. The CMV is measured with the help of resistive artificial star point(s) connected at the machine terminals.

Figure Exp1: Experimental Setup (a) SE and (b) DE configurations

V. Results 1: Single-Ended Inverter System [1 page]

A. Review: Different Possible CMV Levels

[Review from Special Issue Paper; if accepted. Otherwise… decide then.]

B. Occurring CMV Levels, Their Frequencies of Occurrence, and Transitions Between Individual Levels

The total number of different possible CMV levels in an *n*-level *m*-phase SE inverter drive system is given by (1). For the NCBPWM, all of these possible CMV levels occur. For the PD, POD, and APOD the number of CMV levels that do exist is reduced. Table I shows the occurring levels ($n_o v_{com}\_ctrl$) and their respective frequencies of occurrence ($f\_n_o v_{com,i}$) for one switching cycle for both a three-level and a five-level SE inverter for the different control methods. For the sake of completeness, Table II shows these parameters for a two-level three- and five-phase VSI when controlled using SPWM. In these tables, the voltage levels and step sizes are presented as multiples of the dc link voltage v_{dc}.

TABLE I: Frequencies of occurrence of the different CMV levels within one switching cycle in a three- and a five-level SE VSI system

		$n_o v_{com}\_ctrl_{T_s}$							
CMV levels		PD		POD		APOD		NCBPWM	
3-Phase	5-Phase	3-Phase	5-Phase	3-Phase	5-Phase	3-Phase	5-Phase	3-Phase	5-Phase
3-Level									
0	0	2	2	3	5	3	5	2	2
±1/6	±1/10	1.5+1.5=3	2+2=4	1.5+1.5=3	2.5+2.5=5	1.5+1.5=3	2.5+2.5=5	2+2=4	2+2=4

±2/6	±2/10	0.5+0.5=1	1.5+1.5=3	-	-	-	-	2+2=4	2+2=4
±3/6	±3/10	-	0.5+0.5=1	-	-	-	-	1 + 1 = 2	2+2=4
-	±4/10		-	-	-	-	-	-	2+2=4
-	±5/10		-	-	-	-	-	-	1+1=2
$f\_n_o v_{com}\_ctrl$		∑ 2·3 = 6	∑ 2·5 = 10	∑ 2·3 = 6	∑ 2·5 = 10	∑ 2·3 = 6	∑ 2·5 = 10	∑ 2·2·3 = 12	∑ 2·2·5 = 20
				5-Level					
0	0	2	2	3	5	3	2	2	2
±1/12	±1/20	1.5+1.5=3	2+2=4	1.5+1.5=3	2.5+2.5=5	1.5+1.5=3	2.5+2.5=5	2 + 2 = 4	2 + 2 = 4
±2/12	±2/20	0.5+0.5=1	1.5+1.5=3	-	-	-	1.5+1.5=3	2 + 2 = 4	2 + 2 = 4
±3/12	±3/20	-	0.5+0.5=1	-	-	-	-	2 + 2 = 4	2 + 2 = 4
±4/12	±4/20	-	-	-	-	-	-	2 + 2 = 4	2 + 2 = 4
±5/12	±5/20	-	-	-	-	-	-	2 + 2 = 4	2 + 2 = 4
±6/12	±6/20	-	-	-	-	-	-	1 + 1 = 2	2 + 2 = 4
-	±7/20	-	-	-	-	-	-	-	2 + 2 = 4
-	±8/20	-	-	-	-	-	-	-	2 + 2 = 4
-	±9/20	-	-	-	-	-	-	-	2 + 2 = 4
-	±10/20	-	-	-	-	-	-	-	1 + 1 = 2
$f\_n_o v_{com}\_ctrl$		∑ 2·3 = 6	∑ 2·5 = 10	∑ 2·3 = 6	∑ 2·5 = 10	∑ 2·3 = 6	∑ 2·5 = 10	∑ 2·4·3 = 24	∑ 2·4·5 = 40

TABLE II: FREQUENCIES OF OCCURRENCE OF THE DIFFERENT CMV LEVELS WITHIN ONE SWITCHING CYCLE IN A TWO-LEVEL SE VSI SYSTEM

		$n_o v_{com}\_ctrl_{T_s}$	
CMV levels		SPWM	
3-Phase	5-Phase	3-Phase	5-Phase
±1/6	±1/10	1 + 1 = 2	1 + 1 = 2
±3/6	±3/10	2 + 2 = 4	2 + 2 = 4
-	±5/10	-	2 + 2 = 4
$f\_n_o v_{com}\_ctrl$		∑ 2·3 = 6	∑ 2·5 = 10

The following observations are made regarding the existence of the different theoretically possible CMV levels and their respective frequencies of occurrence, all considering the four investigated control patterns.

1. *New carrier based PWM (NCBPWM):*
   - *(a) Total number of occurring CMV levels* ($n_o v_{com}\_ctrl$)*:* With this control method, all (n-1)m+1 maximum possible CMV levels do occur, i.e. $n_o v_{com}\_ctrl = (n\text{-}1)m+1$.
   - *(b) Frequency of occurrence of all occurring CMV levels* ($f\_n_o v_{com}$): The overall frequency of occurrence of all the different CMV levels in one switching cycle equals the switching frequency in the CMV and is derived as follows: With one switching event per device and cycle, 2(n-1) devices per leg (phase), there are (at maximum, assuming a change in the CMV with every switching event) 2(n-1)m instances of CMV levels (including repetitions) generated during one switching cycle T_s of an m-phase n-level inverter.
   - *(c) Frequency of occurrence of a particular level* ($f\_v_{com,i}$): Within one switching cycle, T_s, the maximum and minimum levels of the CMV (i.e. $½v_{dc}$ and $-½v_{dc}$) occur once and all other levels occur two times. For a given per-unit simulation time $t_{sim,pu}$, the occurrences are $t_{sim,pu}$ and $2t_{sim,pu}$ times respectively. (For example, for a three-level five-phase inverter, the levels 0, $\pm1/10v_{dc}$, $\pm2/10v_{dc}$, , $\pm3/10v_{dc}$ and $\pm4/10v_{dc}$ occur $2t_{sim,pu}$, and the level $\pm5/10v_{dc}$ $t_{sim,pu}$ times.)
   - *(d)* For verification, we discuss the following cross check: The frequencies of occurrence of the different CMV levels and the switching frequency in the CMV need to be the same: Except for the minimum and maximum levels of v_{com} (i.e. 2 levels) all other levels of $n_o v_{com}$ (i.e. $n_o v_{com}$ -2) occur two times: $2(n_o v_{com} - 2) + 2 = 2((n\text{-}1)m + 1 - 2) + 2 = 2((n\text{-}1)m - 1) + 2 = 2(n\text{-}1)m$.
2. *Phase Disposition (PD):*
   - *(a) Total number of occurring CMV levels* ($n_o v_{com}\_ctrl$)*:* The maximum possible number of levels ($n_o v_{com}\_ctrl$) that do occur is five and seven for three- and five-phase systems respectively, for both three- and five-level inverters; $n_o v_{com}\_ctrl < n_o v_{com}$.
   - *(b) Frequency of occurrence of all occurring CMV levels* ($f\_n_o v_{com}$): The total frequency of occurrence of all the different CMV levels is found to be $2mt_{sim,pu}$.
   - *(c) Frequency of occurrence of a particular level* ($f\_v_{com,i}$): It can be observed from Table I that a particular level (from $n_o v_{com}\_ctrl$) might not appear within a switching cycle.
3. *Phase Opposition Disposition (POD):*
   - *(a) Total number of occurring CMV levels* ($n_o v_{com}\_ctrl$)*:* The maximum possible number of levels ($n_o v_{com}\_ctrl$) that do occur is five and seven for three- and five-phase systems respectively, for both three- and five-level inverters; $n_o v_{com}\_ctrl < n_o v_{com}$.
   - *(b) Frequency of occurrence of all occurring CMV levels* ($f\_n_o v_{com}$): The total frequency of occurrence of all the different CMV levels is found to be $2mt_{sim,pu}$.

(c) *Frequency of occurrence of a particular level* ($f\_v_{com,i}$): The different occurring levels for the three-level and five-level three-phase VSI occur three times each, whereas for the five-phase systems, the frequency of occurrence of each of the different occurring levels is five.

4. *Alternate Phase Opposition Disposition (APOD):*
   (a) *Total number of occurring CMV levels* ($n_o v_{com}\_ctrl$)*:* The maximum possible number of different CMV levels ($n_o v_{com}\_ctrl$) that do occur is three for three- and five-phase three-level VSI system, and three and five for three- and five-phase five-level inverter systems respectively; $n_o v_{com}\_ctrl < n_o v_{com}$.
   (b) *Frequency of occurrence of all occurring CMV levels* ($f\_n_o v_{com}$): The total frequency of occurrence of all the different CMV levels is found to be $2mt_{sim,pu}$, similar to the PD and POD methods.
   (c) *Frequency of occurrence of a particular level* ($f\_v_{com,i}$): The different occurring levels for the three- and five-level, three-phase VSI occur three times each. For the five-phase systems, the frequency of occurrence is five for three-level CMV levels (0, ±1/10 v_{dc}), and two, five and three respectively for the five-level counterparts, (0, ±1/20, ±2/20 v_{dc}).
5. *SPWM for two-level inverters:*
   (a) *Total number of occurring CMV levels* ($n_o v_{com}\_ctrl$)*:* For the two-level VSIs, all possible CMV levels do occur, i.e. $n_o v_{com}\_ctrl = n_o v_{com}$.
   (b) *Frequency of occurrence of all occurring CMV levels* ($f\_n_o v_{com}$): The total frequency of occurrence of all possible levels is found to be $2mt_{sim,pu}$.
   (c) *Frequency of occurrence of a particular level* ($f\_v_{com,i}$): For both three- and five-phase systems, the CMV levels ±1/6 and ±1/10 v_{dc} respectively) occur $2t_{sim,pu}$ times, whereas the other levels occur $2t_{sim,pu}$ as much.

   As per Table II, the total number of level occurrences in one switching cycle is $2m$ and all CMV levels do occur as expected.

Regarding the step size of the CMV, all transitions between the different levels of the CMV $\Delta v_{com,SE}$ are by the minimum step size $\Delta_{min} v_{com,SE}$ only. This is true for all investigated control patterns.

C. Experimental Verification

The SE three-level five-phase VSI drive described above was run at no-load, using the three different control methods described in this section. The different occurring CMV levels were determined and their frequencies of occurrence counted. The experimental results confirm the theoretical and simulated results presented before. Exemplarily, Fig. Exp2 shows measured waveforms of the CMV for the (a) PD (b) APOD and (c) NCBPWM control methods.

[To measure back in the US]

Figure Exp2: Measured CMV in a three-level five-phase SE system using (a) PD (b) POD/APOD and (c) NCBPWM, for a 60-Hz cycle (i.e. 16.6 sec)

VI. Results 2: Double-Ended Inverter system [1 page]

A. Review: Different Possible CMV Levels

[Review from Special Issue Paper; if accepted. Otherwise… decide then.]

B. Occurring CMV Levels, Their Frequencies of Occurrence, and Transitions Between Individual Levels

The total number of different possible CMV levels in an *n*-level *m*-phase DE inverter drive system is given by (2), giving, for a three-phase system, a total of seven and thirteen CMV levels for a two- and three-level DE inverter respectively. The results are shown in Tables III and IV for three-, five- and two-level inverters, respectively. These tables show that such converter configurations result in a reduced total number of CMV voltage level occurrences for all the four control methods (PD, POD, APOD, NCBPWM) for multilevel inverters, as well as SPWM for two-level inverters.

TABLE III: Frequencies of occurrence of the different CMV levels within one switching cycle in a three and five-level DE VSI system

		$n_o v_{com}\_ctrl_{T_s}$							
CMV levels		PD		POD		APOD		NCBPWM	
3-Phase	5-Phase	3-Phase	5-Phase	3-Phase	5-Phase	3-Phase	5-Phase	3-Phase	5-Phase
3-Level									
0	0	6	5	3	5	3	5	12	15
±1/6	±1/10	3+3=6	5+5=10	-	-	-	-	6+6=12	10+10=20
±2/6	±2/10	-	2.5+2.5=5	1.5+1.5=3	2.5+2.5=5	1.5+1.5=3	2.5+2.5=5	-	2.5+2.5=5
$f\_n_o v_{com}\_ctrl$		$\sum 2{\cdot}2{\cdot}3 = 12$	$\sum 2{\cdot}2{\cdot}5 = 20$	$\sum 2{\cdot}3 = 6$	$\sum 2{\cdot}5 = 10$	$\sum 2{\cdot}3 = 6$	$\sum 2{\cdot}5 = 10$	$\sum 2{\cdot}\ 2{\cdot}2{\cdot}3 = 24$	$\sum 2{\cdot}2{\cdot}2{\cdot}5 = 40$

5-Level									
0	0	5.8	9.4	3	5	3	2.6	22.2	35
±1/12	±1/20	3+3=6	5+5=10	-	-	1.5+1.5=3	-	12 + 12 = 24	20 + 20 = 40
±2/12	±2/20	0.1+0.1=0.2	0.3+0.3=0.6	1.5+1.5=3	2.5+2.5=5	-	2.5+2.5=5	0.9 + 0.9 = 1.8	2.5 + 2.5 = 5
±4/12	±4/20	-	-	-	-	-	1.2+1.2=2.4	-	-
$f\_n_o v_{com}\_ctrl$		$\sum 2{\cdot}2{\cdot}3 = 12$	$\sum 2{\cdot}2{\cdot}5 = 20$	$\sum 2{\cdot}3 = 6$	$\sum 2{\cdot}5 = 10$	$\sum 2{\cdot}3 = 6$	$\sum 2{\cdot}5 = 10$	$\sum 2{\cdot}2{\cdot}4{\cdot}3 = 48$	$\sum 2{\cdot}2{\cdot}4{\cdot}5 = 80$

TABLE IV: FREQUENCIES OF OCCURRENCE OF THE DIFFERENT CMV LEVELS WITHIN ONE SWITCHING CYCLE IN A TWO-LEVEL DE VSI SYSTEM

CMV levels		$n_o v_{com}\_ctrl_{T_s}$	
2-Level		SPWM	
3-Phase	5-Phase	3-Phase	5-Phase
0	0	6	10
±1/3	±1/5	3 + 3 = 6	5 + 5 = 10
$f\_n_o v_{com}\_ctrl$		$\sum 2{\cdot}2{\cdot}3 = 12$	$\sum 2{\cdot}2{\cdot}5 = 20$

From the results shown in Tables III and IV, the following conclusions are drawn:

1. *New carrier based PWM (NCBPWM)*:
   - *(a) Total number of occurring CMV levels* ($n_o v_{com}\_ctrl$)*:* As opposed to the SE system, in the DE system, the maximum possible CMV levels that do occur are reduced. For a three-level three- and five-phase system, only three and five instead of 13 and 21 CMV levels occur respectively. Likewise, for the five-level three- and five-phase system, only five CMV levels occur instead of 25 and 41 respectively. i.e. $n_o v_{com}\_ctrl < 2(n\text{-}1)m+1$.
   - *(b) Frequency of occurrence of all occurring CMV levels* ($f\_n_o v_{com}$): With one switching event per device and cycle, $2(n\text{-}1)$ devices per inverter leg (phase) (which results in 4(n-1) devices in total), there are (at maximum, assuming a change in the CMV with every switching event) $4(n\text{-}1)m$ instances of CMV levels (including repetitions) generated during one switching cycle T_s of an m-phase n-level inverter. This is twice as much as for the SE configuration.
   - *(c) Frequency of occurrence of a particular level* ($f\_v_{com,i}$): With the total number of occurring levels ($n_o v_{com}\_ctrl$) being reduced, the frequencies of occurrence of those individual levels that do occur increases. For example, for a three-level three-phase DE system, the CMV level ±1/6 v_{dc} occurs $12t_{sim,pu}$ times compared to the same level in the SE system where it occurs $4t_{sim,pu}$ times.
2. *Phase Disposition (PD):*
   - *(a) Total number of occurring CMV levels* ($n_o v_{com}\_ctrl$)*:* The maximum possible number of levels ($n_o v_{com}\_ctrl$) that do occur is three and five for three- and five-phase systems respectively, in a three-level VSI, and five for the five-level VSI. As for the case of the SE systems, it is $n_o v_{com}\_ctrl < n_o v_{com}$.
   - *(b) Frequency of occurrence of all occurring CMV levels* ($f\_n_o v_{com}$): The frequency of occurrence of all possible levels is found to be $4mt_{sim,pu}$.
   - *(c) Frequency of occurrence of a particular level* ($f\_v_{com,i}$): There is an increase in the frequency of occurrence of the individual occurring levels. For example, a zero CMV level in a three-level three- and five-phase systems occurs $6t_{sim,pu}$ and $5t_{sim,pu}$ times respectively, as compared to the SE systems in which it occurs $2t_{sim,pu}$ times each.
3. *Phase Opposition Disposition (POD):*
   - *(a) Total number of occurring CMV levels* ($n_o v_{com}\_ctrl$)*:* The maximum possible number of levels ($n_o v_{com}\_ctrl$) that do occur is three for three- and five-phase systems, for both three- and five-level inverters; $n_o v_{com}\_ctrl < n_o v_{com}$.
   - *(b) Frequency of occurrence of all occurring CMV levels* ($f\_n_o v_{com}$): The frequency of occurrence of all possible levels is found to be $2mt_{sim,pu}$.
   - *(c) Frequency of occurrence of a particular level* ($f\_v_{com,i}$): The available levels for the three- and five-level three-phase VSIs occur three times each, whereas for the five-phase systems, the frequency of occurrence of each of the levels is five. It is worth-noting that the minimum step size of the CMV is twice as much as that of the SE configuration for both levels (three and five).
4. *Alternate Phase Opposition Disposition (APOD):*
   - *(a) Total number of occurring CMV levels* ($n_o v_{com}\_ctrl$)*:* The maximum possible number of levels ($n_o v_{com}\_ctrl$) that do occur is three for three-phase (for both three - and five-level), three and five for three- and five-level five-phase systems, respectively; $n_o v_{com}\_ctrl < n_o v_{com}$.
   - *(b) Frequency of occurrence of all occurring CMV levels* ($f\_n_o v_{com}$): The frequency of occurrence of all possible levels is found to be $2mt_{sim,pu}$.
   - *(c) Frequency of occurrence of a particular level* ($f\_v_{com,i}$): For the zero CMV level, the frequency of occurrence is the same as for the SE system for the three-level VSI (i.e. three and five for three- and

five-phase systems, respectively). While with the three-level three- and five-phase systems, the CMV levels ±2/6 and ±2/10 v_{dc} respectively do not occur in the SE systems, they do exist in the DE systems, replacing the CMV levels ±1/6 and ±1/10 v_{dc} respectively. This change of occurring CMV levels results in an increase in the step size of the CMV Δv_{com}, which now becomes twice the minimum step seize $\Delta_{min} v_{com}$ and hence twice the step size of the SE configurations. A similar argument can be made for five-level five-phase systems with CMV levels ±2/20 and ±4/10 v_{dc}.

5. *SPWM for two-level inverters:*
   (a) Total number of occurring CMV levels ($n_o v_{com}\_ctrl$)*:* For the two-level VSIs, the number of maximum occurring levels is reduced to three for both three- and five-phase systems, i.e. $n_o v_{com}\_ctrl = n_o v_{com}$.
   (b) Frequency of occurrence of all occurring CMV levels ($f\_n_o v_{com}$): The frequency of occurrence of all possible levels is found to be $4mt_{sim,pu}$.
   (c) Frequency of occurrence of a particular level ($f\_v_{com=i}$): For both three- and five-phase systems, the existing levels occur $6t_{sim,pu}$ and $10t_{sim,pu}$ times, respectively.

[NOTE: We might include the 7-level systems… time and space permitting.]

C. Experimental Verification

The DE three-level five-phase VSI drive described above was run at no-load, using the three different control methods described in this section. The different occurring CMV levels were determined and their frequencies of occurrence counted. The experimental results confirm the theoretical and simulated results presented before. Exemplarily, Fig. Exp3 shows measured waveforms of the CMV for the (a) PD (b) APOD and (c) NCBPWM control methods.

[To measure back in the US]

Figure Exp3: Measured CMV in a three-level five-phase DE system using (a) PD (b) POD/APOD and (c) NCBPWM, for a 60-Hz cycle (i.e. 16.6 sec)

VI. ANALYSIS [1 PAGE]

A. Comparison of SE and DE Inverter Drive Systems

The frequencies of occurrences of the individual occurring CMV levels increases for the DE inverter drive systems, some of the CMV levels do not appear for all the methods including the SPWM for two-level systems.

1. *Number of occurring levels*
   With the DE configuration, the number of levels of the CMV that exist (out of those theoretically possible) decreases when compared to the SE VSI system, especially for the NCBPWM method. This is a significant improvement especially for the NCBPWM whose CMV levels have reduced drastically.
2. *Frequencies of occurrence of all possible CMV levels*
   For the SE VSI it is
   - $2m(n\text{-}1)t_{sim,pu}$ for NCBPWM
   - $2mt_{sim,pu}$ for SPWM (two-level VSI), PD, POD and APOD

   For the DE VSI it is
   - $2mt_{sim,pu}$ for POD and APOD
   - $4mt_{sim,pu}$ for SPWM (two-level VSI) and PD
   - $4m(n\text{-}1)t_{sim,pu}$ for NCBPWM.
3. *Number of transitions*
   For the POD and APOD, the total frequency of occurrence of all the different levels of v_{com} is the same as for the SE VSI system. For the PD and NCBPWM methods, the total frequency of occurrence of all the different levels of v_{com} is twice as large as for the SE VSI system.
4. *Step size*
   Whereas, the step size Δv_{com} is the same for SE and DE systems for the PD, NCBPWM and SPWM methods (and it is always the minimum step size $\Delta_{min} v_{com}$), there is a change of the step size from the SE to the DE system for the POD and APOD methods. As per Table III, for the three-level three- and five-phase inverters, the step sizes of the DE systems with POD and APOD control are doubled when compared with the respective SE systems, i.e. 2/6 and 2/10 v_{dc} ($2\Delta_{min} v_{com}$) respectively.

B. Interpretation in the context of IIBCs

[Interpretation in the context of IIBCs → Tradeoff, machine size → AM to add later.]

VII. CONCLUSIONS [1/4 PAGE]

[To add later]

REFERENCES

[To add later]

[Not sure if we will leave the Appendix in, or if this will blow the size of the paper.]

APPENDIX

A. SE Inverter Systems:

For the SE inverter drive systems, the results of Table V through Table VII show the CMV levels available as well as their number of occurrences in one cycle of the fundamental frequency. It is worth mentioning that for the SE inverter drives, all the CMV levels do exist when the NCBPWM method is used.

TABLE V: SUMMARY OF THE TOTAL NUMBER OF LEVELS AND COMPARISON OF THE CONTROL METHODS IN ONE CYCLE OF THE FUNDAMENTAL FREQUENCY FOR THE SE 3-LEVEL 3- AND 5-PHASE INVERTER SYSTEMS:

Control Method	Available CMV Levels							$n_o v_{com\_ctrl_{Tm,SE}}$ (actual)	General Expression	$n_o v_{com\_ctrl_{Tm,SE}}$ (expected)
3-Phase										
	-3/6	-2/6	-1/6	0	1/6	2/6	3/6			
PD	-	81	248	333	247	81	-	990	$6t_{simpu}$	1000
APOD/POD	-	-	247	495	248	-	-	990	$6t_{simpu}$	1000
5-Phase										
	-3/10	-2/10	1/10	0	1/10	2/10	3/10			
PD	83	248	332	333	331	246	81	1654	$10t_{simpu}$	1667
APOD/POD	-	-	413	827	414	-	-	1654	$10t_{simpu}$	1667

TABLE VI: SUMMARY OF THE TOTAL NUMBER OF LEVELS AND COMPARISON OF THE CONTROL METHODS IN ONE CYCLE OF THE FUNDAMENTAL FREQUENCY FOR THE SE 2-LEVEL 3- AND 5-PHASE INVERTER SYSTEMS:

Available CMV Levels						$n_o v_{com\_ctrl_{Tm,SE}}$ (actual)	General Expression	$n_o v_{com\_ctrl_{Tm,SE}}$ (expected)
3-Phase								
-5/6	-3/6	-1/6	1/6	3/6	5/6			
-	167	333	333	167	-	1000	$6t_{simpu}$	1000
5-Phase								
-5/10	-3/10	-1/10	1/10	3/10	5/10			
167	334	334	333	332	166	1666	$10t_{simpu}$	16667

TABLE VII: SUMMARY OF THE TOTAL NUMBER OF LEVELS AND COMPARISON OF THE CONTROL METHODS IN ONE CYCLE OF THE FUNDAMENTAL FREQUENCY FOR THE SE 5-LEVEL 3- AND 5-PHASE INVERTER SYSTEMS:

Control Method	Available CMV Levels							$n_o v_{com\_ctrl_{Tm,SE}}$ (actual)	General Expression	$n_o v_{com\_ctrl_{Tm,SE}}$ (expected)
3-Phase										
	-3/12	-2/12	-1/12	0	1/12	2/12	3/12			
PD	-	82	249	334	248	82	-	995	$6t_{simpu}$	1000
POD	-	-	250	500	250	-	-	1000	$6t_{simpu}$	1667
APOD	-	-	248	498	250	-	-	996	$6t_{simpu}$	1000
5-Phase										
	-3/20	-2/20	-1/20	0	1/20	2/20	3/20			
PD	80	246	333	334	333	246	80	1652	$10t_{simpu}$	1667

POD	-	-	416	834	418	-	-	1668	$10t_{simpu}$	1667
APOD	-	203	414	423	412	202	-	1654	$10t_{simpu}$	1667

B. DE Inverter Systems:

For the DE inverter drive systems, the results of Table VIII through Table X show the CMV levels available as well as their number of occurrences in one cycle of the fundamental frequency.

TABLE VIII: SUMMARY OF THE TOTAL NUMBER OF LEVELS AND COMPARISON OF THE CONTROL METHODS IN ONE CYCLE OF THE FUNDAMENTAL FREQUENCY FOR THE DE 3-LEVEL 3- AND 5-PHASE INVERTER SYSTEMS:

Control Method	Available CMV Levels					$n_o v_{com\_ctrl_{Tm,DE}}$ (actual)	General Expression	$n_o v_{com\_ctrl_{Tm,DE}}$ (expected)
3-Phase								
	-2/6	-1/6	0	1/6	2/6			
PD		496	1000	496		1992	$12t_{simpu}$	
APOD/POD	247	-	500	-	248	995	$6t_{simpu}$	
NCBPWM	-	997	1988	992	-	3977	$24t_{simpu}$	
5-Phase								
	-2/10	-1/10	0	1/10	2/10			
PD	397	824	857	827	397	3302	$20t_{simpu}$	3333
APOD/POD	413	-	827	-	414	1654	$10t_{simpu}$	1667
NCBPWM	404	1656	2506	1656	402	6624	$40t_{simpu}$	6667

TABLE IX: SUMMARY OF THE TOTAL NUMBER OF LEVELS AND COMPARISON OF THE CONTROL METHODS IN ONE CYCLE OF THE FUNDAMENTAL FREQUENCY FOR THE DE 2-LEVEL 3- AND 5-PHASE INVERTER SYSTEMS:

Available CMV Levels			$n_o v_{com\_ctrl_{Tm,DE}}$ (actual)	General Expression	$n_o v_{com\_ctrl_{Tm,DE}}$ (expected)
3-Phase					
-2/6	0	2/6			
497	999	502	1998	$12t_{simpu}$	2000
5-Phase					
-2/10	0	2/10			
833	1663	830	3326	$20t_{simpu}$	3333

TABLE X: SUMMARY OF THE TOTAL NUMBER OF LEVELS AND COMPARISON OF THE CONTROL METHODS IN ONE CYCLE OF THE FUNDAMENTAL FREQUENCY FOR THE DE 5-LEVEL 3- AND 5-PHASE INVERTER SYSTEMS:

Control Method	Available CMV Levels							$n_o v_{com\_ctrl_{Tm,DE}}$ (actual)	General Expression	$n_o v_{com\_ctrl_{Tm,DE}}$ (expected)
3-Phase										
	-3/12	-2/12	-1/12	0	1/12	2/12	3/12			
PD	-	-	496	1000	496	-	-	1992	$12t_{simpu}$	2000
POD		249	-	500	-	250	-	999	$6t_{simpu}$	1000
APOD		247	-	500	-	248	-	995	$6t_{simpu}$	1000
NCBPWM		-	997	1988	992	-	-	3977	$24t_{simpu}$	4000
5-Phase										
	-4/20	-2/20	-1/20	0	1/20	2/20	4/20			
PD	-	51	829	1558	830	53	-	3321	$20t_{simpu}$	3333
POD	-	416	-	834	-	418	-	1668	$10t_{simpu}$	1667
APOD	200	415	-	435	-	419	204	1673	$10t_{simpu}$	1667
NCBPWM	-	407	3332	5849	3332	407	-	13327	$80t_{simpu}$	13333

Fig. 7 shows the PD-SPWM method for five-level inverter, four carrier triangular signals and one reference modulation signal. Fig. 8(a) and (b) shows the switching function S_i and the switched phase voltage respectively. Similar results are shown for the POD-SPWM method in Figs. 9 and 10. For the APOD-SPWM method, the corresponding results are shown in Figs. 11 and 12.

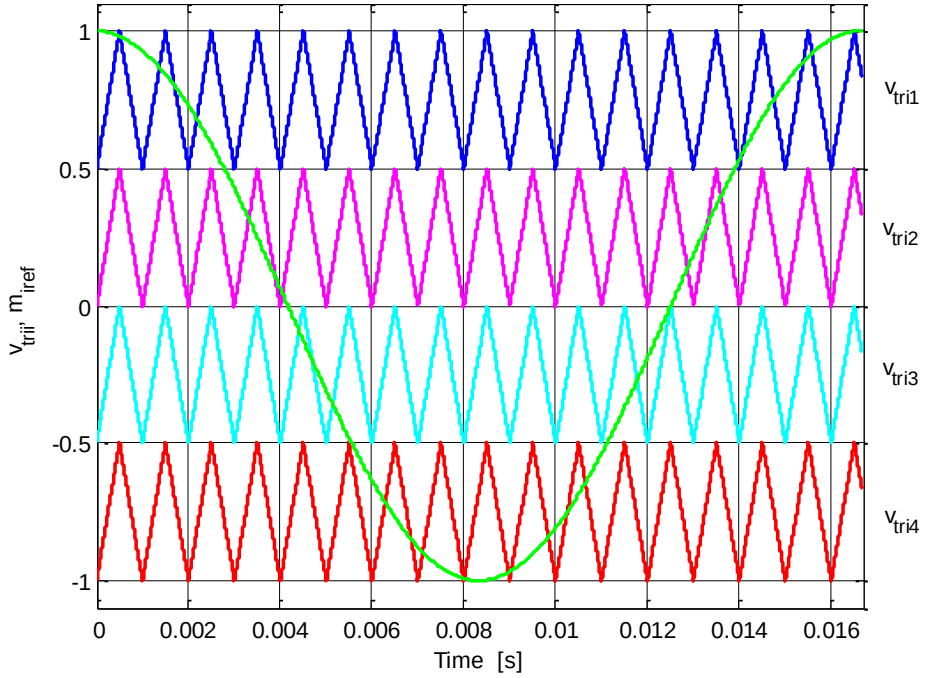

Figure 7 PD method for five-level inverter: (n-1) carrier signals and one reference modulation signal.

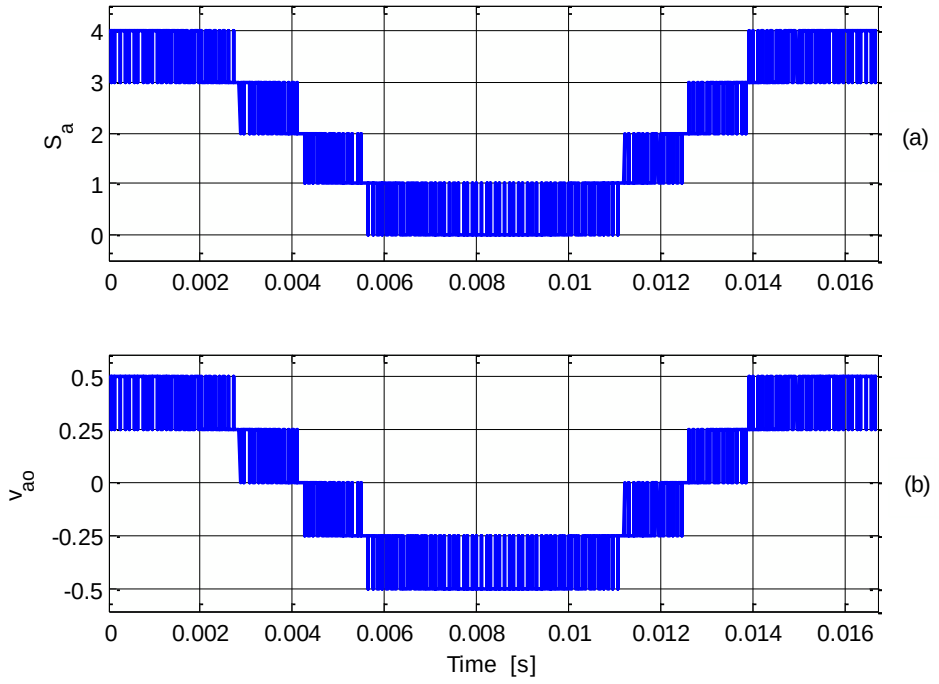

Figure 8 PD method for five-level inverter (a) switching function (S_i) (b) phase switched voltage (v_{io}).

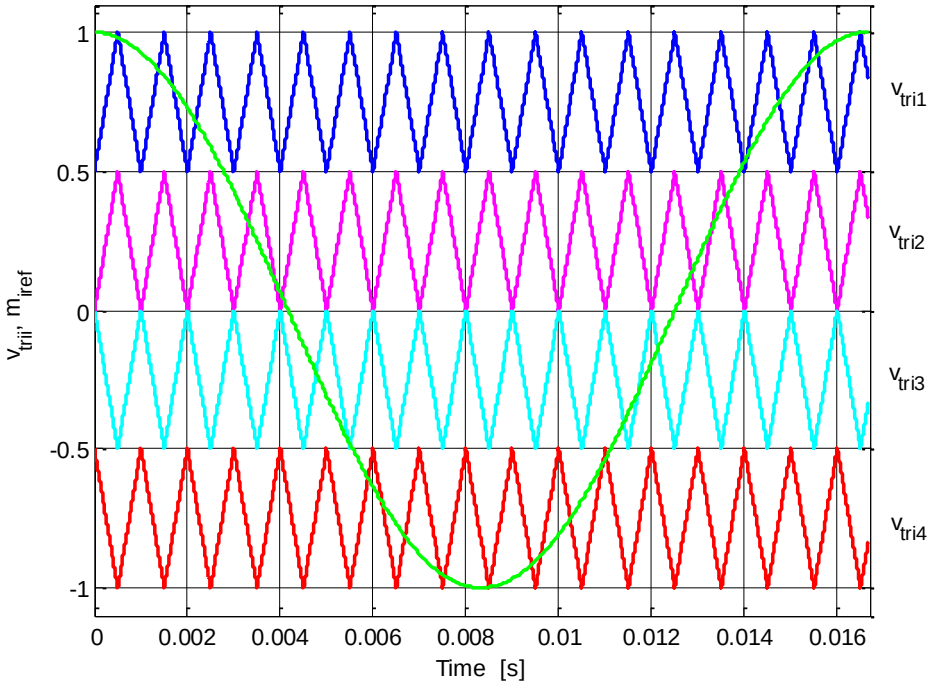

Figure 9 POD method for five-level inverter: (n-1) carrier signals and one reference modulation signal.

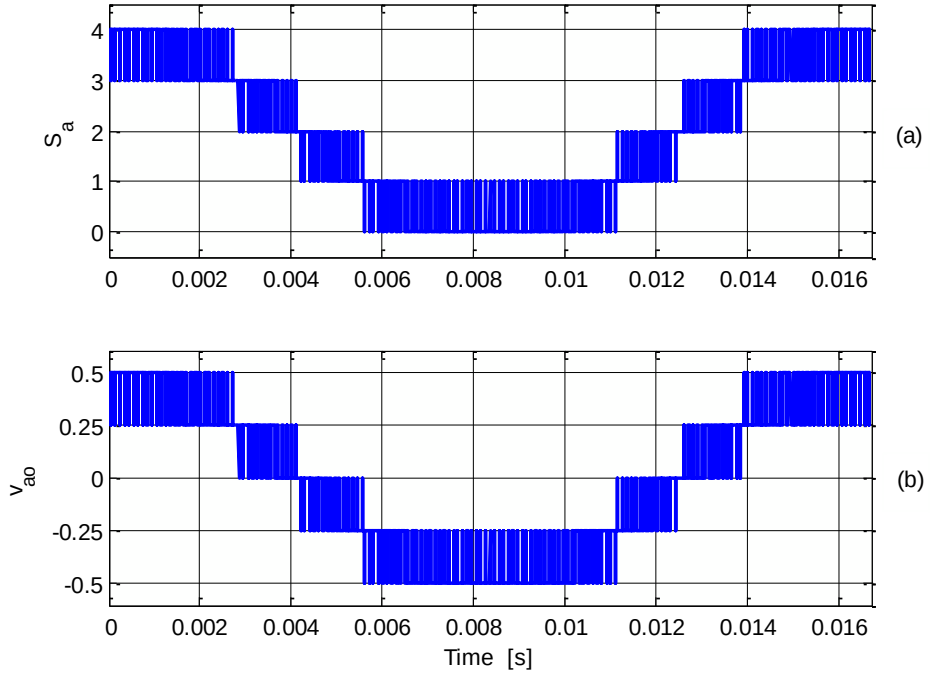

Figure 10 POD method for five-level inverter (a) switching function (S_i) (b) phase switched voltage (v_{io}).

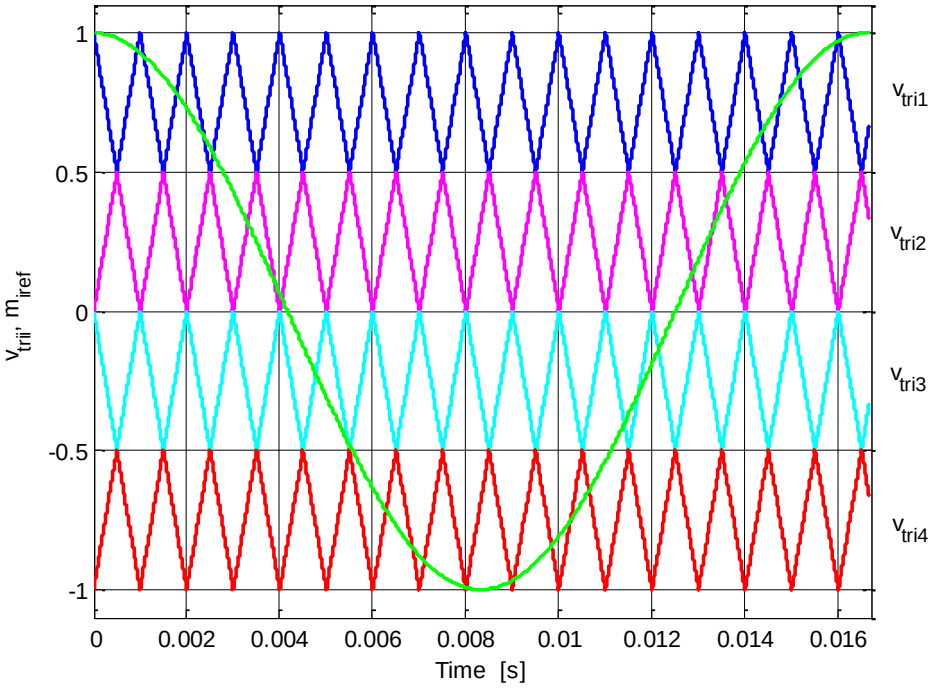

Figure 11 APOD method for five-level inverter (n-1) carrier signals and one reference modulation signal.

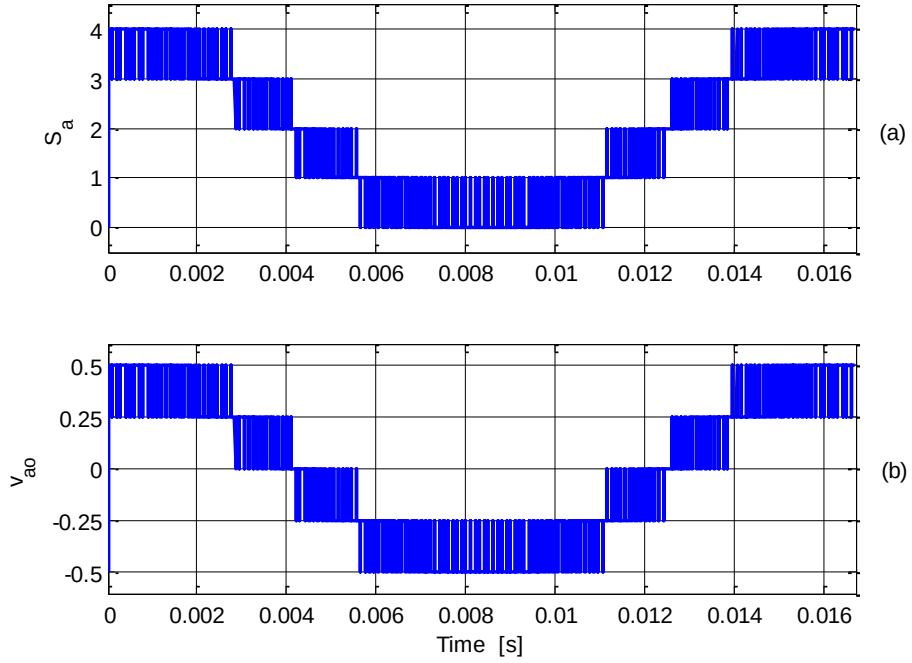

Figure 12 APOD method for five-level inverter (a) switching function (S_i) (b) phase switched voltage (v_{io}).